Delta-Sigma ADCs in Wireless Transceivers

Ian Galton
University of California, San Diego, CA

UCSD INTEGRATED SIGNAL PROCESSING GROUP

Outline

- Uses of ΔΣ Data Converters in Wireless Transceivers
- A Brief, Self-Contained ΔΣ ADC Overview
- The Receiver Demodulation Problem
- Nyquist-rate ADCs Versus Oversampling ΔΣ ADCs in Receivers with Quadrature Baseband Demodulation

1

ΔΣ Data Converters in Wireless Systems

Typical Applications in Wireless Systems

ΔΣ ADCs:
- Receive Demodulation
- Received Signal Strength Measurement
- Audio CODECs

ΔΣ DACs:
- Audio CODECs

Fractional-*N* PLLs:
- Local Oscillator Synthesis
- Transmit Frequency/Phase Modulation

Reason for Wide-Spread Use in Wireless Systems

Often need very high-precision data conversion over bandwidths that are narrow compared to practical sample-rates [1]

2

Outline

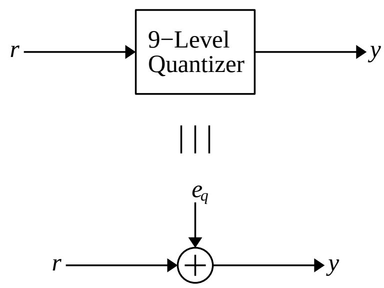
- Uses of ΔΣ Data Converters in Wireless Transceivers
- **A Brief, Self-Contained ΔΣ ADC Overview**
- The Receiver Demodulation Problem
- Nyquist-rate ADCs Versus Oversampling ΔΣ ADCs in Receivers with Quadrature Baseband Demodulation

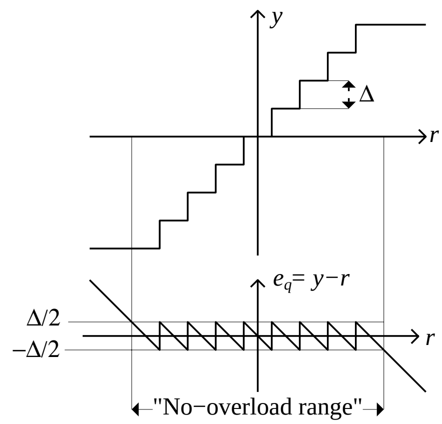
3

Quantizer Example

Most ΔΣ modulators involve feedback around uniform quantizers [2]

Example: a 9-level uniform quantizer

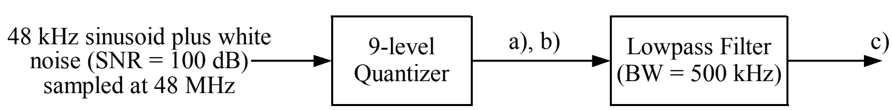


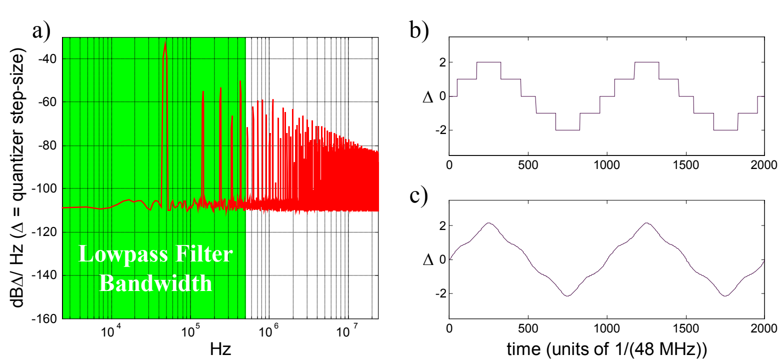


4

Quantizer Example

Such quantizers alone do not have well-behaved quantization noise:



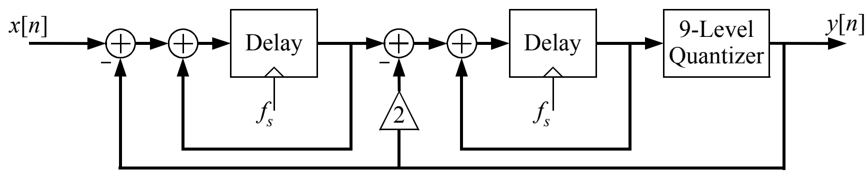


In the 0-500 kHz band, the SNR is only 14 dB

5

ΔΣ Modulator Example [3]

A *second-order* ΔΣ *modulator* using the same 9-level uniform quantizer



Can show:

$$y[n] = x[n-2] + \underbrace{e_q[n] - 2e_q[n-1] + e_q[n-2]}_{\Delta\Sigma \text{ Modulator Quantization Noise}}$$

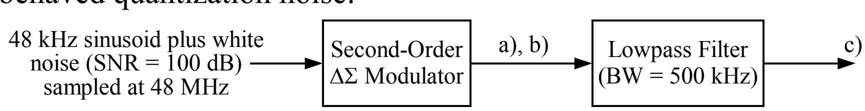
Idea: The quantizer noise, $e_q[n]$, is subjected to two zero-frequency zeros whereas the signal is just delayed

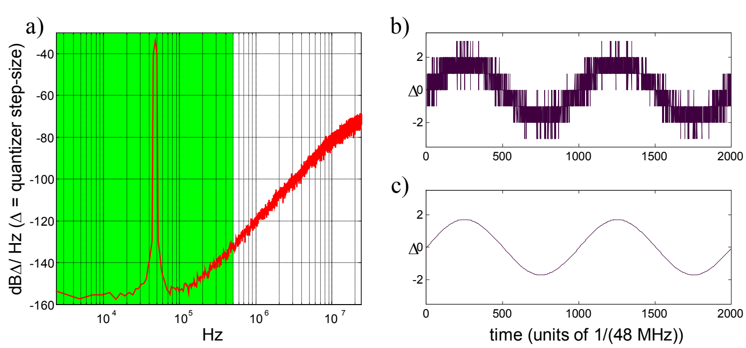
⇒ Quantization noise power is mostly at high frequencies

6

ΔΣ Modulator Example

Unlike the 9-level quantizer alone, the ΔΣ modulator has well-behaved quantization noise: [4-6]

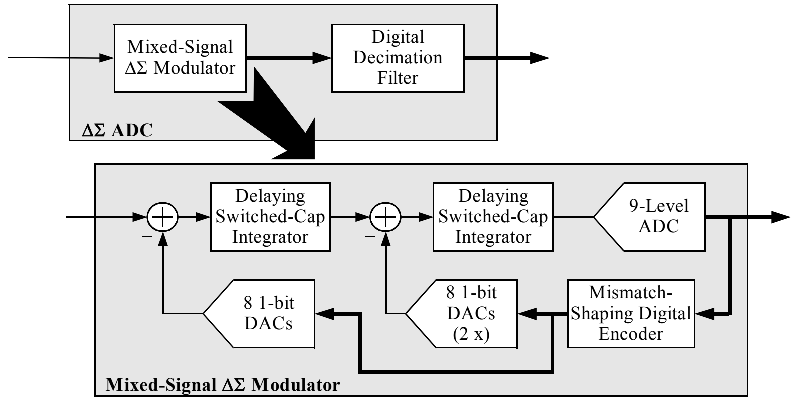




In the 0-500 kHz band, the SNR is 84 dB with no spurious tones!

7

An ADC Based on the Example ΔΣ Modulator



- ΔΣ sample-rate >> Nyquist rate
  ⇒ *ΔΣ output = lowpass desired signal + highpass quant. noise*
  ⇒ *Decimation filter removes most of the quantization noise*

- Mismatch-shaping minimizes in-band error from DAC step-size mismatches [7-20]

8

Other ΔΣ Modulator Options:

Single-Bit Quantization: [21-22]

Avoids need for mismatch-shaping DACs. Used to be the norm prior to the invention of mismatch-shaping DACs. Still used frequently.

Higher-order Quantization Noise Shaping: [23-25]

Used to further suppress in-band quantization noise.

Bandpass Quantization Noise Shaping: [26-29]

Used in ADCs to efficiently digitize signals in narrow bands away from dc.

Continuous-time loop filtering: [30-33]

More difficult to design, but sometimes used in ultra-low power, or bandpass applications.

9

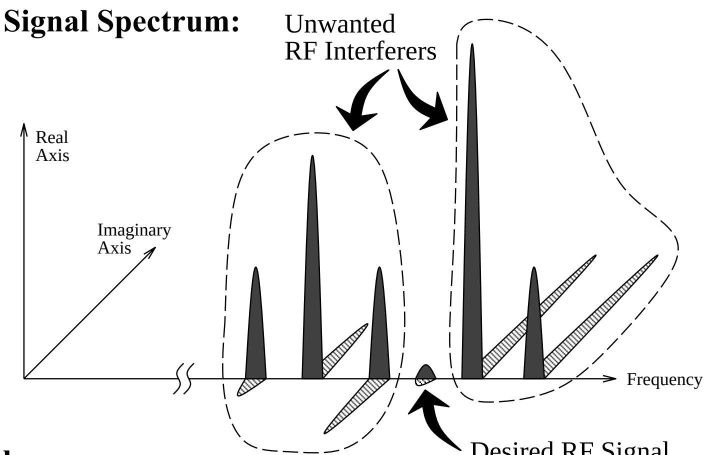
Outline

- Uses of ΔΣ Data Converters in Wireless Transceivers
- A Brief, Self-Contained ΔΣ ADC Overview
- **The Receiver Demodulation Problem**
- Nyquist-rate ADCs Versus Oversampling ΔΣ ADCs in Receivers with Quadrature Baseband Demodulation

10

Demodulation Tasks [39-40]

RF Signal Spectrum:

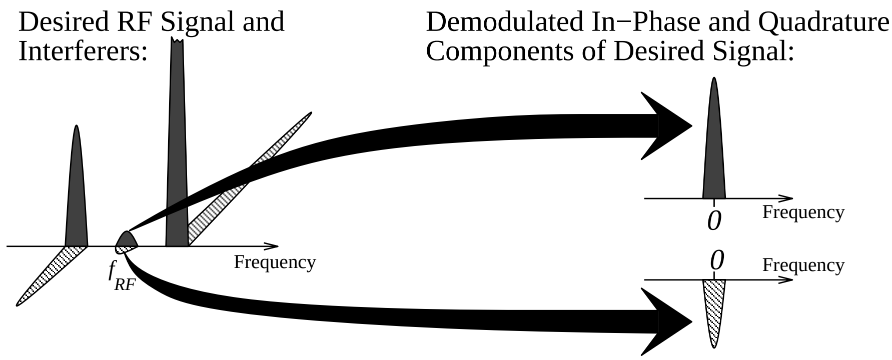


Tasks:

- Remove Interferers
- Downconvert real and imaginary parts of desired RF signal to "manageable" frequencies

11

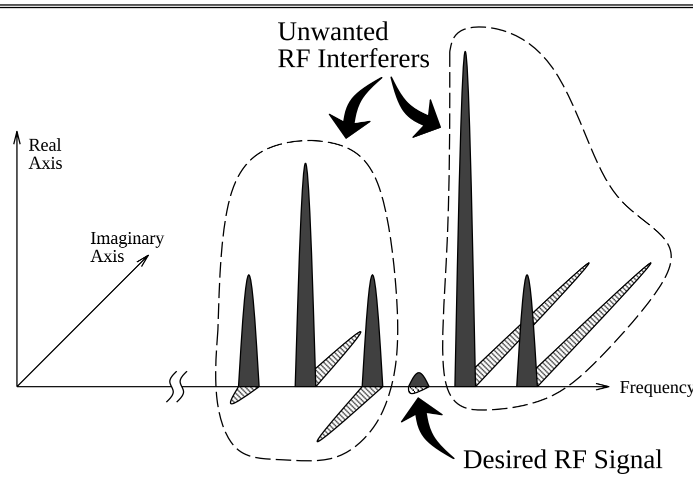
Quadrature Demodulation



Phase of desired signal's carrier is arbitrary, so must preserve both real and imaginary parts

⇒ Demodulation to dc (or near dc) requires two output signals: "in-phase" and "quadrature"

Demodulation Challenges



- Desired signal can be very small (e.g., -104dBm or 2μV peak amplitude for GSM)
- Interferers can be very large (e.g., -23dBm or 22mV peak for GSM)

Significance of Potentially Small Desired Signal

- *Need high-gain amplification prior to ADC S/H*
- *Noise performance of initial amplifier stages is critical*

GSM Example:

Minimum Discernable Signal at antenna connector	= 2μV peak
Minimum SNR required at detector	= 9dB
Two-sided 3dB signal bandwidth	≈ 160kHz

$\Rightarrow$ Maximum input referred noise $\approx 1.3\text{nV}/\sqrt{\text{Hz}}$

14

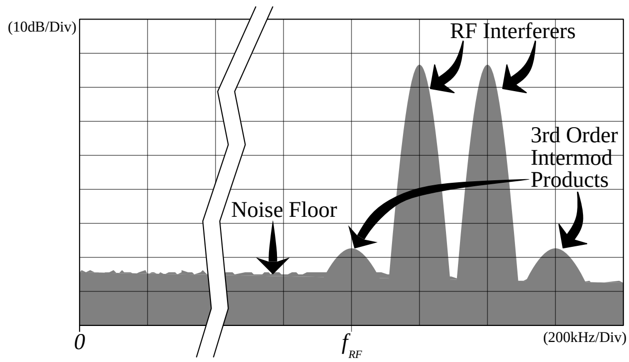
Significance of Potentially Large Interferers

- Amplification and downconversion stages prior to attenuation of the interferers by channel filtering must have high linearity (how linear depends on demodulator topology)
- Phase noise of local oscillator used in downcoversion process must be very low (e.g., -140dBc/Hz at 1.6MHz in GSM)
- Dynamic range of demodulation circuitry (and possibly the ADC) must be large (e.g., ≈ 100dB in GSM)

15

Effect of Third-Order Receiver Non-Linearity

PSD of two RF interferers after a third-order non-linearity:

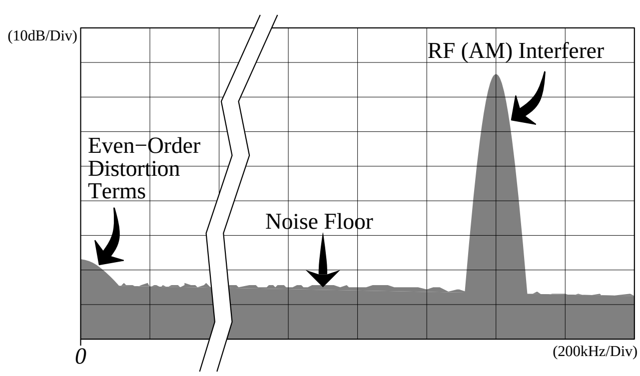


- Intermodulation product from interferers at Δf and $2\Delta f$ from desired signal frequency corrupts desired signal
- Similar situations with higher-order odd non-linearities, but effects are usually reduced (amplifiers and mixers tend to be "weakly non-linear")

16

Effect of Even-Order Receiver Non-Linearities

PSD of an AM interferer after even-order non-linearities:



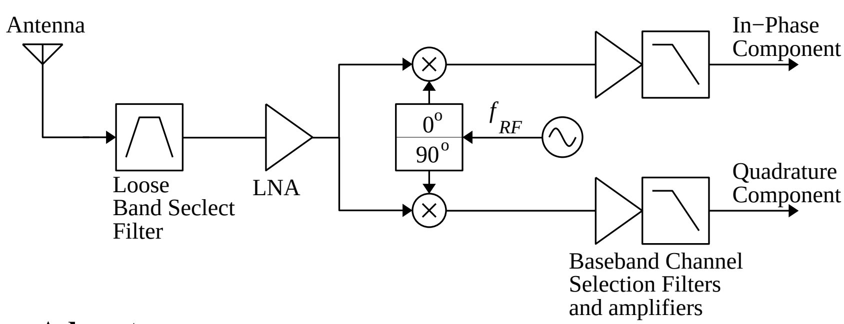
- Have distortion at dc regardless of interferer frequency
- Differential circuits can suppress such distortion up to about 35dB
- Second-order distortion is usually most significant

17

Outline

- Uses of ΔΣ Data Converters in Wireless Transceivers
- A Brief, Self-Contained ΔΣ ADC Overview
- The Receiver Demodulation Problem
- **Nyquist-rate ADCs Versus Oversampling ΔΣ ADCs in Receivers with Quadrature Baseband Demodulation**

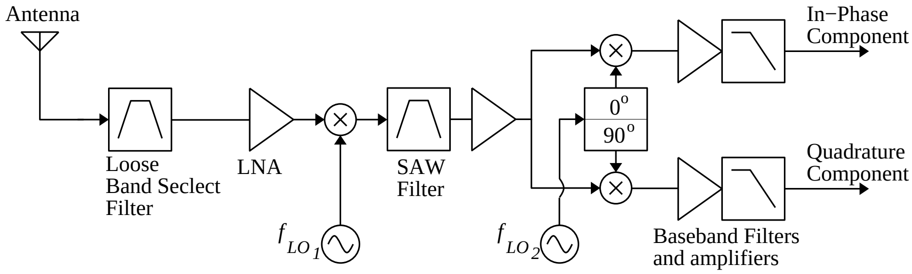
Direct Conversion Quadrature Demodulation [39-41, 57]



Advantages:
- Avoids (expensive) off-chip filters
- With digital channel filtering, facilitates “software radios”

Disadvantages:
- Sensitive to (2nd and 3rd order) non-linearities in baseband amplifiers (because large interferers still present)
- Prone to errors from “local oscillator self-mixing”

Superheterodyne Quadrature Demodulation [39-40]



Advantages:

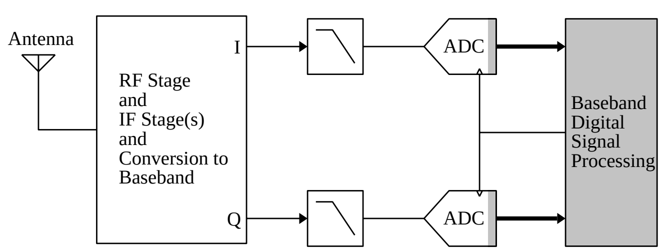
- Low distortion, low noise, passive bandpass filters attenuate interferers prior to baseband circuitry
  - ⇒ *greatly reduces baseband linearity requirements*
  - ⇒ *eliminates local oscillator self-mixing problem*

Disadvantages:

- Requires (expensive) off-chip passive components
- Requires careful frequency planning to limit spurious responses

20

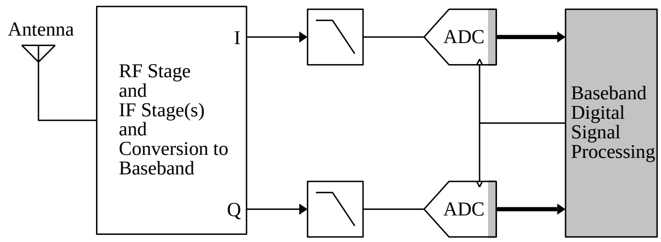
Quadrature Baseband Sampling Options



- **Option 1**: Channel selection/shaping filter is continuous-time analog
- **Option 2**: Channel selection/shaping filter is partly digital

21

Quadrature Baseband Sampling Option 1

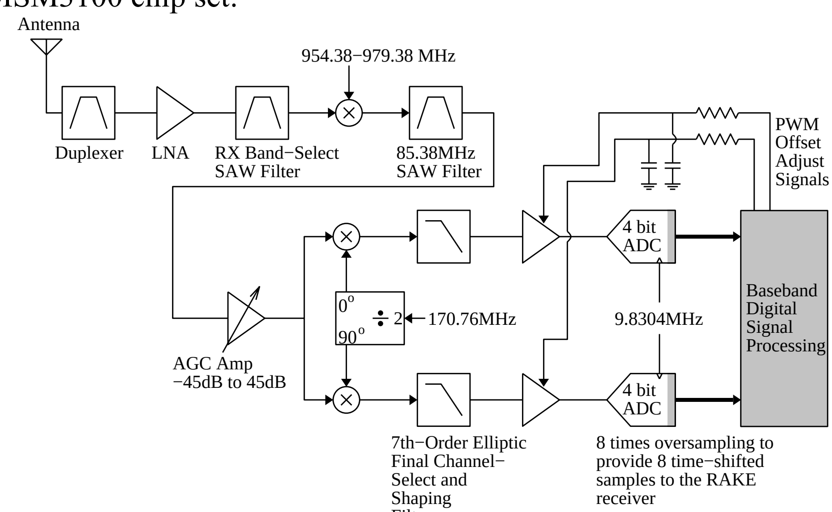


Option 1: Channel selection/shaping filter is continuous-time analog

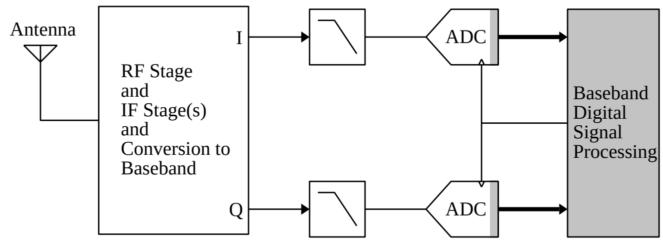
- symbol-rate ≤ sample-rate ≤ Nyquist-rate of channel
- ADC Precision: < 4-10 bits

Option 1 Example

An IS-95 receiver based on the Qualcomm RFR3100, IRF3000, MSM3100 chip set:



Quadrature Baseband Sampling Option 2

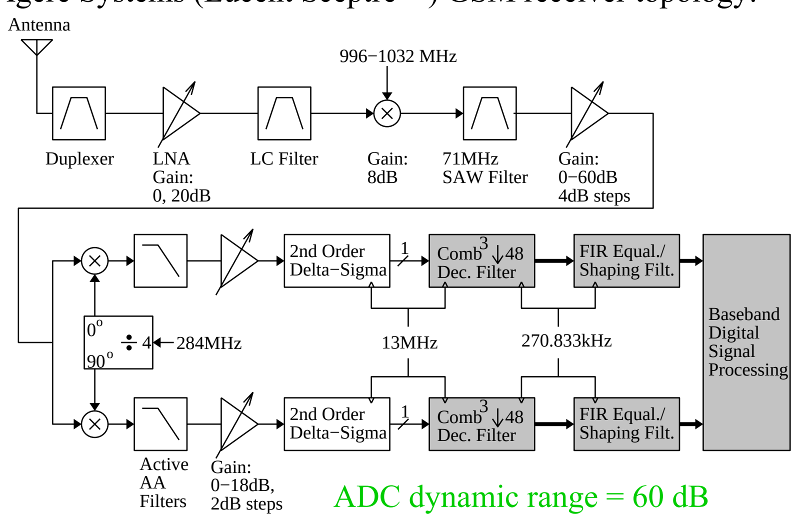


Option 2: Channel selection/shaping filter is partly digital

- sample-rate > Nyquist-rate of channel
- ADC Precision: > 4-10 bits

Option 2 Example

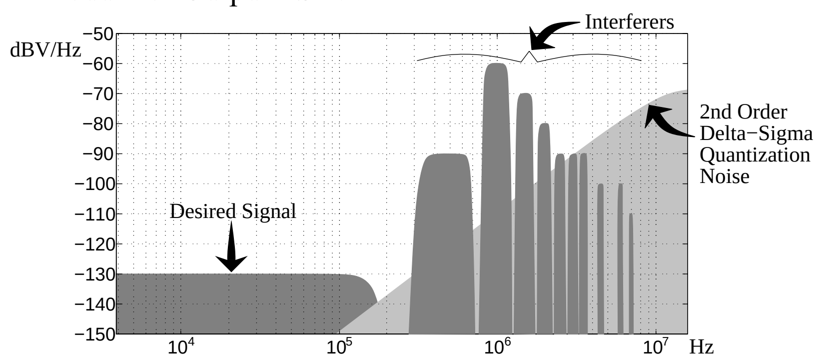
Agere Systems (Lucent Sceptre™) GSM receiver topology: [41-43]



ADC dynamic range = 60 dB

ΔΣ ADCs in Quadrature Demodulator Receivers

ΔΣ Modulator Output PSD:



- Oversampling and good linearity of ΔΣ ADCs
  - ⇒ *Interferers don't "fold down" onto desired signal*
  - ⇒ *Channel filtering can be mostly digital*
- Low out-of-band precision of ΔΣ ADCs
  - ⇒ *Don't waste power and area accurately digitizing interferers*

Analog Versus Digital Filtering [42-50]

In general, increasing the percentage of filtering performed digitally in a receiver implies:

1) The ADC sample-rate must increase

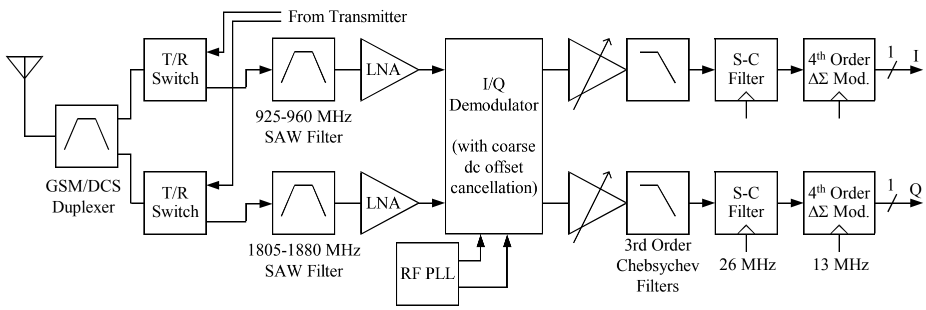
2) The ADC dynamic range must increase

3) Less analog filtering ⇒ interferers and are less attenuated prior to the ADC ⇒ the linearity of the IF and baseband stages must increase

4) Less gain is required prior to the ADC, and dc offsets from the radio are less of a problem ⇒ greatly eases the design of direct conversion receivers

A Direct-Conversion Option 2 Example [44-46]

Analog Devices Othello™ GSM/DCS Receiver:

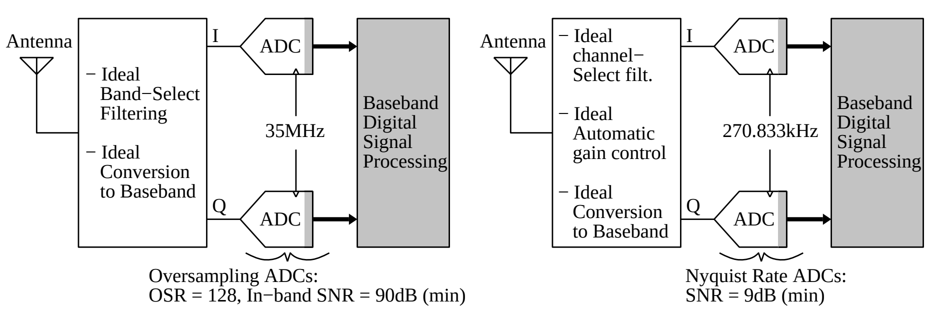


Relaxed analog filtering ⇒ Required ADC dynamic range = 80 dB

In this and other high-performance direct-conversion receivers, ΔΣ ADCs have proven to be enabling technology [44-46, 56-59]

ADC Performance Extremes: GSM Example

Full Digital Channel Selection: **Full Analog Channel Selection:**



Relevant GSM Specs:

- *MDS = –104dBm*
- *Required SNR at decoder = 9dB*
- *Maximum in-band blocking signal = –23dBm*

In practice, non-ideal radio performance tends to increase the ADC requirements above those shown here.

Conclusion

Have Provided Tutorial Coverage of:

- ΔΣ data converters
- The receiver demodulation problem
- Receivers with quadrature baseband ADCs
- Why ΔΣ ADCs help make direct conversion receivers practical

Important Topics Not Covered for Lack of Time:

- Receivers with *intermediate frequency* bandpass ADCs [54-55]
- Audio CODECs
- Local oscillator generation and transmit modulation using fractional-*N* PLLs [34-39]

30

Delta-Sigma ADCs in Wireless Transceivers References

1. I. Galton, "Delta-sigma data conversion in wireless transceivers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 302-315, January 2002.

2. *Delta-Sigma Data Converters, Theory, Design, and Simulation*, S. R. Norsworthy, R. Schreier, and G. C. Temes, Eds. New York: IEEE Press, 1997.

3. G. Lainey, R. Saintlaurens, P. Senn, "Switched-capacitor second-order noise-shaping coder," *IEE Electronics Letters*, vol. 19, pp. 149-150, February 1983.

4. J. C. Candy, "A Use of double integration in sigma delta modulation," *IEEE Transactions on Communications*, vol. COM-33, no.3, pp. 249-258, March 1985.

5. N. He, F. Kuhlmann, A. Buzo, "Multiloop sigma-delta quantization," *IEEE Transactions on Information Theory*, vol. 38, no.3, pp.1015-1028, May 1992.

6. I. Galton, "Granular quantization noise in a class of delta-sigma modulators," *IEEE Transactions on Information Theory*, vol. 40, no. 3, pp. 848-859, May 1994.

7. B. H. Leung, S. Sutarja, "Multi-bit sigma-delta A/D converter incorporating a novel class of dynamic element matching techniques,"*IEEE Trans. on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 39, no. 1, pp. 35-51, Jan. 1992.

8. M. J. Story, "Digital to analogue converter adapted to select input sources based on a preselected algorithm once per cycle of a sampling signal," U.S. Patent No. 5,138,317, Aug. 11, 1992.

9. H. Spence Jackson, "Circuit and Method for Cancelling Nonlinearity Error Associated with Component Value Mismatches in a Data Converter," U.S. Patent No. 5,221,926, June 22, 1993.

10. F. Chen, B. H. Leung, "A high resolution multibit sigma-delta modulator with individual level averaging,"*IEEE Journal of Solid-State Circuits*, vol. SC-30, no. 4, pp. 453-460, April 1995.

11. R. T. Baird, T. S. Fiez, "Linearity enhancement of multi-bit ΔΣ A/D and D/A converters using data weighted averaging,"*IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 42, no. 12, pp. 753-762, Dec. 1995.

12. R. Schreier, B. Zhang, "Noise-shaped multi-bit D/A converter employing unit elements,"*IEE Electronics Letters*, vol. 31, no. 20, pp. 1712-1713, Sept. 28, 1995.

13. R. W. Adams, T. W. Kwan, "Data-directed Scrambler for Multi-bit Noise Shaping D/A Converters," U.S. Patent No. 5,404,142, Apr. 4, 1995.

14. T. W. Kwan, R. W. Adams, R. Libert, "A stereo multibit Sigma Delta DAC with asynchronous master-clock interface,"*IEEE Journal of Solid-State Circuits*, vol. 31, no. 12, pp. 1881-1887, Dec. 1996.

15. R. Adams, K. Nguyen, K. Sweetland, "A 113-dB SNR oversampling DAC with segmented noise-shaped scrambling,"*IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 1871-1878, Dec. 1998.

16. I. Galton, "Spectral shaping of circuit errors in digital-to-analog converters," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 44, no. 10, pp. 808-817, Oct. 1997.

17. I. Galton, "Spectral Shaping of Circuit Errors in Digital-to-Analog Converters, " U.S. Patent No. 5,684,482, Nov 4, 1997.

18. A. Yasuda, H. Tanimoto, T. Iida, "A third-order ΔΣ modulator using second-order noise-shaping dynamic element matching," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 1879-1886, Dec. 1998.

19. I. Fujimori, L. Longo, A. Hairapetian, K. Seiyama, S. Kosic, J. Cao, S. Chan, "A 90dB SNR, 2.5 MHz output rate ADC using cascaded multibit delta-sigma modulation at 8x Oversampling Ratio,"*Journal of Solid-State Circuits*, vol 35, no. 12,pp. 1820-1828, December 2000.

20. E. Fogleman, J. Welz, I. Galton, "An audio ADC Delta-Sigma modulator with 100-dB peak SINAD and 102-dB DR using a second-order mismatch-shaping DAC," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 3, p.339-348, March 2001.

21. W. L. Lee, C. G. Sodini, "A topology for higher order interpolative coders," *Proceedings of the 1987 IEEE International Symposium on Circuits and Systems*, vol. 2, pp.459-462, May 1987.

22. K. C.-H. Chao, S. Nadeem, W. L. Lee, C. G. Sodini, "A higher order topology for interpolative modulators for oversampling A/D converters," *IEEE Transactions on Circuits and Systems*, vol. 37, no.3, p.309-318, March 1990.

23. S. K. Tewksbury, R. W. Hallock, "Oversampled, linear predictive and noise-shaping coders of order $N > 1$," *IEEE Transactions on Circuits and Systems*, vol. CAS-25, pp. 436-447, July 1978.

24. Y. Matsuya, K. Uchimura, A. Iwata, T. Kobayashi, M. Ishikawa, T. Yoshitome, "A 16-bit oversampling A-to-D conversion technology using triple integration noise shaping," *IEEE Journal of Solid-State Circuits*, vol. SC-22, pp. 921-929, December 1987.

25. K. Uchimura, T. Hayashi, T. Kimura, A. Iwata, "Oversampling A-to-D and D-to-A converters with multistage noise shaping modulators," *IEEE Transactions on Acoustics, Speech, and Signal Processing*, vol. AASP-36, pp. 1899-1905, December 1988.

26. T. H. Pearce, A. C. Baker, "Analogue to digital conversion requirements for HF radio receivers," *Proceedings of the IEE Colloquium on System Aspects and Applications of ADCs for Radar, Sonar, and Communications*, London, Digest No. 1987/92, November 1987.

27. P. H. Gailus, W. J. Turney, F. R. Yester Jr., "Method and arrangement for a sigma delta converter for bandpass signals," U.S. Patent No. 4,857,928, August 15, 1989.

28. R. Schreier, W. M. Snelgrove, "Bandpass sigma-delta modulation," *IEE Electronics Letters*, vol. 25, no. 23, pp. 1560-1561, November 1989.

29. S. Jantzi, R. Schreier, M. Snelgrove, "Bandpass sigma-delta analog-to-digital conversion," *IEEE Transactions on Circuits and Systems*, vol. 38, no.11, pp. 1406-1409, November 1991.

30. H. Inose, Y. Yasuda, J. Murakami, "A telemetring system by code modulation—ΔΣ modulation," *IRE Transactions on Space Electronics and Telemetry*, vol. SET-8, pp. 204-209, September 1962.

31. R. Schreier, B. Zhang, "Delta-sigma modulators employing continuous-time circuitry," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 43, no.4, pp. 878-879, April 1996.

32. E. J. van der Zwan, E. C. Dijkmans, "A 0.2-mW CMOS ΣΔ modulator for speech coding with 80 dB dynamic range," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 12, pp. 1873-1880, December 1996.

33. G. Raghavan, J. F. Jensen, J. Laskowski, M. Kardos, M. G. Case, M. Sokolich, S. Thomas III, "Architecture, design, and test of continuous-time tunable intermediate-frequency bandpass delta-sigma modulators," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 1, pp. 5-13, January 2001.

34. P. M. Gardner "Charge-pump phase-lock loops," *IEEE Transactions on Communications*, vol. COM-28, pp. 1849-1858, November 1980.

35. Bluetooth Wireless LAN Specification, Version 1.0, 2000.

36. B. Miller, B. Conley, "A multiple modulator fractional divider," *Annual IEEE Symposium on Frequency Control*, vol. 44, pp. 559-568, March 1990.

37. B. Miller, B. Conley, "A multiple modulator fractional divider," *IEEE Transactions on Instrumentation and Measurement*, vol. 40, no. 3, pp. 578-583, June 1991.

38. T. A. Riley, M. A. Copeland, T. A. Kwasniewski, "Delta-sigma modulation in fractional-N frequency synthesis," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 5, pp. 553-559, May, 1993.

39. B. Razavi, *RF Microelectronics*, Prentice Hall, 1997.

40. T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, 1998.

41. A. Abidi, "Direct conversion radio transceivers for digital communication," *IEEE*

Journal of Solid-State Circuits, vol. 30, no. 12, pp. 1399-1410, December 1995.

42. T. D. Stetzler, I. G. Post, J. H. Havens, M. Koyama, "A 2.7-4.5 V single chip GSM transceiver RF integrated circuit," *IEEE Journal of Solid-State Circuits*, vol. 30, no.12, pp. 1421-1429, December 1995.

43. Lucent Technologies, W2020 and CSP1088 data sheets, September 1996 and July 1995, respectively.

44. J. Strange, S. Atkinson, "A direct conversion transceiver for multi-band GSM application," Digest of Papers, *2000 IEEE RFIC Symposium*, pp. 25-28, June 2000.

45. Analog Devices AD6523 Zero-IF GSM Transceiver IC Data Sheet, 2001.

46. P. F. Ferguson, Jr., "ΣΔ designs in the wireless handset: a case study," MEAD Short Course, EPFL, Lausanne, Switzerland, July 2000.

47. E. J. van der Zwan, K. Philips, C.A.A. Bastiaansen, "A 10.7-MHz IF-to-baseband Sigma Delta A/D conversion system for AM/FM radio receivers," *IEEE Journal of Solid-State Circuits*, vol. 35, no.12, pp.1810-19, Dec. 2000.

48. Silicon Wave SiW1502 Bluetooth Radio Modem IC Data Sheet, November 3, 2000.

49. J. Grilo, I. Galton, K. Wang and R. Montemayor, "A 12 mW ADC Delta-Sigma Modulator with 80dB of Dynamic Range Integrated in a Single-Chip Bluetooth Transceiver," *IEEE Custom Integrated Circuits Conference*, May 2001.

50. O. Oliaei, P. Clement, P. Gorisse, "A 5mW ΣΔ modulator with 84dB dynamic range for GSM/EDGE," Digest of Technical Papers, *IEEE International Solid-State Circuits Conference*, vol. 44, February, 2001.

51. S. Willingham, M. Perrott, B. Setterberg, A. Grzegorek, B. McFarland, "An integrated 2.5GHz ΣΔ frequency synthesizer with 5μs settling and 2Mb/s closed loop modulation," Digest of Technical Papers, *IEEE International Solid-State Circuits Conference*, vol. 43, pp. 200-201, Feb. 2000.

52. M. H. Perrott, T. L. Tewksbury III, C. G. Sodini, "A 27-mW CMOS fractional-N synthesizer using digital compensation for 2.5-Mb/s GFSK modulation," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 12, pp. 2048-2059, Dec. 1997.

53. N. Filiol, et. al., "A 22 mW Bluetooth RF transceiver with direct RF modulation and on-chip IF filtering," Digest of Technical Papers, *IEEE International Solid-State Circuits Conference*, vol. 43, pp. 202-203, Feb. 2001.

54. R. Schreier, J. Lloyd, L. Singer, F. Weiss, B. Sam, D. Paterson, C. Jacobs, J. Steinheider, M. Timko, J. Zhou and W. Martin, "A Flexible 10-300 MHz Receiver IC Employing A Bandpass Sigma-Delta ADC," Digest of Papers, *IEEE RFIC Symposium*, June 2001.

55. R. Schreier, J. Lloyd, L. Singer, D. Paterson, M. Timko, M. Hensley, G. Patterson, K. Behel, J. Zhou, W. J. Martin, "A 50mW bandpass ΣΔ ADC with 333kHz BW and 90dB DR," Digest of Technical Papers, *IEEE International Solid-State Circuits Conference*, vol. 1, February, 2002.

56. M. Miller, C. S. Petrie, "A multibit sigma–delta ADC for multimode receivers," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 3, pp. 475-482, March 2003.

57. D. Manstretta, M. Brandolini, F. Svelto, "Second-order intermodulation mechanisms in CMOS downconverters," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 3, pp. 464-474, March 2003.

58. G. Chang, L. Jansson, K. Wang, J. Grilo, R. Montemayor, C. Hull, M. Lane, A. X. Estrada, M. Anderson, I. Galton, S. V. Kishore, "A direct-conversion single-chip radio-modem for Bluetooth," *2002 IEEE International Solid-State Circuits Conference,* pp. 88-89, 448, February, 2002.

59. K. Philips, "A 4.4mW 76dB complex ΣΔ ADC for bluetooth receivers," *2003 IEEE International Solid-State Circuits Conference,* pp. 64-65, 478, February, 2003.