Multistep Integrated A/D Converters

P. Jespers
Catholic University of Louvain, Belgium
Jespers@dice.ucl.ac.be

I. MULTISTEP A TO D CONVERTERS [1]

Flash converters reach currently sampling rates of 1 to 2 GHz with 6 to 8 bits resolution. Delta-Sigma converters attain 15 to 16 bits but their bandwidth hardly exceeds 10 to 20 MHz. Neither of the two offers suitable alternatives in the range 20 to 100 MS/s considering 8 to 13-bit resolutions.
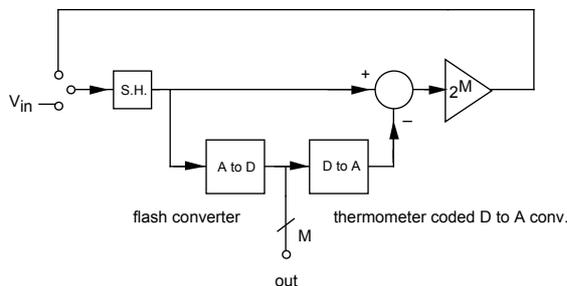

Fig 1: Multistep converters take advantage of subconverters in order to divide the conversion process in sub-steps, according to recycling (above) or pipelined architectures.

Multistep converters offer a sensible alternative [2,3]. The idea is to divide the conversion process in two, three or more steps taking advantage of flash converters and fast parallel D to A converters with few bits only. The result is a substantial savings as far as area and power. For instance, a 2-cycle Multistep converter may achieve 10 bits with only 31 or 62 comparators, depending which kind of architecture is considered, recycling or pipelined.

Few cycles keep the conversion times small but require more bits to be resolved per cycle stressing thus the tolerances. The time to perform one cycle is determined by a number of sub-steps. As shown in fig 1, an A to D conversion is performed first. It is followed by a D to A conversion, which generates the DC replica of the coarsely quantized data outputted by the A to D converter. The latter is subtracted from the analog input in order to evaluate the so-called quantization noise. This signal is amplified in order to expand its dynamic range until it gets the same as that of the input signal. This ends the first cycle. The amplified signal, which is called the 'residue', is now either recycled or fed to another identical cascaded sub-converter. A set of bits is generated every time a cycle is completed. They represent the digital counterpart of the analog input after being concatenated.

Among the operations described above, the most demanding is the amplification step. The number of bits M outputted by the flash converter sets the magnitude of the intermediate gain, which must be equal to 2^M. Amplification is done generally by means of a high performance Op Amp and a capacitive feedback loop as shown in the example of Fig. 2 representing an early version of a recycling 10-bit converter [4].
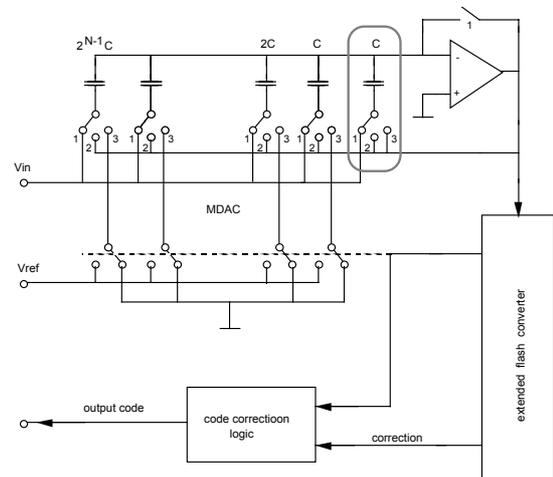

Fig. 2: An early version of a 5-bit 2-cycle recycling converter [4].

The input signal is sampled and stored in the binary array of capacitors to begin with (phase 1). Then, all the capacitors are decoupled from the input and connected in parallel across the input-output terminals of the Op Amp (phase 2). This completes the sample-and-hold phase. Since the Op Amp output is fed to the A to D flash converter, a first M-bit coded word is obtained. At the same time, the output data of the flash determine the positions of all switches connected to the capacitors except the smallest right one, which remains connected across the Op. Amp. (phase 3). The total charge stored in the array of capacitors, not including the last one, is now a replica of the coarsely quantized data delivered by the flash converter. Since the total charge that was stored in the array at the end of phase two represented the input signal, the difference, the quantization noise thus, is stored in the feedback capacitor. The Op Amp outputs consequently the

residue for the total capacitance connected to the flash converter divided by the Op Amp feedback capacitance is equals to 2^M. This completes the first sub-conversion cycle.

The allotted time per cycle and the expected accuracy determine the actual bandwidth and gain of the Op Amp During the acquisition time, the Op Amp is in the unity-gain configuration. An open-loop gain of 45 dB is sufficient to comply with the tolerances. The gain-bandwidth product can be optimized in order to reduce the acquisition time till 5 ns. When the residue is being evaluated, the loop gain must be much larger since M is relatively high. In the example an open-loop gain of 72 dB is required. Settling times below 20 ns are difficult to achieve under such circumstances. This sets the limit on speed.

Two-step resistive subranging flash converters [5] circumvent the problem for they don't need an Op Amp. They require however the same number of analog references as full-flash converters having the same resolution. The number of comparators is the same as in Multistep converters. The conversion process occurs in two phases. During the coarse conversion, the comparator's bank is connected to a sub-set of coarse references in order to find which segment of references encompasses the analog input. The fine references of this segment are connected to the comparators during the second step. No Op Amp is required but the offsets of the comparators may not exceed those of the equivalent full-flash converter.

II. ERROR ANALYSIS

Multistep converters are prone to various types of errors introduced by the A to D and D to A sub-converters mismatch, the intermediate gain error, the Op Amp offset and slew-rate (Fig. 3).
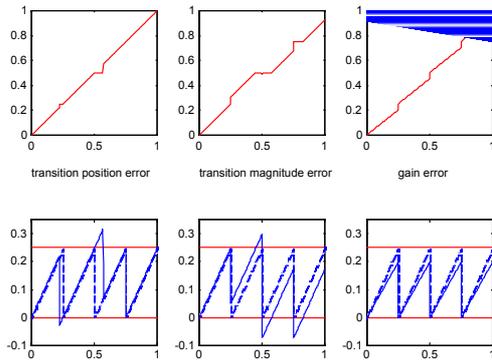

Fig. 3: Illustration of the impact of transition position (left), transition magnitude (middle) and gain error on the transfer characteristics (above) and residues (below).

The flash converter introduces *transition position* errors on account of the comparator's offsets. The D to A converter introduces *transition magnitude* errors, which are the result of its INL impairments. The *intermediate gain* error is a consequence of the capacitance mismatch. Transition position errors overload the sub-converters. Errors may be very large but when the conversion ranges of both, the flash and D to A sub-converter, are extended, these errors can be fully compensated. Linearity is reinstalled and the correct codes are recuperated even though the code words outputted by the flash converter are altered. Summing algebraically adjacent code words takes care of the problem indeed. The point is how to extend the dynamic range without being forced to increase the supply voltage. This can be done if the comparison levels of the flash converter correspond to the series:

$$ -1 - (Z-2).2^{-M} \; ; \; 2^{1-M} \; ; \; +1 + (Z-2).2^{-M} $$

M represents the number of bits resolved per cycle, Z the number of extra levels within the +/- 1 range. The most left and most right expressions are the comparison end-levels and the term in the middle is the distance between adjacent comparison levels. Similarly for the D to A converter, one has outputs:

$$ -1 - (Z-1).2^{-M} \; ; \; 2^{1-M} \; ; \; +1 + (Z-1).2^{-M} $$

with the same definitions.

The D to A converter error is more difficult to correct. Matching is essential. Since the number of unit-elements that belongs to the D to A converter is restricted to 2^M, whether capacitors or current sources, sizes may be relatively large. When current sources are used, the possibility to select the unit-elements according to a pseudo-random sequence offers a means to improve slightly the overall INL performances at the expense of the DNL. As far as spectrum, a concomitant reduction of harmonic distortion is obtained against a small increase of the noise floor.

The most challenging problem is the accuracy of the intermediate gain block. If M is equal to 5, a gain of 32 is required. This has not only an impact on the open loop gain of the Op Amp but also on the tolerances of the unit-elements. Errors don't affect the data outputted by the flash converter during the first cycle but the residue. A 2-cycle 5-bit converter tolerates an intermediate gain error as large as 1%. The situation is different when single-bit subconverters, called 'cyclic converters' are considered. The flash converter resumes to a comparator ignoring transition position errors, while the D to A converter outputs two levels only: + and − ref. The intermediate gain stage multiplies the magnitude of the quantization noise by two. This is easy to implement and lessens somehow the bandwidth

requirements of the Op Amp. The number of cycles gets larger however and the impact of the intermediate gain error is visible right after the first bit. The number of cycles equals the number of bits but the total conversion time is not strictly proportional to the ratio of cycles for the low intermediate gain allows faster operation of the Op Amp.

In a single-bit converter block, the Op Amp offset doesn't formulate a problem if the dynamic range of the sub-converters is extended. The output data are shifted by a quantity that is strictly proportional to the magnitude of the offset. This error can be removed numerically after zeroing. When the dynamic range of the internal sub-converters is not extended this is not possible. In the particular case of a 1.5-bit architecture, like the one considered below, the offset error is added simply to the output data. An easy compensation technique is to swap the I/O terminals of the Op. Amp. right after the first cycle. This annihilates the offset error while conversion cycles go on.

Noise affects the comparators and the Op Amp. The comparator's noise has no impact on the accuracy because it causes transition position errors, which don't impair the resolution as long as the dynamic range of both sub-converters is properly extended. The Op Amp noise however sets an upper limit to the achievable resolution making 14 bits difficult to attain.

III. A closer view to a 1.5-bit recycling A to D converter

A very interesting combination is obtained when the single-bit sub-converters dynamic range is extended by means of one single extra bit only [6,7]. The comparison levels according to the formula above become respectively + and − 0.25 for an input range between + and − 1. Three output levels must be implemented for the D to A converter, respectively −1, 0 and +1. As far as the flash converter tolerances, the comparison levels must be kept within 0 and + and - 0.5 respectively, in other words they don't care. The D to A mismatch may be reduced substantially when switched capacitor techniques are contemplated, for these guarantee equal height steps. Hence, there is no INL to take care of. Of course the D to A converter may introduce a global offset but, as stated earlier, its impact can be annihilated numerically. The only impairments left over are then the intermediate gain error and the unavoidable Op Amp noise. Calibration of the intermediate gain is feasible.

The achievable gain error sets an upper limit on the resolution. An accuracy of 0.1% is required for a 10-bit converter. But this error does not affect the whole dynamic range in the same way. As shown in fig. 4, the SNR plotted versus the magnitude of the input signal
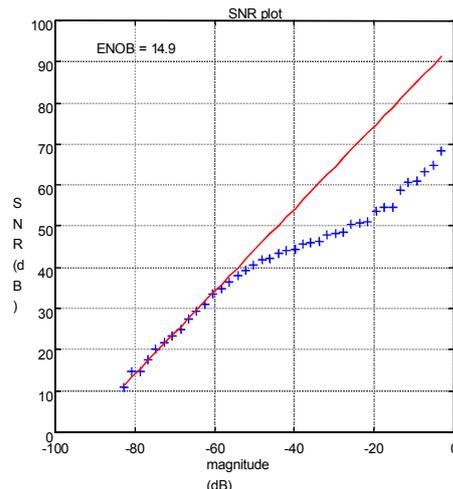

Fig. 4: SNR plot of a 1.5-bit 15-cycle converter with extended range considering 0.1 % error for the intermediate gain.

exhibits two regions: one for large signals where the extrapolated SNR exhibits an ENOB of 11 bits, and another for small signals where the ENOB reaches 15 bits. This region moves to the left with the numbers of cycles but in practice the Op Amp noise limits the range where this is applicable. In the region between − 20 and − 50 dB, the converter behaves like a kind of floating-point device. This may be a useful feature for telecom applications. It doesn't hold in the true 1-bit counterpart.

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