Automatic Generation of LH-BIST Architecture for ADC Testing

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Abstract – No generic BIST architecture exists for Analog-to-Digital Converters testing. For each application and test setup we thus have to build a dedicated BIST architecture. In this paper, we show that the LH-BIST architectures based on the Linear Histogram-based test technique are configurable and we evaluate hardware resources according to any given application. We also propose a software tool allowing the automatic generation of the LH-BIST description.

Keywords – ADC testing, Histogram-based test, BIST, configurable BIST architecture

I. INTRODUCTION

With the growing complexity of digital and analog circuits and the generalization of System-On-Chip (SOC), the price of mixed-signal circuits is being dominated by production testing costs. Indeed, the price of Automatic Test Equipment (ATE) becomes prohibitive because testing devices have to be regularly upgraded due to the evolution of mixed-signal circuits. Moreover, the poor observability and controllability of these high-complexity circuits demand ever increasing test time and resources. In this context, Built-In-Self Test (BIST) technique is an attractive alternative to reduce the testing cost. Indeed a BIST technique allows to get rid of expensive mixed-signal ATE, reducing the test time and improving the accessibility inside the chip. Many mature BIST techniques have been proposed over the past years for digital circuits. Today, several of these BIST techniques are incorporated into automatic synthesis tools and are used by most of digital designers.

The situation is not so advanced for analog and mixed-signal circuits. Generally, these mixed-signal circuits include an Analog-to-Digital Converter (ADC) to link analog and digital domains. Therefore, it is essential to define a generic BIST solution for this critical component. Unlike BIST solutions for digital circuits, the ADC BIST architecture might be different depending on the converter specifications: ADC resolution, sampling frequency, expected accuracy of ADC parameter measurement … Consequently, we need to develop a tool that enables the automatic generation of the BIST architecture description according to the considered application.

In the past few years, many published papers have dealt with the definition of BIST techniques for ADC. Number of the proposed techniques assume requirements on the pre-existing circuitry, such as the presence of both an ADC and a Digital-to-Analog Converter (DAC) and/or digital signal processing capabilities [1-2]. Other solutions, considering solely the ADC, concern either the analog test stimulus generation [8-12] or the digital output response analyze [3-7]. All techniques are dedicated to given applications.

The objective of our work is to develop a configurable BIST architecture with both a stimulus generator based on ramp or triangle wave generator and a digital analyzer based on the histogram-based BIST technique. As BIST structure depends on both the ADC under test and the test conditions, an automatic tool is proposed to generate various possible BIST structures (called LH-BIST for Linear Histogram-based BIST) for the considered application. Once the structure is chosen, the tool generates automatically both the VHDL description of the LH-BIST digital blocs and the size of the transistors used in the analog part of the LH-BIST circuitry.

The paper is organized as follows. Section II defines the LH-BIST scheme based on previous works and evaluates the needed hardware resources according to a given application (ADC under test and test conditions). The tool allowing the generation of such a LH-BIST architecture is described in section III.

II. CONFIGURABLE ADC BIST SCHEME

The BIST scheme we propose is dedicated to implement the histogram-based test technique for a linear input signal. In order to build this BIST structure we have to integrate both a stimulus generator based on technique proposed in [11-12] and a digital response analyzer based on technique presented in [5] as illustrated in figure 1.

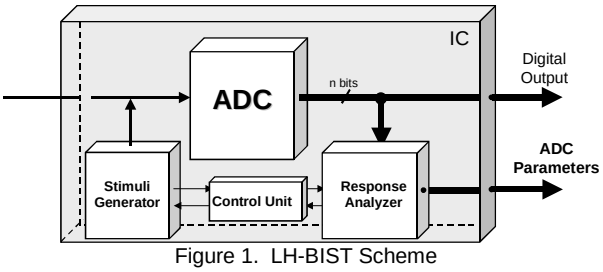

Figure 1. LH-BIST Scheme

II.1 Analog Stimulus Generator

The analog generator is based on the simple principle of a constant current charging a capacitor. Figure 2 and 3 give the conceptual scheme of two kinds of generators where Ic, C and Init are the charging current, the charging capacitor and the initialization signal respectively. In the case of the ramp generator (figure 2) the signal step simply defines the ramp period.

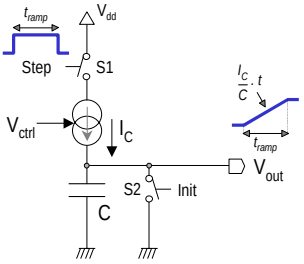

Figure 2. Ramp generator

Concerning the triangle wave generator (figure 3) the operating cycle is more complex.

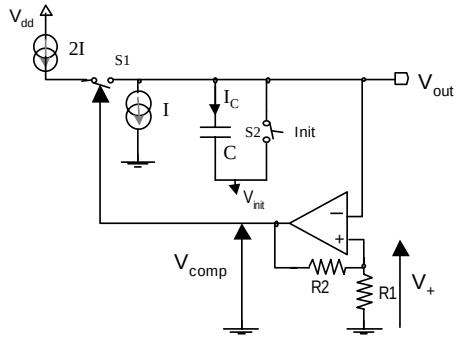

Figure 3. Triangle wave generator

We use two current generators connected by a switch. The switch is directly controlled by the output of a Schmitt trigger. In choosing the initial value of the generated signal lower than the negative threshold voltage of the trigger the switch is on involving that the charging current Ic, the slope of the signal and the threshold of the trigger are positive. When the generated signal is equal to the positive threshold voltage of the trigger the switch is off. Consequently, the charging current, the slope of the signal and the threshold voltage of the trigger are negative. When the generated signal is equal to the negative threshold voltage of the trigger the switch is on and the slope of the signal becomes positive and so on.

In order to achieve satisfactory quality in terms of linearity, the generators are based on *Wide Swing* current mirrors. These mirrors copy the current generated by a single transistor with a controlled gate-source voltage. This architecture allows to achieve 15 bits of linearity. Unfortunately, the BIST context forces us to use both small charging current and small charging capacitor in order to obtain the smallest area overhead. Moreover, the slope of the generated analog signal presents high sensitivity to process variations. Consequently, we have proposed an adaptive scheme to calibrate the slope of the generated linear signal.

In the case of ramp signal generation, the basic principle consists in comparing the generated ramp voltage to a predetermined reference voltage and feeding back an adjustment signal on the control voltage V_{ctr} so that the ramp voltage converges with the reference voltage within a given period. In the case of the triangle wave generator the basic principle of the calibration scheme consists in adjusting the positive charging current according to the sign of the trigger output within a given period $T_{Triangle}$. In this phase of calibration, the triangle wave signal is initialized every $T_{Triangle}$. As an illustration, figure 4 and 5 give respectively the scheme and the timing diagram of the adaptive triangle wave generator.

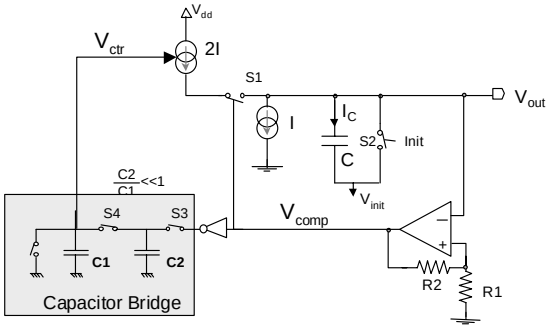

Figure 4. Scheme of the adaptive triangle-wave generator

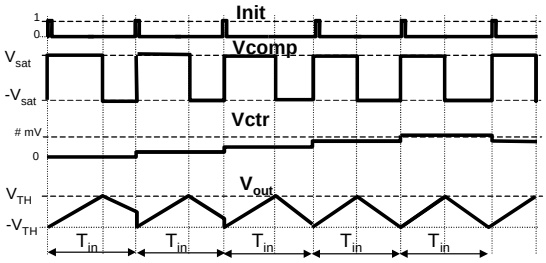

Figure 5. Timing diagram of the adaptive triangle-wave generator

Finally, the figure 6 and 7 shows the transistor level of the adaptive ramp and triangle-wave generators. The ramp signal generator is composed of several transistors, two capacitors and a comparator.

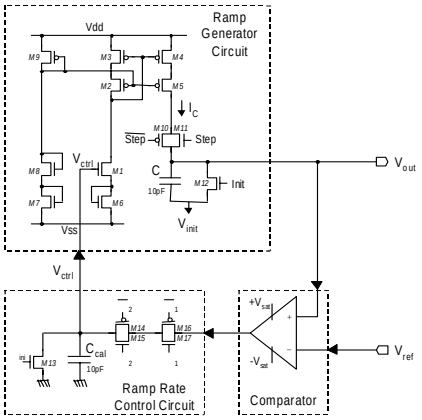

Figure 6. Ramp signal generator

Concerning the triangle-wave generator (figure 7), the Schmitt Trigger symbolized in figure 7 with an opamp and two resistors is actually built with a system of six transistors.

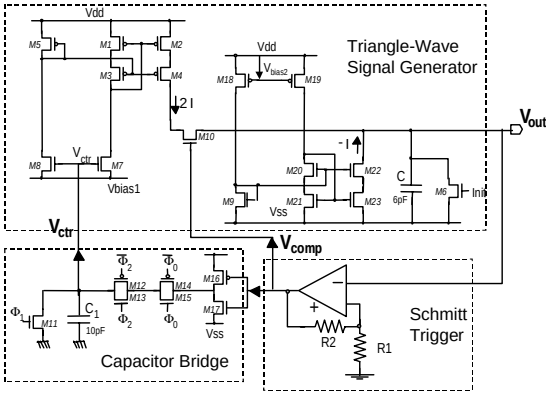

Figure 7. Adaptive triangle wave generator

Each of these generators has some advantages and drawbacks. The ramp generator is simple to use but the for each end of period we have to initialize the generated signal. In practice, the histogram-based test needs a lot of samples in order to achieve satisfactory statistical result. These samples can not be collected in a single period of the input signal and the initialization phases of the input signal is equivalent to a degradation of the overall linearity of the input test pattern "seen" through the ADC under test. In practice, the test pattern linearity in terms of equivalent resolution is equal to 10 bits. In contrast, the triangle-wave needs no initialization phase (out of calibration procedure) and it is possible to get an equivalent linearity of 13 bits.

In order to build the generator configuration into an automatic tool we have to define the parameter needed to configure the generator for a given application. Firstly, it is commonly accepted that the input stimulus applied on the ADC input should present a resolution 2 bits higher than the converter resolution. Consequently, the BIST structure automatic generator will choose the ramp generator for ADC resolution lower than 9 bits and the triangle-wave generator for ADC resolution higher than 9 bits. After the choice of the kind of generator, the automatic tool generates the transistors sizes and the capacitors value according to both the expected period of the generated signal and the full scale of the ADC.

II.2 DIGITAL RESPONSE ANALYZER

The histogram technique is based on a statistical analysis of the ADC output codes [13]. It is actually constituted of three steps. The first step consists in building the experimental histogram that represents the number of times each ADC output code appears for a given input signal. Then, this experimental histogram is compared with an ideal histogram obtained in the case of both ideal ADC and ideal analog input. Note that for a linear input signal this ideal histogram is perfectly flat along ADC codes. Finally, the main ADC parameters are extracted from the comparison between the two histograms.

The straightforward implementation of the histogram test technique requires two memories of 2^n words to store the experimental and the ideal histograms and a DSP to perform the computation needed to extract ADC parameters. Of course, it is not a viable solution in a BIST context. In order to reduce the required hardware resources, the proposed digital analyzer solution is based on time decomposition. Firstly, we replace the concurrent calculation of all the parameters by a sequential determination. Time-spread calculation allows us to reduce storage hardware. Then each phase is also sequentially decomposed. The one-bit bloc structure of this digital analyzer allowing the implementation of the histogram-based test technique is only composed of two small modules:

- A Detector Module (DM) that positions the reference code to be processed. Then, it compares this reference code with the running code delivered on the output of the ADC. So, this module contains a register together with configuration logic. Depending on the *Control* signal, the register is configured in either a counter or a comparator. Code selection is achieved in the counter mode by incrementing the counter until the reference code is

reached; then code comparison is performed in the comparator mode.

– An Exploitation Module (EM), which calculates the ADC parameters. As for the DM, this module is composed of a register together with a configuration logic controlled by the two signals *c1* and *c2*. Depending on the values applied on these control inputs, the module is configured in different operating modes. Basically, the module can either operate as an up/down counter to realize addition and subtraction or provide the 2's complement of the value stored in the register to manage the sign of results. Note that obviously, this module can compute division if the divisor is a power of 2. Indeed, the binary division by 2^P simply corresponds to a P-bit shift.

Figure 8 gives the one-bit circuitry needed for implementing the functionality of the DM and the EM, the complete modules being constituted of a cascade of these one-bit blocks.

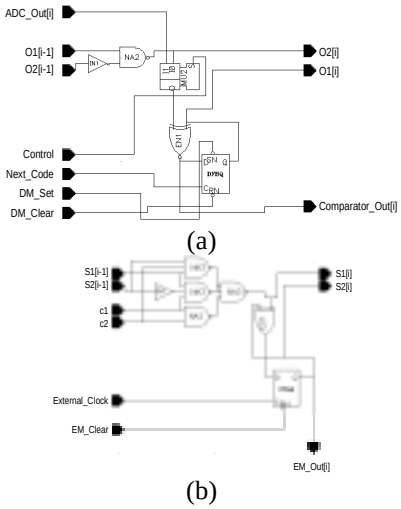

Figure 8. One-bit blocks for the DM (a) and the EM registers (b)

Now, in order to illustrate the operating principle of the test procedure, let us take the example of the gain error computation defined as:

$$\text{Gain}^{-1} = \frac{\sum_{i=N1}^{N2} H(i)}{m \cdot H_{ideal}} \qquad N2 = N1 + m$$

Where H(i) is histogram value of the code i (code count of i), H_{ideal} is the ideal count and m the number of central codes used in the gain determination. To perform the accumulation of the counts for the m central codes, the EM is configured as an up-counter and m input test patterns are applied. So for the first input test pattern, the first code N1 is positioned as the reference code in the DM and the EM is incremented each time the running code occurs on the ADC output. This operation is repeated m times incrementing the reference code until code N2. So, by the end of the m input test patterns, the EM holds the cumulative sum $\sum_{i=N1}^{N2} H(i)$. To obtain the Gain^{-1} value, this cumulative sum has to be divided by $m.H_{ideal}$. This division simply corresponds to a shift in the register if $m.H_{ideal}$ is a power of 2. Then, we impose $H_{ideal}=2^P$ and $m=2^Z$, and the division by 2^{P+Z} is equivalent to a (P+Z)-bit shift.

Concerning the incorporation of the digital analyzer construction into the automatic tool, we can note that the DM module is simply obtained by cascading as many one-bit blocks as the number of bits of the converter under test. Moreover, as for the DM, we cascade a number of one-bit blocks to build the Exploitation Module. However, the length of the register of EM does not only depend on the number of bits of the converter, but is determined by the calculation procedure. Indeed, the offset determination requires a (P+1)-bit shift in the register, the non-linearity determination requires a P-bit shift and we have seen that the gain determination requires a (P+Z)-bit shift. As a result, the length of the register has to be at least P+Z+1 bits, where P is determined from the ideal count ($H_{ideal}=2^P$) and Z from the number of codes on which the gain measurement is performed ($m=2^Z$). The choice of the ideal count value H_{ideal} actually depends on the desired accuracy on the measurements. Starting from the DNL expression, the measurement accuracy is defined as:

$$\delta\text{DNL} = \frac{1}{H_{ideal}}$$

Then, we have to choose the number of central codes on which the gain measurement is performed. Of course, the higher this number, the better the accuracy, but the higher the area overhead. So, we empirically choose to take ¼ of the total number of codes ($Z=2^{n-2}$).

To summarize, the length of the registers can be defined according to both the number of bits of the ADC and the desired accuracy on the parameters measurement:

# of one-block for DM = n

# of one-block for EM = $-\log_2(\delta\text{DNL}) + n - 2$

II.3 CONTROL UNIT

The control unit manages the test process and the calibration phase of the stimulus generator. This unit is simply defined in VHDL and then synthesized by an automatic tool such as *Ambit* of *Cadence*.

III. AUTOMATIC GENERATION OF BIST ARCHITECTURE

III.1 TEST TIME

An important point to discuss is the impact of our technique on the test time. Indeed, our technique is based on a sequential decomposition of the global test procedure, implying a high number of input test patterns to complete the test. The time decomposition permits to drastically reduce the additional circuitry, but this reduction is obviously obtained to the prejudice of the test time.

Let us evaluate the test time for a n-bit converter. This time, of course, depends on the number of required test patterns, but also on the time of the test pattern. Considering the gain measurement is chosen to be performed on ¼ of the total number of codes and neglecting the single input pattern required for the offset determination, we obtain a rough estimation of the test time as:

$$\text{TEST TIME} \approx \frac{2^{2n}}{F_s \times \partial DNL}$$

Where Fs is the sampling frequency. It clearly appears through this expression that the test time considerably increases with the number of bits (n) of the converter. However possible optimizations may be considered to reduce testing time. The first evident one consists in computing DNL and INL during the same test phase. Indeed, this permits to divide the test time by almost a factor 2 and only costs an additional register in the BIST circuitry. A second optimization of the technique consists in replacing the code-after-code process of the histogram by a p-code after p-code process for instance. Again a factor p can be gained on the test time, but of course to the detriment of the BIST area overhead.

Although we modify the level of the time decomposition, the test time remains prohibitive for high-resolution converters. Note that this problem is consistent with the limitation of the test signal generation. So, the LH-BIST should be preferred for medium-resolution converters (6 to 12 bits) that represent a large range of existing ADC.

III.2 PRINCIPLE OF THE AUTOMATIC TOOL

There is a trade-off to define between area overhead and test time. In practice, the BIST description generator evaluates the total area overhead and test time for different solutions. The algorithm synoptic shown figure 9 illustrates the successive steps of the BIST architecture generation.

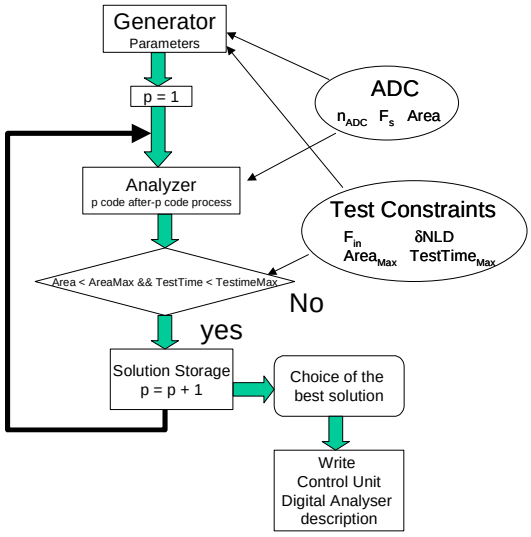

Figure 9. Building Algorithm

Firstly, the tool chooses the best kind of generator according to the ADC resolution. Then, the sizes of the different transistors and capacitors of this generator are evaluated with respect to the expected stimulus frequency. Secondly, the tool estimates the total area overhead for different time decomposition levels on the basis of the assessment of each one-bit block area (with interconnections). The tool simultaneously evaluates the test time for each configuration. If both test time and silicon area are lower than the maximal values demanded by the user, the tool stores the configuration of these BIST solutions. Then, the automatic tool generates the VHDL description of both the digital response analyzer and the control unit for the BIST solution chosen by the user.

The tool we propose has been developed in *labVIEW*. Figure 10 gives an example of its user interface.

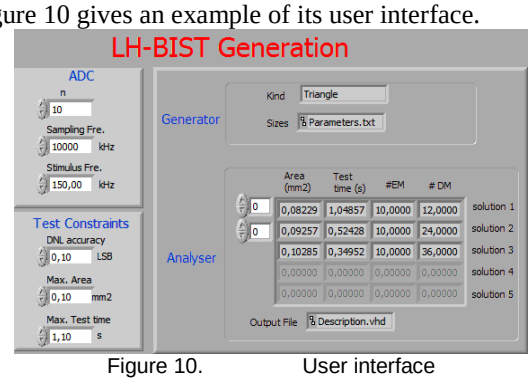

Figure 10. User interface

It also permits to specify, for a given application (ADC resolution, expected DNL accuracy, maximum test time an area overhead) the number of one-bit blocks for the EM and DM registers. Finally, the tool writes the VHDL description of the digital circuitry for the chosen BIST

solution and provides the parameters of the stimulus signal generator.

III.3 Experimental example

Let us consider the following case of an 8-bit ADC with sample frequency of 10MHz built in 0.35 AMS technology and laid on a silicon area of 1,2 mm², to be tested. We demand that test time does not exceed one tenth of second with an input signal frequency of 150kHz and the area overhead has to be smaller than ten percent of the ADC under test own area. For this realistic case study the tool gives the parameters of both the digital response analyzer and the analog signal generator, as illustrated in figure 11.

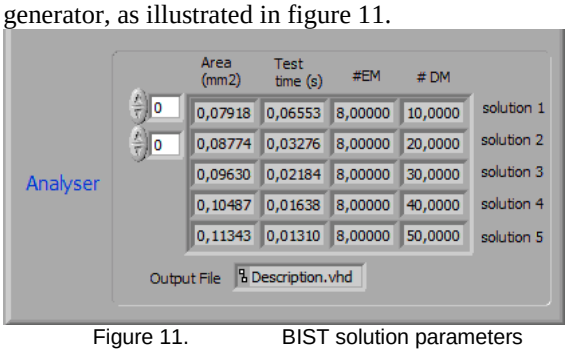

Figure 11. BIST solution parameters

For this ADC resolution we have to use a ramp signal as a stimulus. Concerning the digital response analyzer, only five solutions meet the constraints we have imposed with $p \in \{1, 2, 3, 4, 5\}$. The first solution allows one to use the minimal hardware resources whereas the last solution gives priority to the test time. Finally, we choose this last solution and the automatic tool generates the VHDL description of the digital circuitry of the BIST solution.

IV. Conclusion

We have shown that the LH-BIST architectures based on the linear histogram test technique can be configured. Thus, they can be built according to a given application (ADC under test and test conditions). We have developed a software tool allowing us to automatically generate the BIST hardware description.

In practice, the BIST description generator evaluates the total area overhead and test time. The user can choose the time decomposition level the most appropriate to his specific application. Afterwards the tool generates the VHDL descriptions of the digital response analyzer and the control unit. The tool also gives the value of all the components that constitute the analog input test signal generator.

V. References

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