An all-digital A/D converter for fast conversion with 4-TAD parallel construction using moving-average filtering

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Summary: An all-digital A/D converter (ADC) for fast conversion with 4-TAD [1] parallel construction is presented. The basic structure of the TAD is a completely digital circuit including a ring-delay-line (RDL) with delay units (DUs), along with a frequency counter, latch and encoder. The operating principles are, firstly, that the delay time of the DU is modulated by the A/D conversion voltage (Vin); and secondly, that the delay pulse passes through a number of DUs within a sampling (= integration) time, and the number of DUs through which the delay pulse passes is output as conversion data. The single-TAD area is 0.29 mm^2 (0.65-μm CMOS) with a resolution of 1 mV/LSB (1 MS/s). Also, its non-linearity is ±1% FS per 1000 mV span (1.5-2.5 V). This non-linearity error can be easily compensated for by digital processing using reference points, resulting in FS of less than ±0.1%. A resolution of 12 mV/LSB (40 MS/s) was realized with 4-parallel TAD. Sample holds are unnecessary, and a low-pass filter function [1] removes high-frequency noise simultaneously with A/D conversion. Thus, the combination of this ADC and the digital filter that follows can eliminate the need for an analog pre-filter. Moreover, this ADC can be easily downsized as process technology advances.

Keywords: ADC, moving-average, all-digital.

1. INTRODUCTION

Flash and pipeline schemes are the dominant architectures for high-speed A/D converters (ADCs) [2]-[5]. These architectures employ analog circuits such as op-amps, resistors and capacitors. However, for ease of design of the ICs and to overcome their weaknesses, analog parts should be eliminated from the ADC circuit itself. This report introduces a compact and high-speed A/D converter consisting of an all-digital circuit.

2. PRINCIPLES OF OPERATION

We conceived an original A/D conversion method involving digitization of the number of stages of a *delay unit* (DU) through which a pulse passes within a specific time. This is a revolutionary method that does have not any passive elements such as resistors or capacitors [1]. The principles are as follows. 1) The pulse delay circuit is serially connected to the DU by a primitive gate circuit in the digital circuit, wherein the delay time (Td) of the DU is modulated by the voltage Vin for A/D conversion. In this way, the Td is changed with high sensitivity. The time resolution Td is approximated by the following equation (1) [6]:

$$Td = A\,Vin / (Vin - Vth)^{\alpha} \quad : \alpha = 1.4 \text{ to } 1.6 \qquad (1)$$

where A and α are constant depending on process technology. This equation (1) means that increasing Vin shortens the Td effectively. 2) A digital value (DT) reflecting the input voltage Vin can be obtained by digitizing the number of DUs through which the pulse passes during a fixed time Ts, and outputting this number as output data DT. Since the number of stages of the delay pulse passing through the DU is dependent on the sampling frequency fs (1/Ts), the A/D conversion resolution is controllable by setting the fs using the following equation (2) [1].

$$DT = (1/fs)\{(Vin - Vth)^{\alpha} / A\,Vin\} \quad : \alpha = 1.4 \text{ to } 1.6 \qquad (2)$$

3. BASIC CIRCUIT STRUCTURE

Figure 1 shows the basic structure of the new ADC. This ADC is a completely digital circuit including a ring-delay-line (RDL) with 16 delay units (16 DUs), (DU = 2 inverters), along with a 14-bit frequency counter, latch and encoder. Data on the difference between successive data from the latches are output as 18-bit DT conversion data (this ADC is called TAD [1] for high-resolution and low-power ADC). Sample holds are unnecessary, and a low-pass filter function (defined as TAD filter effect in [1]), which consists of analog moving-average processing, removes high-frequency noise simultaneously with A/D conversion. Thus, the combination of this ADC (TAD) and the digital filter that follows can eliminate the need for an analog pre-filter to prevent the aliasing before A/D conversion.

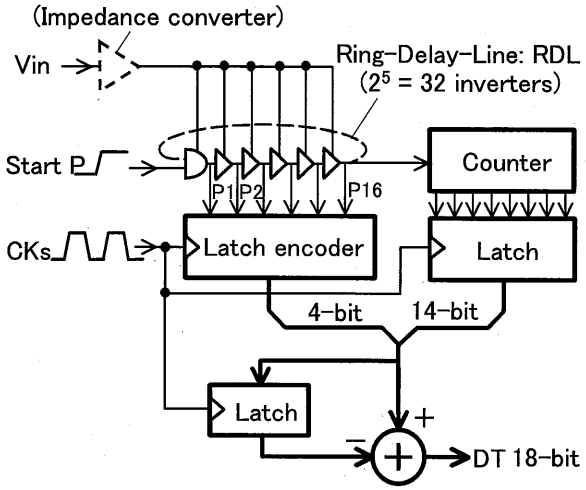

Fig. 1. Block diagram of the A/D converter (TAD).

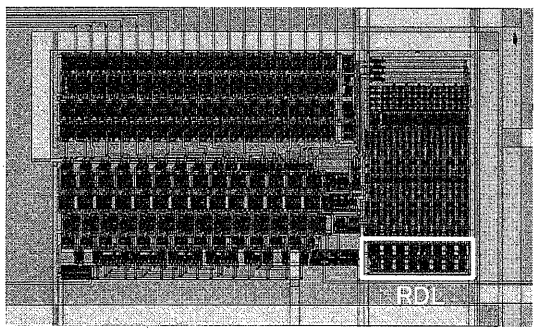

Fig. 2. Photomicrograph of TAD-IC chip (0.72 mm x 0.40 mm: 0.65-μm CMOS).

An individual TAD was realized with an ADC having a circuit area of 0.29 mm^2 (0.65-μm CMOS), as shown in Fig. 2. The small-framed area is the RDL consisting of 16 DUs. Since there are few delay units, the area voltage-modulated by the input voltage Vin can be extremely small, to closely match the mutual characteristics of the DUs. Finally, an original architecture for the TAD was made possible by applying a circuit system [7]-[9] devised to allow stable reading of the frequency of an RDL operating at high speed.

4. 1-TAD EVALUATION RESULT

A/D conversion characteristics with a single TAD at a sampling frequency fs = 1 MHz (25℃) are shown in Fig. 3. Approximately 315 to 1315 digital values correspond to the voltage change in an AD conversion range of 1.5 to 2.5 V of an input voltage span of 1000 mV, with the change component being 1000. Accordingly, the voltage resolution (Vd) is around 10-bit at approximately 1 mV/LSB. Non-linearity is ±1% FS per 1000 mV. However, non-linearity errors can be easily compensated

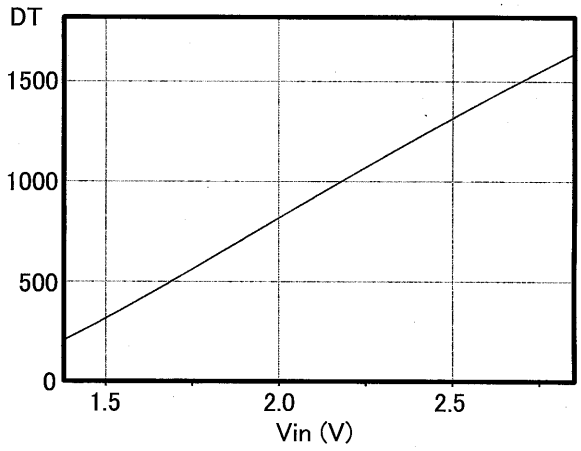

Fig. 3. Characteristics of single TAD A/D conversion (Vin range = 1.4-2.8 V, 25 °C): Sampling frequency fs = 1 MHz.

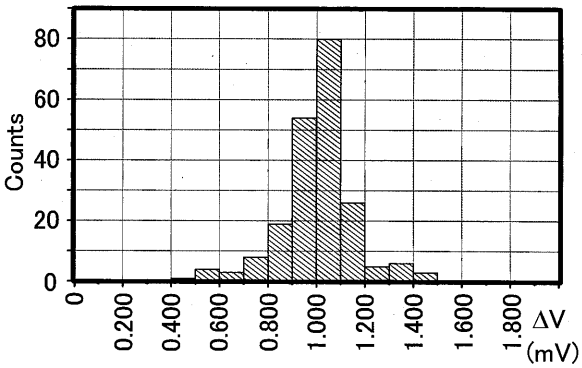

Fig. 4. Histogram of the dispersion of the resolution Vd; that is, the differential voltage ΔV between the code-to-code variation with noise (including RDL jitter, bias line and ground line noise) at a sampling frequency = 1 MHz.

for by digital processing using reference points (see Section 6). Fig. 4 shows the dispersion of the resolution Vd at the same sampling frequency. The Vd average is 0.99 mV/LSB, and the σ of the distribution is 0.15 mV for the Vin range 2.000-2.200 V (n = 200).

Resolution density drift was approximately -20%, +40% against 25 ℃ changes in a temperature range of -35~140°C [10], but this can be resolved by digital calculation correction to obtain the ratio to a reference value [10], [11]. Although resolution may be somewhat imprecise at high temperatures, the TAD is still applicable at high temperatures, with stable operation up to 140°C, since it does not require an analog circuit [10].

5. 4-PARALLEL TAD EVALUATION RESULT

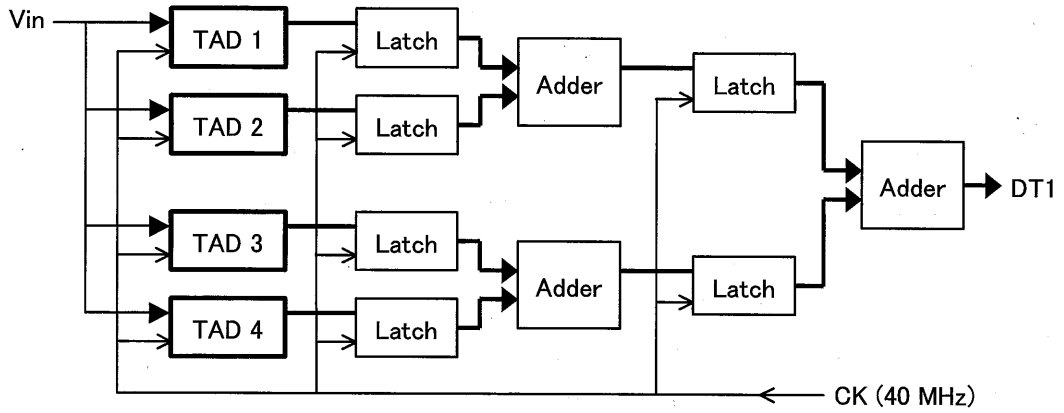

Fig. 5. Block diagram of the A/D converter board (4-TAD parallel construction).

Figure 5 shows a test board construction applying 4 parallel TADs. In the present study the test board uses 4 single TADs (48-pin DIL package) and standard logic ICs. A 40 MHz sampling clock was input from CG. A logic analyzer reads output data (DT1) from the test board. Each RDL in the TADs has some respective jitter (Fig. 4), so that a dither effect can be obtained using only a digital averaging filter with off-line processing.

This 4-parallel onboard TAD achieved a resolution of 12 mV/LSB (40 MS/s). Figure 6(a) (next page) shows the input signal for the test board, which is like a saw-tooth blade waveform at 40 kHz with high-frequency noise. A/D conversion data (DT1) before digital filtering are shown in Fig. 6(b), and the TAD filter effect obviously reduces high-frequency noise. Finally, noise-removed A/D conversion data (DT2) with 8-data moving-average filtering are shown in Fig. 6(c). The non-linearity is ±0.7% FS per 600 mV span (2.2-2.8 V), for 6-bit resolution. The theory of the TAD filter effect (analog moving average) is described in [1].

6. DISCUSSION

Since this fast ADC architecture can be made with an all-digital circuit, advances in process technology will lead to both shorter Td and easier parallel A/D processing of numerous TADs. These effects will enable faster and faster sampling-rates. A high degree of Ts reproducibility is required (minimal clock jitter), but this does not pose a problem if a typical quartz resonator clock is used. In addition, the dither effect will be unnecessary if the 4 TADs have an offset value of (1/4) LSB with respect to one another by modifying their respective resolutions.

Although the TAD has a non-linearity error for Vin, this is not difficult to correct by applying digital calculation processing, because its behavior can be predicted with the approximation equation (2). One correction method is shown in Fig. 7 using multi-straight-line approximation with three reference values (Vr1, Vr2, Vr3). Another is parabolic approximation with three references. Table I shows TAD integral non-linearity error and simulated correction results to equation (2).

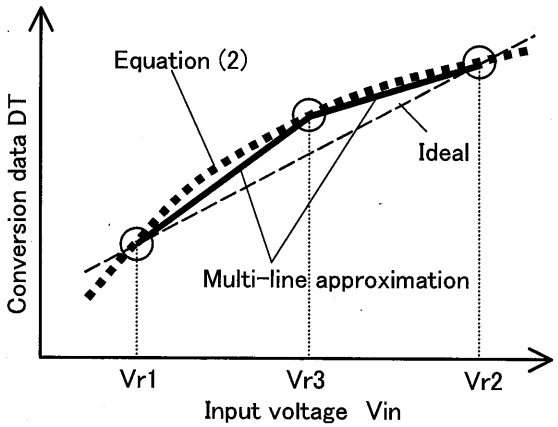

Fig. 7. One method of correcting non-linearity.

Table I. Non-linearity error with correction (%FS)

	Vin span	Vin center voltage (V)		
		1.8	2.0	2.5
Non-correction	400 mV	±0.253	±0.360	±0.414
	1000 mV	–	–	±1.022
Multi-line Approxi-mation	400 mV	±0.080	±0.096	±0.105
	1000 mV	–	–	±0.264
Parabolic Approxi-mation	400 mV	±0.044	±0.022	±0.006
	1000 mV	–	–	±0.041

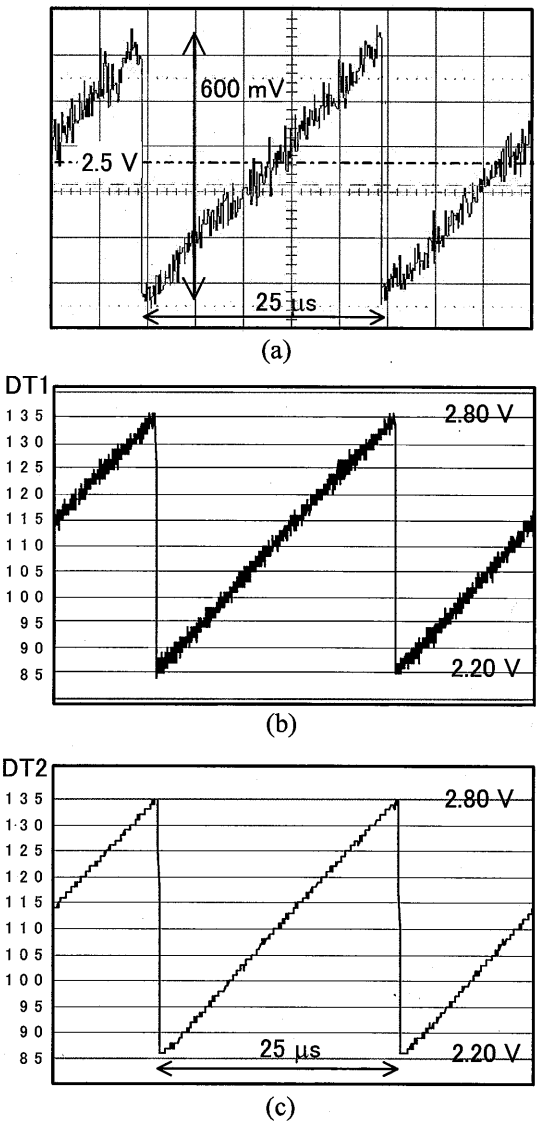

Fig. 6. Characteristics of A/D conversion with 4-TAD parallel construction (sampling frequency: 40 MHz): (a) Input signal (saw-tooth blade waveform with noise). (b) A/D conversion result of 2.2-2.8V by 4-TAD. (c) A/D conversion result with 8-data moving-average filtering.

7. CONCLUSION

In moving toward very fast ADC, advances in process technology and parallel A/D processing of multiple TADs (numerous TADs) will enable faster and faster sampling-rates. It should also be mentioned that this all-digital ADC (TAD) can be shrunk and operated at low voltage, so it is an ideal means to lower cost and power consumption, and ease IC-design. Drift errors [1] and non-linearity error can be easily compensated with the use of digital processing.

8. REFERENCES

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