Novel Calibration Method for a 16-bit 1.5 Megasamples/s Successive Approximation ADC with Non-binary Capacitor Array

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Abstract - A novel calibration method for successive approximation analog-to-digital converter with non-binary capacitor array is presented. It takes advantage of the redundancy in the radix less than 2 non-binary capacitor array and the adaptive calibration algorithm. The capacitor weights are adaptively calibrated to accurately reflect the actual capacitance ratios in the fabricated capacitor array even without good capacitor matching. The capacitor weights are calibrated to better than 22-bit accuracy. The matching requirement in the capacitor array is greatly relaxed. The method is used to design a 16-bit, 1.5 megasamples/s successive approximation analog-to-digital converter.

Keywords - Analog-to-Digital Converter, ADC Calibration, Successive Approximation, Non-binary Capacitor Array.

I. NATURE OF THE PROBLEM

The fabrication technology in sub-micron and nanometer era advances the high performance digital circuitry tremendously, but it becomes more and more difficult to build high performance analog circuitry using the same technology. New architecture must be devised to design high performance analog and mixed signal circuitry. Modern applications in communications and process control require high-accuracy, high-speed Analog-to-Digital Converters (ADC).

Successive approximation register (SAR) converters offer the combination of resolution and speed unmatched by delta-sigma, pipeline or flash ADCs. SAR's have no latency, and can be multiplexed. Furthermore, the power consumption is relatively low. These features make SAR converters a good choice for data acquisition and communications applications.

Calibration is often used to increase the resolution of the ADC. How to take advantage of the huge potential of digital calibration circuitry to relax the requirement on analog circuitry becomes a vital problem.

II. CALIBRATION: STATE OF THE ART

A conventional capacitor based charge redistribution successive approximation ADC uses a binary-weighted capacitor array and a comparator as the internal DAC. The advantage of the binary-weighted DAC is that the back-end digital complexity is low. An accuracy of 10 bits can be easily achieved with straightforward design techniques using capacitor based charge redistribution converters because capacitor matching better than 0.1% is common. However, building a binary weighted DAC with greater than 16-bit accuracy is not trivial. Every decision in the converting steps is critical and affects the final accuracy. In order to get better than 10 bits accuracy in charge-redistribution DAC, production laser trimming or other calibration methods are used to guarantee tight capacitor matching. The production laser trimming is expensive. The accuracy of many calibration methods is usually limited to the size of the smallest capacitor. Increasing the size of the smallest capacitor can improve the accuracy but it will slow down the conversion speed. ADCs with greater than 16-bit accuracy and greater than 1 megasamples per second sampling rates are still hard to build.

III. NOVEL CALIBRATION METHOD BASED ON NON-BINARY CAPACITOR ARRAY

A 10-bit, 20 megasamples/s, non-binary SAR ADC was reported in 2002 International Solid-State Circuits Conference [1]. A 16-by-16 uniform capacitor array was used for the upper 8 bits. The redundancy was not in the DAC, but was calculated in the digital part of the converter. The capacitor matching in the capacitor array was still the limiting factor for higher accuracy.

Instead of matching the physical capacitors themselves to get a precise radix 2 capacitor array, we take a different approach. We build the capacitor array and adaptively adjust the digital representation of the capacitor: capacitor weights to match the fabricated capacitor array. In our 16-

bit, 1.5 megasamples/s SAR ADC based on non-binary capacitor array, we take advantage of the redundancy in the non-binary capacitor array and the adaptive calibration algorithm to greatly relax the capacitor matching requirement. A radix less than 2 capacitor array in the charge-redistribution SAR converter creates redundancy. For a capacitor array with N capacitors and radix R, the capacitor weight of capacitor j is $W(j) = A \times R^j$ where $j = 0,1,\cdots,N-1$ and A is the capacitor weight for the smallest capacitor in the array. The redundancy for capacitor j is defined as:

$$redundancy(j) = \left(\frac{\sum_{k=0}^{j-1} W(k)}{W(j)} - 1 \right) \times 100\%$$

where $j = 1,2,\cdots,N-1$. Based on simulation results, radix 1.8 is a good choice. The exact radix is not critical and will be calibrated out.

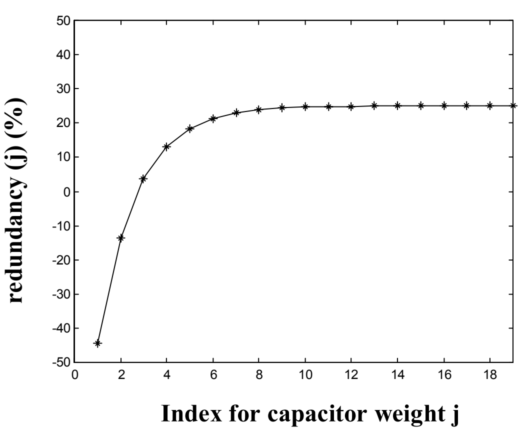

Fig. 1. The redundancy in an array with R = 1.8.

The redundancy in a capacitor array with 20 capacitor and radix $R = 1.8$ is shown in Figure 1. There is no redundancy for capacitor 0, 1, 2 since the corresponding redundancy values for them are less than zero. The redundancy approaches 25% for larger capacitors in the array. Larger error will be tolerated for early decisions in the successive approximation process since the redundancy is larger.

The non-binary capacitor array is shown in Figure 2. The ratio between adjacent capacitors is approximately 1.8 which means that R=1.8. In order to get 16-bit resolution, the largest capacitor in the array should be great than C*2^16. We need 20 capacitors in the capacitor array. The top plates of all the capacitors are connected to the input of the comparator. The bottom plate of each capacitor can be switched to the analog input Vin, the reference voltage Vref or the signal ground Sgnd. The comparator output SARout is the decision of each successive approximation step during conversion.

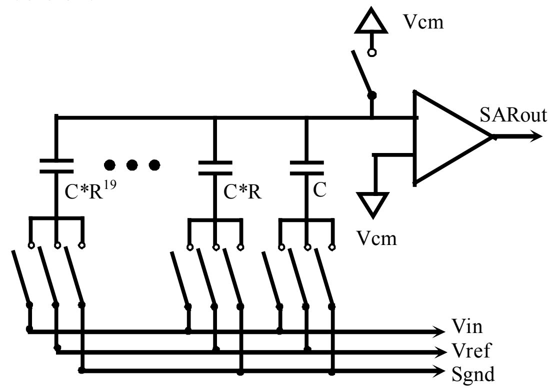

Fig. 2. A non-binary capacitor array based DAC.

The capacitor calibration algorithm is based on a perceptron learning rule [2] that was originally developed for Artificial Intelligence applications. The calibration algorithm works as follows:

(1) Sample the reference voltage using a random vector $\{A(j)\}$. The bottom plate of capacitor j is switched to the reference voltage Vref if $A(j) = 1$. The bottom plate of capacitor j is switched to the signal ground Sgnd if $A(j) = 0$. We can use a linear feedback register (LFSR) to generate this random vector. This will create a charge on the top plate of the array. We use this mechanism to generate a random yet precise analog test voltage as the input to the ADC. Add the corresponding capacitance weights and offset W_{off} to get a digital result D_a.

$$D_a = W_{off} + \sum_j A(j) \times W(j)$$

(2) Perform successive approximation starting from the largest capacitor. After 20 cycles, we can get a result in the SAR register $\{B(j)\}$. $A(j)$ and $B(j)$ may not be the same due to the redundancy and the noise in the system. Add the corresponding capacitor weights to get D_b. D_a and D_b may be different because of the redundancy and the noise in the system.

$$D_b = \sum_j B(j) \times W(j)$$

(3) After the SAR conversion process, we get the sign of the residual analog voltage on the top plate of the array: S_a by checking the comparator output at the end of SAR process. We may check the comparator output multiple times and take the average to reduce the effect of noise. We can also get the sign of D_a minus D_b which is the digital sign: S_d.

$$S_d = D_a - D_b$$

(4) We have a learning case if the analog sign and digital sign do not equal. Although the noise may corrupt the analog sign, the analog sign closely reflects the real result. The digital sign may be wrong because the capacitor weights do not reflect the corresponding capacitance before we finish the calibration. We need change the capacitor weights to the right direction. We can correct the capacitance weights according to the perceptron learning rule:

$$W(j) \leftarrow W(j) + \alpha \times [A(j) - B(j)](S_a - S_d)$$

$$W_{off} \leftarrow W_{off} + \alpha \times (S_a - S_d)$$

where α is called the learning rate. *A(j)* and *B(j)* may not be the same due to the redundancy and the noise in the system. This is essential to the algorithm. Otherwise, nothing can be learned from the process.

(5) Loop through step 1 to 4 for a predetermined number of times or until there is no significant improvement, then change α to a smaller value.

(6) Loop through step 1 to 5 until α is smaller than the accuracy level we want.

It has been proven that the weight space has no local minimum [2]. If the learning rate is not so large to cause overshooting and the learning cases represent linearly separable function, the algorithm will converge to the correct weights. If we calibrate long enough, we can calibrate the capacitor weights to an accuracy level better than the noise level in the system because of the averaging effect in the calibration process.

This algorithm calibrates the capacitor weights so that the matching requirement on the physical capacitor array is no longer a limiting factor. Essentially, the complexity is moved from the analog domain to the digital domain. The same philosophy is used in delta-sigma converter where the analog circuitry is simplified and complicated filtering is moved to the digital domain.

Non-binary capacitor array based DAC is more forgiving due to the redundancy. The errors made in the early steps of the successive approximation conversion process can be corrected in later steps. Due to the relaxed requirement on capacitor matching, total capacitance of the capacitance array can be smaller. The DAC can run faster with smaller total capacitance. The capacitor weights are calibrated with high accuracy. This calibration algorithm is very important for implementing high speed and high accuracy analog-to-digital converters.

The block diagram of the ADC is shown in Figure 3. It uses a mixed-signal micro-controller architecture [3] with a unified control structure. There are separate decoding blocks for the analog and digital datapaths to generate the control signals for the respective blocks. It provides centralized control for the analog and digital circuitry. This allows a unified programming model for implementing the capacitor array calibration algorithm, writing the normal SAR conversion process in micro-code, and interfacing to external peripherals.

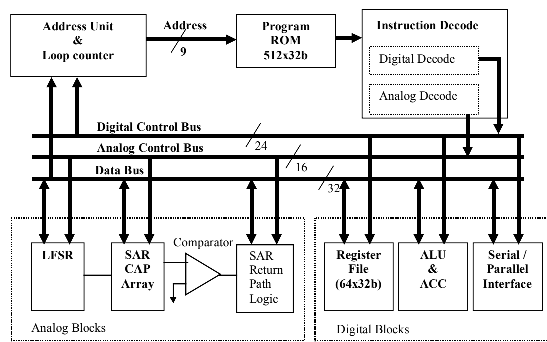

Fig. 3. The block diagram of the ADC.

The analog blocks in the SAR converter include a 20-bit linear feedback shift register (LFSR) to generate *A(j)*, a non-binary capacitor array, a comparator and SAR return path logic. The random vector generated by the LFSR is used to control the bottom plate connection of the capacitor array during the sampling phase. The capacitor is connected to the reference voltage Vref if the corresponding bit in LFSR is 1. The capacitor is connected to the signal ground Sgnd if the corresponding bit in LFSR is 0.

This system provides the infrastructure to implement the calibration algorithm as the instructions running on the mixed-signal micro-controller.

IV. RESULTS AND CONCLUSIONS

We design a 16-bit, 1.5 megasamples/s successive approximation A/D converter using the non-binary capacitor array. We implement the capacitor array calibration algorithm based on the perceptron learning rule. The simulation is done in Verilog. The thermal noise voltage is 19.9 μV. The comparator noise voltage is 9.9 μV. The reference voltage is 2.5 V. The offset is assumed to be 10 mV. We demonstrate through extensive simulation that 20 capacitor weights and one offset converge to the correct values. The accuracy of the capacitor weights is calculated from the statistics of the end results of calibrations. We represent the calibration accuracy in terms of the equivalent accuracy level in bits. It is calculated as in the following equation:

$$accuracy(j) = \log_2 \frac{W_{total}}{\sigma(j)}$$

where $\sigma(j)$ is the standard deviation of capacitor weight j, W_{total} is the sum of total capacitor weights. The accuracy of the capacitor weights after an exemplary calibration process is shown in Figure 4. We can see that the capacitor weights are calibrated with better than 22-bit accuracy. The capacitor weights are calibrated with better than 22-bit accuracy consistently under many different conditions.

Assume that the worst root mean square (RMS) error of the capacitor weights equals σ after calibration. The worst case RMS error in the conversion result due to capacitor weight errors is $\sqrt{20}\sigma$ for 20 capacitors. We check the 6-sigma error:

$$6\sqrt{20}\sigma \leq 2^{-16} \quad \text{for} \quad \sigma < 2^{-21}$$

So it is easy to get 16-bit accuracy for the ADC with weights of better than 22-bit accuracy capacitor.

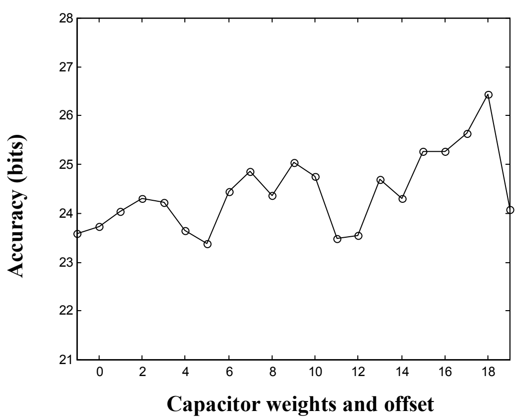

Fig. 4. Calibration accuracy of the weights.

The simulated ADC output spectrum after the calibration for an input sine wave of -60 dB, 150 kHz is shown in Figure 5. This shows the effectiveness and the robustness of the calibration method. The calibration time is about 50ms.

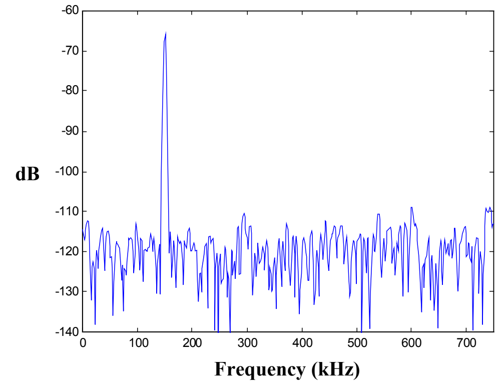

Fig. 5. The ADC output spectrum for –60dB input.

This calibration method is essential to the design of high speed and high resolution ADC.

With 22-bit accuracy for the calibrated capacitor weights, we can potentially get even higher resolution with the same architecture. The limiting factor is the noise in the circuit. Capacitor matching is no longer a limiting factor. There is a trade-off between speed and noise level. We can use larger capacitance in the array if we want to lower the noise level. Larger capacitance will slow down the conversion. Smaller radix will give us more redundancy and will be more forgiving for initial incorrect decisions but it will require more capacitors in the array and longer time for conversion.

We can use the same architecture to get even higher accuracy. This algorithm may also be used to calibrate other analog circuits such as pipeline ADC and relax the matching requirement, which is even more important as we use smaller geometry processes.

References

[1] F. Kuttner, "A 1.2V 10b 20Msamples/s Non-Binary Successive Approximation ADC in 0.13um CMOS", *2002 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp.176-177, Feb. 2002.

[2] S. Russell and P. Norvig, *Artificial Intelligence: A Modern Approach*, Prentice Hall, 1995, Chapter 19, pp.573-578.

[3] J. Gan, J. Page and J. Abraham, "Mixed-Signal Micro-Controller for Non-Binary Capacitor Array Calibration in Data Converter", *Proceedings of 36th Asilomar Conference on Signals, Systems and Computers*, pp.1046-1049, Nov. 3-6, 2002.