An Accurate ADC Model in Radar System Simulation

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Abstract ***– To show the usefulness of performing system simulations with an accurate ADC model, some simulations of a radar receiver are presented. The accurate model gives very different results than simple characterization with SNR and SFDR. System performance varies quite much for ADCs with the same specified performance in terms of SNR or SFDR depending on which error mechanism is active in the ADC. With this detailed knowledge of how the ADC affects system performance, the ADC requirement margin can be reduced thus saving cost and power consumption.***

Keywords ***– ADC, modeling***

1. INTRODUCTION

Modern design methods are based on early system modeling and simulation. Analog-to-digital converters (ADCs) are normally described as a simple quantizer with a given number of bits (NOB), which translates to a certain signal-to-noise ratio (SNR). However, ADCs normally have more errors than the simple quantization error so a more accurate modeling may be useful [1], [2], [3]. An important outcome from simulations with a more accurate model is that the performance requirement margin of the ADC can be minimized, thus saving cost and power consumption. Accurate models have previously been shown to be useful for DSL applications [4].

In this work, the usefulness of an accurate ADC model in system simulation is investigated by studying the effects of various ADC errors on the system performance of a radar receiver. A comparison is made with simple ADC characterization with SNR and spurious-free dynamic range (SFDR). An accurate ADC model, written in embedded MATLAB code [5], was included in Agilent ADS system simulator. A complete Frequency Modulated Continuous Wave (FMCW) radar receiver chain including RF frontend, ADC, digital filters, and post processing was implemented in the system simulator. The models are described in section 2 and the simulation results presented in section 3 followed by conclusions in section 4.

2. MODEL DESCRIPTIONS

2.1 Radar Model

In an FMCW radar, phase and Doppler shifts are used to find the range to and speed of a target [6]. Depending on the range to the target, the input signal to the radar receiver can vary very much in power. A detection threshold is set and any signal above that is recognized as a target. Hence, all harmonics have to be lower than the detection threshold or false targets will appear. Possible multiple input signals with large power differences set tough requirements on the radar receiver. To be able to detect weak targets, the detection threshold has to be set low, which requires spurious peaks originating from strong targets to be even lower. Apart from harmonic distortion, strong targets will also mix with other signals and harmonics creating strong spurious peaks. A relevant measure of system performance for this type of radar is the amplitude difference between a weak target and the largest spurious peak. This can be defined as system level SFDR. It is then assumed that the noise level always is lower than the spurious peaks, which was true for all the cases studied in this work.

The radar receiver is modeled in three blocks as shown in figure 1. The RF block contains predefined ADS components such as filters, amplifiers, and a mixer as shown in figure 2. There are a number of advanced parameters to specify the components, but it can also be made fairly simple by using default values. Filters are

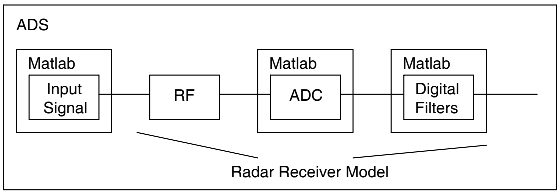

Figure 1. Radar model block diagram.

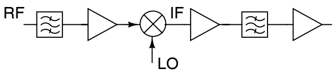

Figure 2. Radar receiver RF part.

characterized with cut-off frequencies, pass band gain, and stop band attenuation, the amplifiers with gain and noise figure, and the mixer with LO and RF rejections, conversion gain, and noise figure. The ADC and digital filters blocks were implemented in MATLAB. MATLAB was also used to generate input signals and for processing output signals. The ADC model is described in the next section.

2.2 ADC Model

A MATLAB-based time-domain model of a subranging successive-approximation ADC that uses binary search has been developed [5], [7]. The main objective was to model all performance limiting errors as realistically as possible. This was done by identifying the main resistances and capacitances in the sampling frontend of a real ADC [8] and considering these an RC network to which the signals are applied. A block diagram of the model is shown in figure 3. Three subranges are used: C (Coarse), M (Middle), and F (Fine). The input is sampled and then, for each iteration in the binary search, resistor ladders are used to generate a reference voltage, V_R, to compare to the sampled voltage, V_S. Figure 4 shows the equivalent circuit for the contribution from the coarse subrange, $V_{R,C}$. The resistances come from the on-resistance of the MOS switches and the capacitances from the sampling capacitors.

In the simulations, the effect of three different error mechanisms will be investigated. The first is static mismatch in the resistor ladders, which causes spread in the generated reference voltages. It is modeled as a Gaussian random number added to the resistance values as

$$R = R_0(1 + \sigma_R x),$$

where R_0 is the nominal resistance and x a Gaussian random number with the standard deviation $\sigma_x = 1$. The error is varied by changing the relative standard

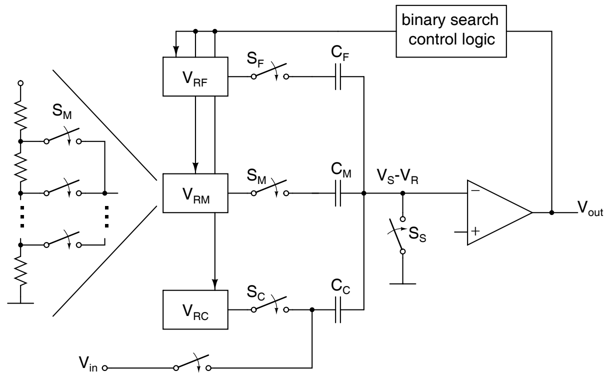

Figure 3. ADC model block diagram.

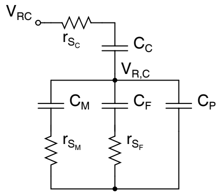

Figure 4. ADC model equivalent RC network.

deviation of the resistance, $R_0\sigma_R$. The second error is comparator recover time, i.e. the time it takes for the comparator to change an initially wrong decision. This is modeled as a constant time loss that limits the time available for settling. The available time for settling is calculated as

$$t = \frac{1}{2f_c} - t_k,$$

where f_c is the clock frequency and t_k is the constant time loss. The error is varied by changing t_k, which has shown to be an important parameter for modeling dynamic errors in SA-ADCs [5]. The third error is NOB. Then, the simulations are equivalent to using a simple ADC model, which only includes ideal quantization and clipping.

3. SIMULATIONS

3.1 Simulation Setup

The radar uses a 10 GHz RF frequency, which is mixed down to an IF of 360 MHz in the receiver. This is then sampled with 160 MHz. To fulfil the ADC requirements, 16 parallel 12-bit cells, each with a sampling frequency of 10 MHz are used, giving a total sampling frequency of 160 MHz. The sweep bandwidth is 150 MHz, the modulation time 3.2 µm, and the number of repeated pulses 40. This gives a range resolution of 1 m and a speed resolution of 117 m/s. The speed resolution is quite low, since increasing it means a significantly longer simulation time.

The test case is a short-range missile detection system. It includes two targets. Target 1, the target of interest, is a weak target at 19 m range moving at a speed of 798 m/s and gives an input signal power of -35 dBm. Target 2 is a strong interfering target at 42 m range moving at 1178 m/s and giving the input signal power -15 dBm. When measuring the system performance, target 2 is removed completely and radar SFDR is measured from the peak of target 1 to the highest spurious peak.

3.2 Simulation Results

A two-dimensional plot of the radar image is shown in figure 5. It is obtained using a standard method that, among other things, involves performing FFTs on the output signal. Since, however, all frequencies used in the FFTs are not used in the system, it is only relevant to look for targets in the lower part of the figure.

To investigate how a certain ADC error affects the system performance, a number of simulations were run for different values of the different errors. Figure 6 shows how radar performance varies as a function of the different errors. Since the curve for resistor ladder mismatch varies quite much depending on the outcome of the statistic variable, the trend is also shown with stars representing a moving average over 7 points. Simulations like these are very useful to find suitable requirements for an ADC in a system.

The ADC is also simulated in single-tone tests to represent a typical characterization. The results are shown in figure 7. A sine wave is used as an input and the SNR is calculated by performing an FFT on the output. To avoid clipping, the input amplitude is set to 90% of full swing. With these tests, the ADC SNR as a function of error amplitude is determined for each error mechanism.

To investigate how the error type affects the radar performance for a certain ADC SNR, the radar SFDR is plotted as a function ADC SNR in figure 8. This plot is obtained by finding the equivalent error amplitude for a certain ADC SNR from the single-tone test and combining it with the radar SFDR that corresponds to that error amplitude in the radar simulation. Again, for visibility, the mismatch curve is, presented as a moving average over 7 points. It is clear that ADC SNR is not a suitable performance measure, since radar performance differ >10 dB depending on error type. Equivalently, the requirement on ADC SNR can differ >20 dB for a certain radar SFDR.

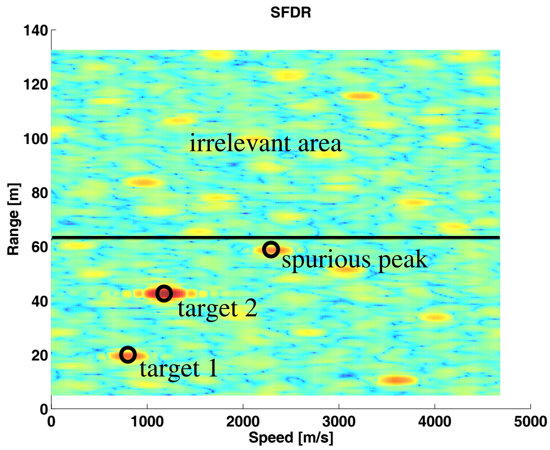

Figure 5. Radar image vs. range and speed.

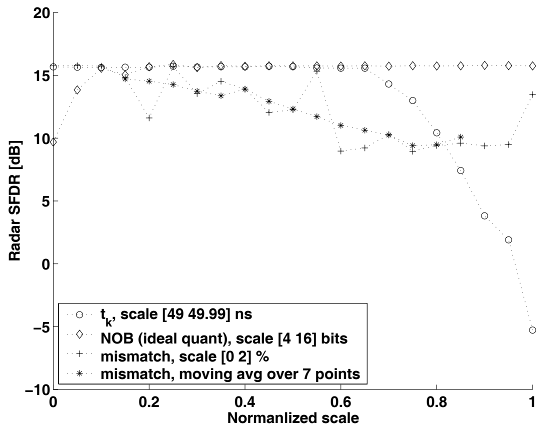

Figure 6. Radar performance vs. errors.

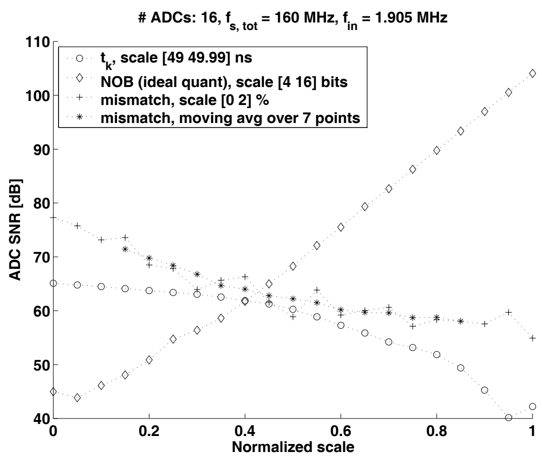

Figure 7. ADC performance vs. errors.

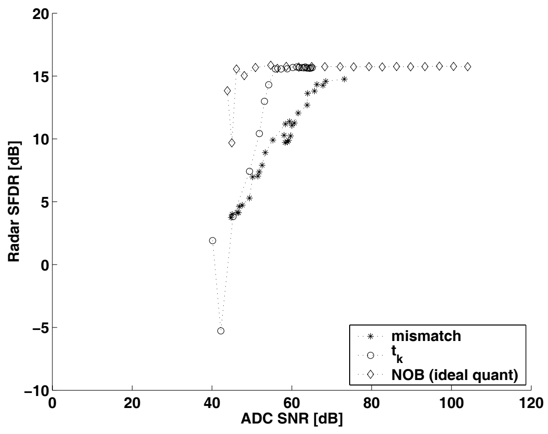

Figure 8. Comparison of error effects.

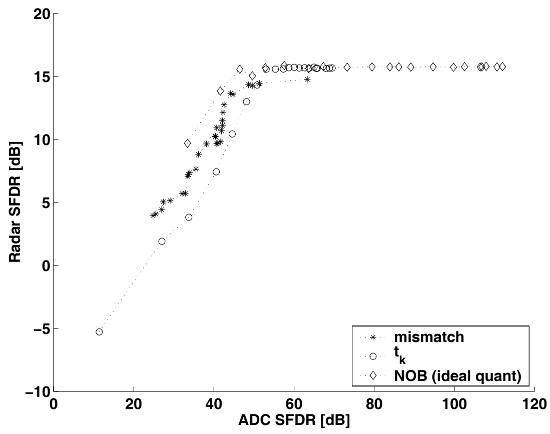

Figure 9. Comparison of error effects.

Figure 9 shows the same simulations as figure 8, but with SFDR used as a measure of ADC performance instead of SNR. Since radar SFDR is the performance limiting factor of the system, ADC SFDR is, of course, a better measure than SNR, but even here system performance and ADC requirement can differ up to 6 and 10 dB respectively depending on error the type.

4. CONCLUSIONS

A successful combination of an accurate ADC model and a radar receiver system implemented in Agilent ADS simulation framework has been demonstrated. It has also been shown how this model can be used to predict the effects of various ADC errors on the radar system performance.

For the actual radar system, where system SFDR is the limiting factor, it was shown that ADC SNR, or the corresponding NOB, is not a suitable measure of ADC performance. The requirement of the ADC for a given system performance can vary up to 20 dB depending on which error mechanism dominates in the ADC. As expected, ADC SFDR is a better measure, but still the ADC requirement can differ up to 10 dB. For these reasons, an accurate ADC model of the type presented here should replace the simple quantizer model in radar system simulation.

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