Asynchronous ADCs: Design Methodology and Case Study

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Abstract - We present a new class of Analog-to-Digital Converters (ADCs), based on an irregular sampling of the analog signal, and an asynchronous design. Because these ADCs are not conventional, a design methodology is also presented. It determines their characteristics given the required Effective Number of Bits and the properties of the analog signal to convert. A prototype has been designed for speech applications, using the 0.18-µm CMOS technology from STMicroelectronics. Electrical simulations prove that the Figure of Merit (FoM) is increased by more than one order of magnitude compared to synchronous Nyquist ADCs.

Keywords - Level-crossing sampling, Asynchronous design, Figure of Merit (FoM).

I. Introduction

It is well known that asynchronous designs exhibit interesting properties [1]. This kind of design has been used in a few publications to improve the performances of Nyquist ADCs such as: immunity to metastable behaviour [2], reduction of the electromagnetic interferences [3], speed [4], power consumption savings [5] ...

Moreover, most of the systems using ADCs bring signals with interesting statistical properties into operation, but Nyquist signal processing architectures do not take advantage of them. Actually, these signals (such as temperature sensors, pressure sensors, electro-cardiograms, speech signals...) are almost always constant and may vary significantly only during brief moments. Thus, classical regular sampling and converting systems are highly constrained, due to the Shannon theory, which is to ensure for the sampling frequency to be at least twice the input signal frequency bandwidth. Therefore, in the time domain, this condition can be translated as a large number of samples without any relevant information. This effect implies a useless increase of activity of the circuit compared to the supplied output digital information relevance, and so a useless increase of the power dissipation. It has been proved in [6] and [7] that ADCs using a non equi-repartition of the samples in time leads to interesting power savings compared to Nyquist ADCs.

The new class of ADCs proposed in this paper consists in using both the "level-crossing" sampling scheme proposed in [6] and an asynchronous implementation of the circuit (no global clock). The theory and the design of such converters is completely different from classical Nyquist ADCs. Hence a complete design methodology is presented, in order to minimize activity, power consumption, and hardware of the circuit, according to the statistical properties of the analog signal to convert, and the Signal-to-Noise Ration (SNR) of the targeted application.

After an introduction on the irregular sampling scheme and the SNR theory, the new contributions of this work are presented in Section II. A design methodology is presented in Section III so as to design such converters. Section IV describes the design and electrical simulations of an asynchronous ADC targeted for speech signals. Figure of Merit, and comparisons of signal processing chains are discussed in Section V. Lastly, Section VI concludes the paper.

II. Principles and architecture

II.1 Irregular sampling

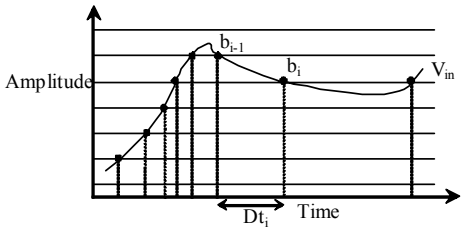

Figure 1: Irregular sampling.

For irregular sampling (cf. Figure 1), and a *M-bit* resolution, 2^M*-1* quantization levels are regularly disposed along the amplitude range of the signal. A sample is taken only when the analog input signal V_{in} crosses one of them. Contrary to classical Nyquist sampling, samples are not regularly spaced out in time, because it depends on the signal variations. Thus, together with the value of the sample b_i, the time Dt_i elapsed since the previous sample b_{i-1} must be recorded. A local timer of period T_C is dedicated to this task. The amplitude of the sample is precise, but the time elapsed since the previous sample is quantized according to the precision T_C of the timer. After computation, the Signal-to-Noise Ratio (SNR) is defined by:

$$SNR_{dB}=10.log\left(\frac{3.P(V_{in})}{P\left(\frac{dV_{in}}{dt}\right)}\right)+20.log\left(\frac{1}{T_C}\right) \quad (1)$$

. The first term of Eq. (1) is only determined by the statistical properties of the input signal V_{in}. The SNR depends on the timer period T_C, and not on the number of quantization levels. Thus, for a given implementation of the irregular sampling A/D converter

(a fixed number of quantization levels: 2^M-*1*), the SNR can be externally tuned by changing the period T_C of the timer. For example, if the SNR has to be improved by *6,02dB* i.e. must have one more bit of effective resolution (or *ENOB* – Equivalent Number Of Bit), T_C has to be divided by 2. Eq. (1) can be used to determine the theoretical SNR of a pure sine wave, a speech signal, an audio signal... In theory, for irregular sampling, the SNR can be improved as far as it is needed, by reducing T_C. The limit is the accuracy of the analog blocks: they determine the precision of the quantization levels position in Figure 1.

II.2 Asynchronous ADC

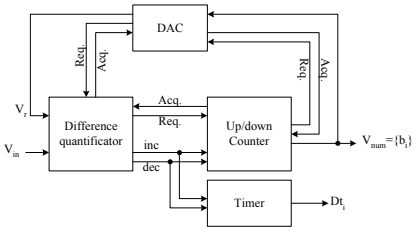

Figure 2: Block diagram of the A-ADC.

The block diagram of the architecture bringing this sampling scheme into operation is shown in Figure 2. The converter resolution M and its dynamic range ΔV_{in} set the quantification step : $q=\frac{\Delta V_{in}}{2^M-1}$ (2). The output digital value V_{num} is converted to V_r by the DAC, and compared to V_{in}. If the difference is greater than $\frac{1}{2}.q$, the state variable is incremented (*inc='1'*), if it is lower than $-\frac{1}{2}.q$, it is decremented (*dec='1'*). In all other cases, nothing is done (*inc=dec='0'*): the converter output signal V_{num} remains constant, there is no activity. The output signal is composed of couples (b_i, Dt_i) where b_i is the digital value of the sample (with $V_{num}=\{b_i\}_{i\in N}$), and Dt_i the time elapsed since the previous converted sample b_{i-1}, given by the timer. The term A-ADC for "Asynchronous ADC" is now used. Information transfer is locally managed with a bi-directional control signalling. Each "data" signal is associated with two "control" signals: a request and an acknowledgement [1]. Let δ be the total delay of the loop, the slope of V_{in} must verify the "tracking condition": $\left|\frac{dV_{in}}{dt}\right| \leq \frac{q}{\delta}$ (3).

II.3 Implementation of the A-ADC

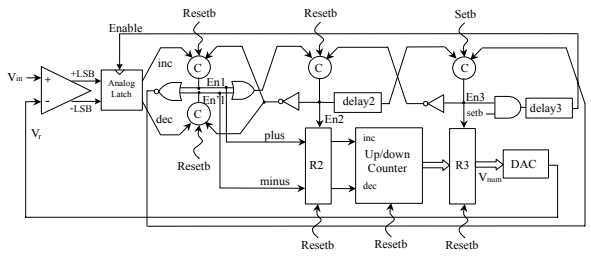

Figure 3 : Implementation of the A-ADC.

The A-ADC presented in Figure 2 has been implemented with a three stage micro-pipelined architecture [8], and a 4-phase protocol [1] (cf. Figure 3). It is composed of two parts: a quasi delay-insensitive control part composed of delays, Muller gates (or C-elements [9]) and standard gates, and a data path part composed in our case of digital and analog blocks. The delay element *delay2* (resp. *delay3*) is matching the counter critical path (resp. DAC critical path). The timer is not represented on the circuit. The bits *Setb* and *Reseth* on the circuit are controlled by the same initialisation signal *RESET*.

III. Design Methodology

As it is explained in Section II.1, the theory associated with the A-ADC is completely different from classical Nyquist ADCs. Thus, the purpose of the proposed methodology is to enable the designers to calculate the design parameters of an A-ADC, given an application. The input parameters are the analog signal characteristics and the desired ENOB, from which the four parameters characterizing an A-ADC must be computed. There is the resolution M (that defines the number of quantization levels), the loop delay δ, the period T_C of the timer, and the inner quantum q_{in} adopted for all the analog blocks design. The input signal must be perfectly known: its Power Spectral Density (PSD), its bandwidth f_{max}, its maximum amplitude ΔV_{in}, and its probability density $p(x)$. It is assured that the amplitude range ΔV_{in} of the signal fits the entire input range of the converter, so it is a known parameter.

III.1 Computing *M*

In the synchronous case, the Shannon theorem, insures the reconstruction of the original signal with a *sinc* basis. For irregular sampling, a reconstruction condition is deduced from the number of quantization levels (i.e. the resolution M), which directly influences the number of samples. It depends also on the signal variations. In an irregular sampling scheme, F.J. Beutler [10] proved that reconstruction of the original continuous signal is possible if the average sampling rate is greater than twice the signal bandwidth f_{max}. For a given type of signals: the density probability of its amplitude $p(x)$ and its maximum slope $\left|\frac{dV_{in}}{dt}\right|$ are known. By statistical considerations, the average sampling rate $\bar{f}_{sample}$ can be computed theoretically. It depends on M, which minimum value can be determined so as to respect the Beutler condition. The same method like the one given in [6] for a band-limited gaussian signal can be applied to determine the average sampling rate $\bar{f}_{sample}$. To conclude, the average number of samples per second will be minimum to insure a reconstruction, and so the activity and the power consumption will be minimized. Moreover, a low value for M insures a low hardware complexity and a reduction of the silicon area.

III.2 Computing δ and q_{in}

The knowledge of the amplitude range and the bandwidth of V_{in} enables us to find the boundaries of the slope using the Bernstein theorem: $\left|\frac{dV_{in}}{dt}\right| \leq 2.\pi.f_{max}.\Delta V_{in}$ (4). The number of quantization levels is now known: 2^M-*1*. According to the tracking condition (3), and the Bernstein inequality (4), the loop delay δ must verify: $\delta \leq \delta_{max}$, with: $\delta_{max}=\frac{1}{2.\pi.f_{max}.\left(2^M-1\right)}$

(5). When δ_{max} is fixed, q_{in} can be tuned in order for the loop delay δ to reach its upper bound.

III.3 Computing T_C

The first term of Eq. (1) can be computed from the PSD of the signal V_{in}. The desired ENOB gives the corresponding SNR, then the timer period T_C.

III.4 Design methodology

The design methodology is summed up in Figure 4. The desired ENOB gives T_C, and the signal properties give M, δ_{max} and q_{in}. In conclusion, exploiting the statistical properties of the signal leads to a low value for M, while keeping a high *ENOB*. The hardware complexity is thus much lower than in synchronous Nyquist ADCs. Hence, together with the silicon area reduction, such A-ADC has a reduced electrical activity.

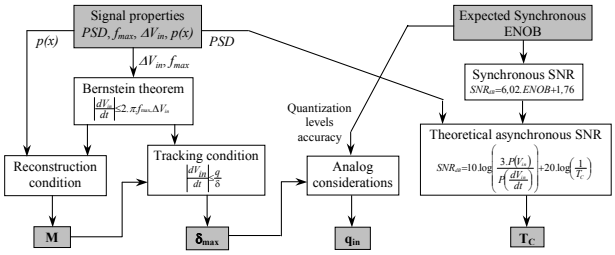

Figure 4: Design flow of an A-ADC given a targeted application.

IV. A design example

IV.1 Computation of the A-ADC parameters

The case study considered to illustrate our approach is the processing of speech signals. The parameters of such signals are perfectly known. The PSD is given in [7], Eq. (1) becomes: $SNR_{dB}=-66,3+20.\log\left(\frac{1}{T_C}\right)$ (6). The bandwidth of the signal is set to: $f_{max}=4kHz$, its amplitude ΔV_{in} is set to match 5% to 95% of the A-ADC input range. The probability density function p of the amplitude of the signal is a Laplacian distribution [11]: $p(x)=\frac{1}{\sqrt{2}.\sigma_x}.\exp\left(\frac{-\sqrt{2}|x|}{\sigma_x}\right)$ (7). It is easy to show that 99,65% of the speech samples belong to the range: $-4.\sigma_x \le x \le 4.\sigma_x$ (8). It is deduced that: $\sigma_x=\frac{0,9.\Delta V_{in}}{8}$ (9). When $M \ge 4$, the Beutler condition is verified: the average sampling frequency is: $\bar{f}_{sample} \approx 8,2kHz > 2.f_{max}$. The resolution of the A-ADC is then: *M=4-bits*. The tracking condition (5) gives the maximum loop delay: $\delta_{max}=2,65\mu s$. All the parameters being computed, the A-ADC can now be designed. An ENOB higher than *8-bits* is also targeted.

IV.2 Design of the A-ADC

We used the 0.18µm CMOS technology from STMicroelectronics. A current mode design has been chosen to implement the analog part. This prototype (including the conversion loop, the timer and the synchronization interface) enables us to perform electrical simulations (cf. Table1). The total measured delay δ of the conversion loop, needed to convert a sample, is $\delta=93ns$. This value is very far from the calculated limit of speech signals ($\delta_{max}=2,65\mu s$). Thus, with Eq. (5), a maximum input frequency of $f_{max}=114kHz$ could be accepted. The fact that the loop is faster is not important because activity is only determined by the input signal and the number of quantization levels.

Table 1. Electrical characteristics of the A-ADC targeted for a speech application.

Hardware resolution	*M=4-bits*
Timer	*18-bits, T_C^{-1} up to 36-MHz*
ENOB	*8 to 12-bits*
Technology	*0.18µm CMOS*
Power supply	*V_{dd}=1.8V*
Voltage dynamic	*ΔV=800mV*
Current quantum	*q_{in}=3.2µA*
Loop delay	*δ=93ns*
Input signal bandwidth	*f_{max}=114kHz*
Total static power consumption of the A-ADC	*P_{min}=0.898mW* *P_{max}=1.603mW*
Total dynamic power consumption of the A-ADC	*P_{avg}=1.716mW* *@A-ADC max. speed*
Timer consumption	*P_{timer}=0.015mW* (for *ENOB=10-bits*)
Analog area	*S_{analog}=220µm×68µm*
Digital area	*$S_{digital}$=160µm×80µm*

V. Discussion

V.1 Figure of Merit

The Figure of Merit (FoM) we have chosen is defined by: $FoM=\frac{2^{ENOB}.f_{samp}}{P_m.S}$ (10), where P_m is the average dissipated power in Watts (*W*), f_{samp} is the sampling frequency of the converter in Hertz (*Hz*), and *S* the area of the core of the circuit in m^2. More than forty recent ADCs published in *IEEE journals* and *IEEE conferences proceedings*, from 2000 to 2002 have been used for the comparison. The FoMs have been computed and are summed up in Figure 5. Each dot is below 10^{18} and it can be seen that the FoM of the A-ADC is one order of magnitude higher beyond *ENOB=11-bits*: it reaches $FoM=10^{19}$.

V.2 Conversion and signal processing

Let us now consider the use of ADCs in a signal-processing chain to estimate the global performances of a whole system.

The purpose of A-ADCs is to have an asynchronous system, processing the irregular sampled data. The digital output of the A-ADC is composed of couples (b_i, Dt_i) (cf. Section II.1). Usual Nyquist signal theory cannot be used, because samples are not time equi-spaced. Hence, new digital asynchronous circuits, performing Fourier Transforms, filtering, detection... directly on the irregular stream of data, are now under investigation in our research team, to implement such fully "asynchronous SoCs".

Nevertheless, the A-ADC can firstly be used as a low-power front-end in a classical Nyquist signal processing system. In this way, an interpolation stage must be added to re-sample the samples in a regular way. This aspect has been

studied in [7]. It is proved that the stream of data could be re-sampled to the Shannon frequency, respecting the initial A-ADC SNR, using a simple 2nd order polynomial interpolation.

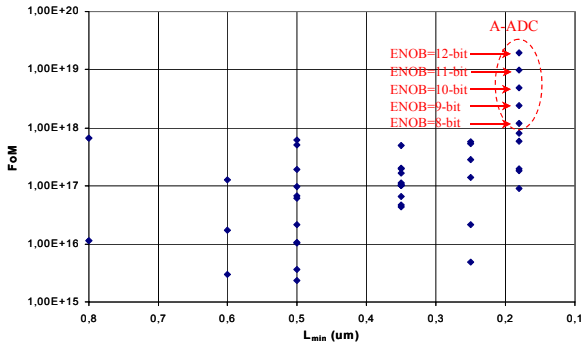

Figure 5: FoM of state-of-the-art ADCs and A-ADCs.

Let us now consider a similar approach for the synchronous Nyquist ADC. It is perfectly known that the ENOB of any Nyquist ADC can be improved by over-sampling at f_{sample} the input signal V_{in} and filtering the quantization noise outside the signal bandwidth. In this case: $SNR_{dB}=1,76+6,02.N+10.log\left(\frac{f_{sample}}{f_{Nyq}}\right)$ (11). The ENOB is improved by 1-bit, when the sampling frequency is multiplied by four. Given an *M-bit* resolution ADC, an effective resolution of *ENOB-bits* can be achieved if the sampling frequency is: $f_{sample}=4^{(ENOB-M)}f_{Nyq}$ (12). To preserve a similar hardware complexity for both types of conversions, we consider a Successive Approximation ADC (SA-ADC) for the synchronous reference. The SA-ADC output must be processed by a decimation filter to obtain the *ENOB-bits* of resolution and a sampling frequency of f_{Nyq}. It limits the bandwidth of the over-sampled input signal and down-samples the output. To simplify our comparison, we can consider the output digital stages of the two types of A/D converters (2nd order polynomial interpolation and decimation filter) as equivalent in terms of complexity and power consumption, although this approximation is certainly unfair to the A-ADC. Let's now analyze the two front-end conversion stages. For a speech signal, we have $f_{Nyq}=2.f_{max}=8KHz$. For a SA-ADC, *M* cycles are needed to convert a sample. Using Eq. (12), the number of cycles per second is: $f_{cycle}=4.M^{(ENOB-M)}f_{Nyq}$ (13). For the A-ADC, we always have $\bar{f}_{cycle}=\bar{f}_{sample}\approx 8,2kHz$. The gain brought by the A-ADC in terms of the number of cycles per second is: $G_{\%}(cycles/sec)=100.\left[\frac{2.N.f_{max}-\bar{f}_{sample}}{2.N.f_{max}}\right]$ (14).

Table 2: A-ADC vs. ov-samp. SA-ADC.

ENOB	SA-ADC nb cyc/sec	T_C (Hz)	A-ADC avg nb cyc/sec	G(%)
8-bit	512-k	754-k	≈ 8,2-k	98,39
10-bit	768-k	3,01-M	≈ 8,2-k	98,93
12-bit	1,024-M	12,06-M	≈ 8,2-k	99,19

The results are given in Table 2. Above *ENOB=10-bits*, the average number of cycles is reduced by two orders of magnitude for the A-ADC. Hence, in first approximation, a similar gain in power savings is achieved. Thus, an A-ADC could easily be used as a low-power front-end in a classical Nyquist rate signal processing chain. In this case, a 2nd order polynomial interpolation stage must be used.

VI. Conclusion

In this paper, a new class of ADCs based on an asynchronous design mode and an irregular sampling scheme. These two characteristics are the source of a significant reduction in power consumption, complexity and area. A methodology is also presented in order to design such converters, respecting a required ENOB, and exploiting the statistical properties of the analog input signal. An A-ADC has been designed for speech applications in the 0.18µm STMicroelectronics CMOS process. Electrical simulations demonstrate that the Figure of Merit (FoM) is increased by one order of magnitude compared to state-of-the-art synchronous Nyquist ADCs. In terms of applications, A-ADCs can be used in classical signal processing systems as a low-power conversion front-end. Nevertheless, our goal is to use these converters in fully asynchronous systems combining irregular sampling and asynchronous processing means. This solution is under investigation in our research team, and we believe it is one of the most promising approaches to reduce the power consumption of integrated mixed signal circuits by more than one order of magnitude.

VII. References

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