An All-Digital A/D Converter for Increased Resolution With a 2^{22}-Delay-Unit TAD Architecture Using Moving-Average Filtering

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Abstract – An all-digital A/D converter (ADC) for increased resolution with a 2^{22}-delay-unit delay-line using TAD architecture [1] is presented. The basic structure of the TAD is a completely digital circuit including a ring-delay-line (RDL) with delay units (DUs) and a frequency counter, latch and encoder. The operating principle is to count the number of DUs through which the delay pulse passes within a sampling time. A 22-bit TAD area is 0.34 mm^2 (0.65-μm CMOS), and its resolution of 1 μV/LSB (1 kS/s) per (1.5–2.5 V) was realized with 20-bit resolution. Sample holds are unnecessary, and a low-pass filter function [1] removes high-frequency noise simultaneously with A/D conversion. On the other hand, low-frequency noise can be eliminated by using digital correction with this TAD. The likelihood is also suggested that TAD has no internal low-frequency noise.

Keywords – ADC, moving-average, all-digital.

I. INTRODUCTION

In recent years, the ΣΔ modulation scheme has been one of the dominant architectures for high-resolution A/D converters (ADC) [2]-[4], either together with or replacing dual-slope type ADCs. Both types have analog circuits such as op-amps, resistors, capacitors, and occasionally inductors. For ease of design of the ICs and to overcome their undesirable aspects (power-consumption, external-parts, process options, and so on), analog parts should be eliminated from the ADC circuit itself. This paper presents a compact and high-resolution A/D converter consisting of an all-digital circuit.

II. PRINCIPLES OF OPERATION

We conceived an original A/D conversion method involving digitization of the number of stages of a *delay unit* (DU) through which a pulse passes within a specific time. This is a revolutionary method that does have not any passive elements such as resistors or capacitors [1]. The principles are as follows. 1) The pulse delay circuit is serially connected to the DU by a primitive gate circuit in the digital circuit, wherein the delay time (Td) of the DU is modulated by the voltage Vin (power-supply) for A/D conversion. In this way the Td is changed with high sensitivity, approximated by the following equation (1) [5]:

$$Td = A\,Vin / (Vin - Vth)^{\alpha} \quad : \alpha = 1.4 \text{ to } 1.6 \qquad (1)$$

where A and α are constant depending on process technology. This equation (1) means that increasing Vin shortens the Td effectively. 2) A digital value (DT) reflecting the input voltage Vin can be obtained by digitizing the number of DUs through which the pulse passes during a fixed time Ts, and outputting this number as output data DT. Since the number of stages of the delay pulse passing through the DU is dependent on the sampling frequency fs (1/Ts), the A/D conversion resolution is controllable by setting the fs using the following equation (2) [1].

$$DT = (1/fs)\{(Vin - Vth)^{\alpha} / A\,Vin\} \quad : \alpha = 1.4 \text{ to } 1.6 \qquad (2)$$

III. BASIC CIRCUIT STRUCTURE

Figure 1 shows the basic structure of the new ADC. This ADC is a completely digital circuit including a ring-delay-line (RDL in Fig. 2) with 16 delay units (DUs) consisting of 2 inverters per DU, along with an 18-bit frequency counter, latch and encoder. Data on the difference between successive data from the latches are output as 22-bit DT conversion data (this type of ADC is called TAD [1], especially for sensors). Sample holds are unnecessary, and a low-pass filter function, or an analog moving-average processing [1], removes high-frequency noise simultaneously with A/D conversion. Thus, the combination of this ADC (TAD) and the digital filter that follows can eliminate the need for an analog pre-filter to prevent the aliasing before A/D conversion.
Finally, an original architecture for the TAD was made possible by applying a circuit system [6]-[8] devised to allow stable reading of the frequency of an RDL operating at high speed. A detailed explanation of the RDL frequency readout method is that: 1) In the first step, frequency readout data are obtained using two latches L(a) and L(b). A given time delay, Tdly, is obtained with the latch timing as the difference between L(a) and L(b). The Tdly is set to 8 stages, half the RDL 1 cycle (period). In this way, we can always go outside the counter output

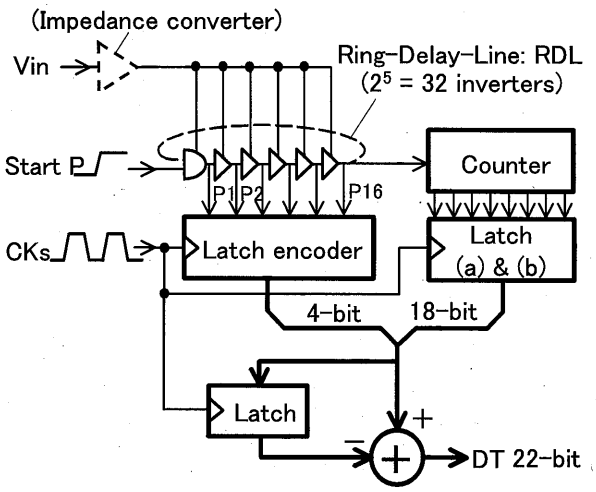

Fig. 1. Block diagram of the 22-bit ADC (TAD).

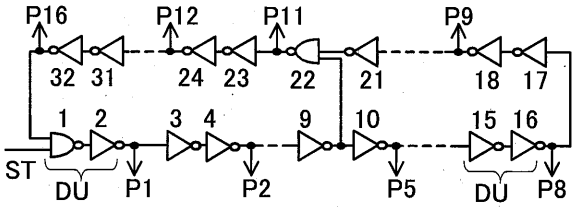

Fig. 2. Block diagram of the RDL.

data transition phase with one latch. Thus, with stable timing, counter output data can be obtained. 2) In the second step, latch L(a) or latch L(b) is selected. Selection control is done by the encoder MSB output. When the MSB is at zero, the latch L(b) output data with Tdly are selected, and when the MSB is at 1, the latch L(a) output data are selected.

IV. RDL CONFIGULATION

The configuration of the newly designed ring-delay-line (RDL) is shown in Fig. 2. The difference between the RDL and a conventional ring oscillator is the number of gates making the ring circuit. The RDL consists of an even number of inverters and NAND gates (total of 32 gates). On the other hand, a conventional ring oscillator is made with an odd number of inverters (ex. 31 gates).

If DUs consist of *1 inverter* for increasing resolution, the TAD with the conversion data is separated into 18 high order bits and *5 low order bits*. That is, the phase difference in the polyphase delay pulse (P1, P2, P3---P32) with output from the ring-delay-line is used as the resolution of the 5 low order bits, and the RDL uses one cycle period as the unit for the high order bits. For this reason, configurations with odd gate numbers (31 inverters) were adopted in conventional ring oscillators, so only odd number polyphase delay pulses could be output, resulting in a lack of code (continuous lack) between the high and low order bits.

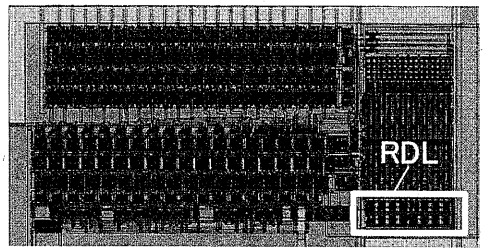

Fig. 3. Photomicrograph of 22-bit TAD-IC chip (0.85 mm x 0.40 mm: 0.65-μm CMOS).

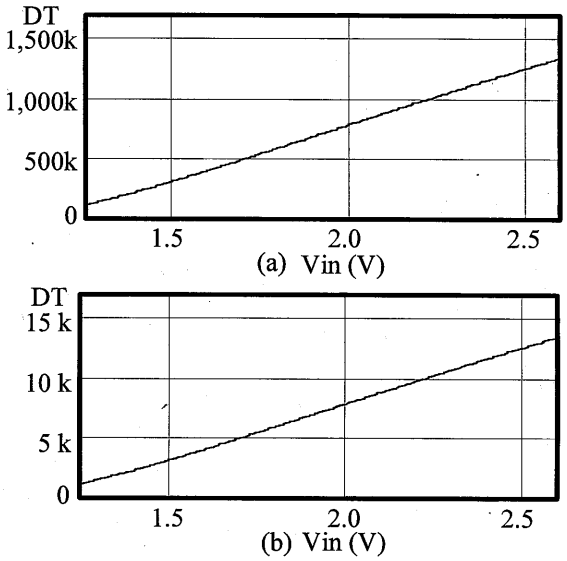

Fig. 4. Characteristics of A/D conversion (Vin range = 1.3-2.6 V, 25 °C): (a) Sampling frequency fs = 1 kHz. (b) Sampling frequency fs = 100 kHz.

Therefore, as shown in Fig. 2, we devised a ring-delay-line (RDL) with an even number of stages using a double loop. In the RDL the leading (main) edge and trailing (reset) edge go around simultaneously, so the RDL could output a polyphase delay pulse of 2 to the nth power (2^5 = 32) stages [9]. In the present study, a 2-inverter DU can be used with the even-gate RDL in order to closely match the mutual characteristics of the DUs. In this circuit, a 16-stage (P1~P16) polyphase delay pulse is generated when the starting signal ST reaches level H.

V. 1-TAD EVALUATION RESULT

A 22-bit TAD was realized with an ADC having a circuit area of 0.34 mm^2 (0.65-μm CMOS), as shown in Fig. 3. The small-framed area is the RDL. Since there are few delay units (DUs), the area voltage-modulated by the input voltage Vin can be extremely small, to closely match the mutual characteristics of the DUs.

The A/D conversion characteristics at a sampling frequency fs = 1 kHz (25°C) are shown in Fig. 4(a). Approximately 310,000 to 1,250,000 digital values

correspond to a range from 1.5 to 2.5 V. Accordingly, the voltage resolution (Vd) is extremely high (about 20-bit) at approximately 1.06 μV/LSB. Non-linearity is around ±1% FS per 1000 mV, but non-linearity errors can be easily compensated for by digital processing using reference points (see Section IX). Next, the A/D conversion characteristics at fs = 100 kHz are shown in Fig. 4(b). The voltage resolution is also high (13-bit) at 106 μV/LSB.

Resolution density drift was approximately -20%, +40% against 25℃ changes in a range of -35~140°C, but this can be resolved by digital calculation correction to obtain the ratio to a reference value [10], [11].

VI. Low-Frequency Noise Reduction

Figures 5(a) and 5(b) show a low-frequency noise (a) (548 LSB: about 600 μV-drift between 60 seconds) caused by CMOS input buffer, and the compensation result (b) (5 LSB: < 6 μVpp between 60 s). With this method, first the A/D conversion voltage Vin (2.5 V) and reference voltage Vr (2.5 V) are quickly A/D converted alternatively by TAD (fs = 1 kHz). Switching of analog-switches synchronized with TAD operation, and the process of averaging 1000 data points for Vin and Vr are then executed respectively, after which the data ratio (ave.Vin/ave.Vr) is calculated by the digital correction processor. If Vin is not equal to Vr, this low-frequency noise removing effect can be realized by calculating (Vin/Vr), because TAD has an extremely wide dynamic range and the signals (Vin, Vr) have almost the same noise level (detailed explanations are given in [12]).

VII. 4-TAD Evaluation Result

A/D conversion characteristics of a test board applying the sums of 0.8-μm CMOS 4-parallel TAD at fs = 1 MHz (25°C) are shown in Fig. 6 without digital averaging.

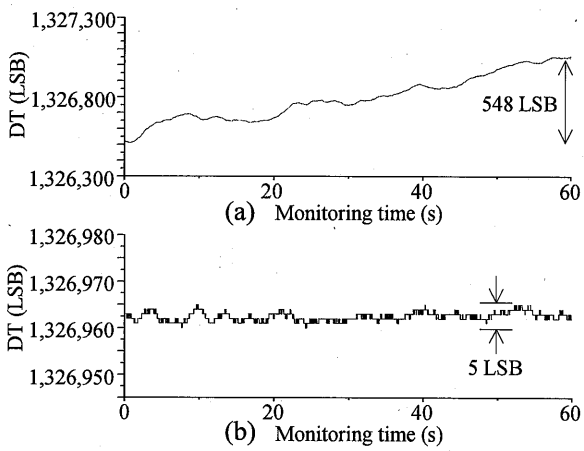

Fig. 5. Low-frequency noise removing result: (a) Before compensation. (b) After compensation. (sampling frequency: 1 kHz, 25 °C).

Approximately 3000 to 5600 digital values correspond to a range from 2.0 to 2.8 V. Accordingly, the voltage resolution is still high (11 bits) at approximately 300 μV/LSB. Non-linearity is ±0.9 % FS. Each RDL in TAD has some respective jitter [1] so that a dither effect can be obtained using only a digital averaging filter following the TADs.

Since this high-resolution ADC architecture can be made with an all-digital circuit, advances in process technology will lead to both shorter Td and easier parallel A/D processing of numerous TADs. These effects will enable higher and higher resolution. A high degree of Ts reproducibility is required (minimal clock jitter), but this does not pose a problem if a typical quartz resonator clock is used. In addition, the dither effect will be unnecessary if the 4 TADs are made to have an offset value of (1/4) LSB with respect one another by modifying their respective resolutions.

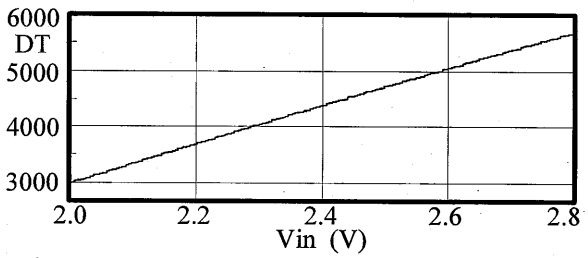

Fig. 6. Characteristics of A/D conversion of 0.8-μm CMOS 4-TAD [1] parallel construction (sampling frequency: 1 MHz, 25 °C).

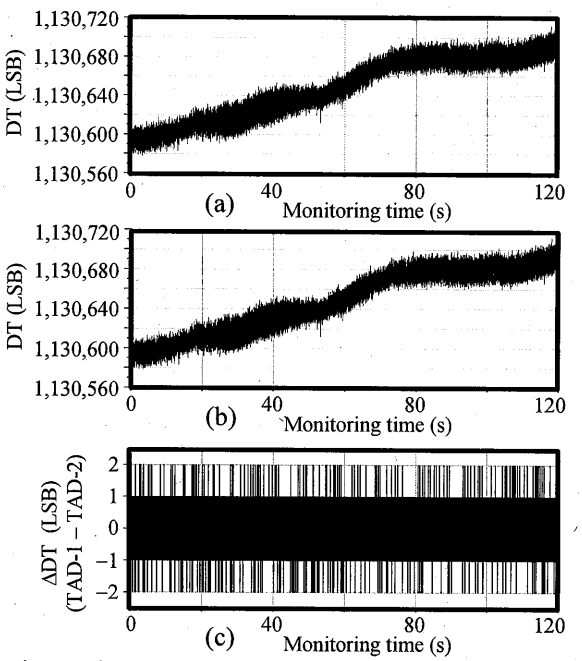

Fig. 7. Fluctuation of respective TAD (Vin = 2.4 V, fs = 1 kHz, 25 °C): (a) TAD-1. (b) TAD-2. (c) Fluctuation in TAD itself = difference between TAD-1 and TAD-2.

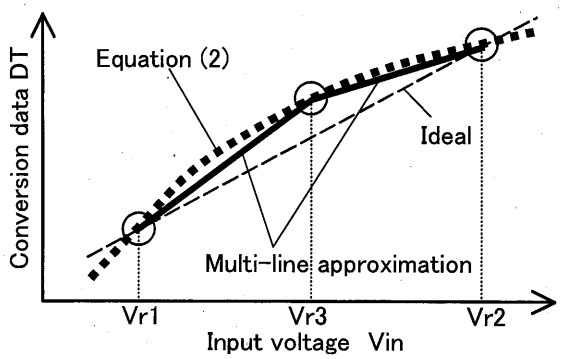

Fig. 8. One method of correcting non-linearity.

Table I. Non-linearity error with correction (%FS)

	Vin span	Vin center voltage (V)		
		1.8	2.0	2.5
Non-correction	200 mV	±0.130	±0.182	±0.207
	1000 mV	–	–	±1.022
Multi-line Approxi-mation	200 mV	±0.037	±0.047	±0.052
	1000 mV	–	–	±0.264
Parabolic Approxi-mation	200 mV	±0.011	±0.005	±0.001
	1000 mV	–	–	±0.041

VIII. TAD STABILITY DISCUSSION

Figure 7(a) and 7(b) shows respective output data of two TADs (TAD-1 and TAD-2) for 120 seconds, under the exact same conditions (using same Vin = 2.4 V, same sampling clock at 1 kHz, and under same temperature 25°C). The data difference between TAD-1 and TAD-2 is nearly 0 (±2 LSB), as shown in Fig. 7(c). Although the individual output data has a large drift quantity (about 100 LSB) due to condition-drift for 120 s, given that Figure 7(c) shows no fluctuation it should be expected that TAD has no low-frequency noise in itself due to its switching behavior without steady-state current.

IX. NON-LINEARITY CORRECTION

Although the TAD has non-linearity error for Vin, this is not difficult to correct by applying digital calculation processing, because its behavior can be predicted from the approximation equation (2). One correction method is shown in Fig. 8, using multi-straight-line approximation with three reference values (Vr1, Vr2, Vr3). Another is parabolic approximation with three references. Table I shows TAD integral non-linearity error and its correction simulation results according to equation (2).

X. CONCLUSION

In moving toward high-resolution ADC, advances in process technology and parallel A/D processing of multiple TADs (numerous TADs) will enable higher and higher resolution, despite using the same sampling rate. It should also be mentioned that this all-digital ADC (TAD) can be downsized and operated at low voltage, so it is an ideal means to lower the cost and power consumption, and make IC design easier. Both low- and high-frequency noise can be removed by using uniqueness of TAD technology.

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