Rail-to-Rail High Gain Telescopic Operational Amplifier Using Positive Feedback Technique

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Abstract

A CMOS very high DC-gain telescopic amplifier that uses internal positive feedback technique is presented. The structure of considered amplifier is consisted of rail-to-rail output swing and very high DC-gain. Simulation results predict a DC-gain can be achieved larger than 100dB without limiting the output swing. The proposed amplifier is applied to sample and hold circuit for 10bits 100Ms/s ADC.

Keywords

Positive feedback, Amplifier, Telescopic, Output swing, high DC-gain, Bandwidth

1. Introduction

There are three fundamental techniques for gain enhancement: gain-boosting technique, cascading stages, and positive feedback gain enhancement technique. Gain-boosting technique is one of the most successful ways of boosting amplifier gain, even though boosting amplifier adds their own poles and zeros to the final amplifier, which affects amplifier settling slow [1]-[2]. On the other hand, cascading two stages or more will result in a very high DC-gain. However, proper compensation for stable operation in cascading technique seriously limits the high frequency performance [3]-[4]. As the supply voltage is reduced, conventional gain enhancement techniques such as gain-boosting technique and cascading stages do not give great effect any more.

In recent years, to overcome the obstacles that are inherent in conventional gain enhancement techniques, especially in very low supply voltage circuits, the positive feedback gain enhancement technique has received increasing attention [5]-[8]. By using the positive feedback, we can obtain a very high DC-gain, which is ideally infinite gain without affecting high frequency performance. Even though it has such an advantage, most of the positive feedback implementations have suffered from three problems: sensitivity to temperature and process variation of the transconductance of each transistor, strong dependence on output signal level of the transconductance or the conductance of transistor that has its gate directly connected to the output node, and a limited output swing of the amplifier when the output impedance is very low [5], [7]. The first problem has dealt in [1]-[3], while the second problem can be relaxed by applying a self-adjusting feedback with cascoding [5].

In this paper, we consider the third problem, problem of limited output swing, and as an approach we present a high DC-gain telescopic amplifier, which is using internal positive feedback technique without limiting the output swing.

2. Introduction to Positive Feedback Technique

The basic concept of positive feedback system is shown in Fig. 1[8].
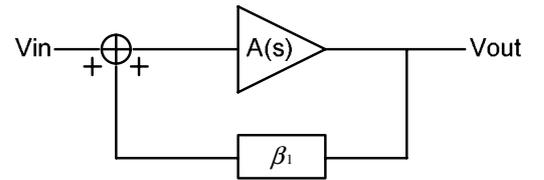

Fig. 1. Positive feedback system.

Assume the feedforward amplifier has a one-pole transfer function:

$$A(s) = \frac{g_m}{g_o + sC} \qquad (1)$$

where g_m, g_o, and C are the small signal transconductance, output conductance of the amplifier, and the total capacitive load at its output, respectively. The transfer function of the closed-loop system is given by

$$\frac{V_{out}}{V_{in}} = \frac{A(s)}{1 - \beta A(s)} \quad , \quad \frac{V_{out}}{V_{in}} = \frac{g_m}{\varepsilon + sC} \qquad (2)$$

where β is the feedback factor of the closed-loop system and ε is defined as

$$\varepsilon = g_o - g_m \beta \qquad (3)$$

Therefore, the DC-gain of amplifier is represented to

$$A_{v(openlooppos.fb)} = \frac{g_m}{\varepsilon} \qquad (4)$$

Note that if we choose β such that ε is close to zero, we obtain the required high DC-gain.

3. Conventional Positive Feedback Amplifier

Conventional folded cascode amplifier using positive feedback technique is shown in Fig. 2.

The DC-gain of this amplifier is represented as the following equations.

$$A_v = \frac{G_m}{(g_{o2} + g_{o12} - g_{o4} - g_{o10})(g_{m8}g_{o6} - g_{m6}g_{o8})} \quad (5)$$

$$g_{o2} + g_{o12} = g_{o4} + g_{o10} \quad (6)$$

where g_{oi} and g_{mi} are the small signal transconductance and output conductance of the amplifier for each transistor, respectively.
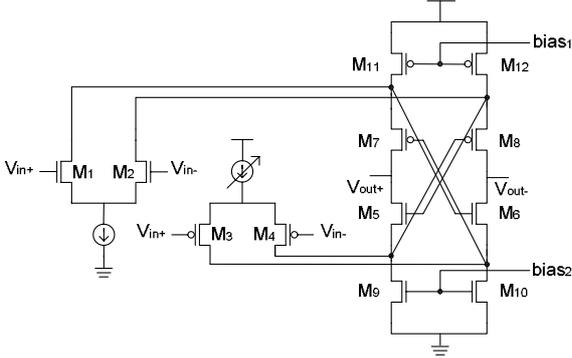

Fig. 2. Conventional folded cascode amplifier.

If the DC-gain satisfies Eq. (6), then we obtain very high DC-gain. However, this amplifier has some problems such as requiring additional external bias for controlling the DC-gain, using two complementary differential stages in parallel, and limited output swing. Requiring additional external bias for controlling the DC-gain is caused by the fact that the current source is controlling both g_{o4} and g_{o10} to obtain the required amplifier gain to relax the transistor matching. In addition, two complementary differential stages in parallel are used to increase the gain-bandwidth of the amplifier and two parallel differential amplifiers increase the input capacitance, which can limit high frequency performance. Moreover, since the output impedance is very low [5], [7], this amplifier has a limited output swing.

In this paper, we approach these problems by presenting a high DC-gain telescopic amplifier, which uses internal positive feedback technique without limiting the output swing.

4. Description of The Proposed Amplifier

The proposed telescopic amplifier is shown in Fig. 3. Common mode feedback circuit and biasing circuit are not shown for simplicity. This amplifier has an open-loop gain A_v with the following simplified form, which is obtained from the small signal model described in Fig. 4.

$$A_v \approx \frac{g_{m1}(g_{m5} + g_{o5} + g_{m7})}{g_{o5}g_{m7} - g_{o7}g_{m5} - g_{o5}g_{o1} - g_{o7}g_{o1} - g_{o5}g_{o7}} \quad (7)$$

Eq. (7) shows that the proposed amplifier exhibits a positive feedback property. To obtain large value of A_v, we assume that $g_{o1} \approx 0$ and so the following condition.

$$\frac{g_{m5}}{g_{o5}} = \frac{g_{m7} - g_{o7}}{g_{o7}} \quad (8)$$

If open-loop gain of amplifier satisfies the condition of Eq. (8), we can obtain the required high DC-gain.

Ignoring the bulk effect, the transconductance and output conductance of the amplifier are respectively defined as

$$g_m \approx \mu C_{ox}(W/L)V_{DS} , \ g_o \approx \mu C_{ox}(W/L)(V_{GS} - V_{TH} - V_{DS})$$

In the above equation, μ, C_{ox}, V_{TH}, V_{GS}, V_{DS}, W, and L represent the mobility, the capacitance per unit area between the gate and channel, the threshold voltage of the transistor, the voltage between the gate and source, the voltage between the drain and source of the transistor, the width of the device, and the channel length, respectively.

Therefore, Eq. (8) can be rewritten by the following equation.

$$\frac{V_{DS5}}{V_{GS5} - V_{THN} - V_{DS5}} = \frac{2V_{SD7} - V_{SG7} + |V_{THP}|}{V_{SG7} - |V_{THP}| - V_{SD7}} \quad (9)$$

We notice that the DC-gain of the amplifier can be determined by the voltage ratio from Eq. (9).

Since the four transistors M5, M6, M7, and M8 are operated in the triode region, the output swing does not limited by the transistors. Furthermore, if we reduce the length of these four transistors, we can obtain much higher frequency performance [5].

The proposed amplifier does not include transistors that its gate directly connected to the output node. Connecting the gates of transistors to the nodes created by cascading instead of connecting to the output nodes which have a large voltage swing may cause reducing dependence on output signal of the transconductance and the output conductance [5].
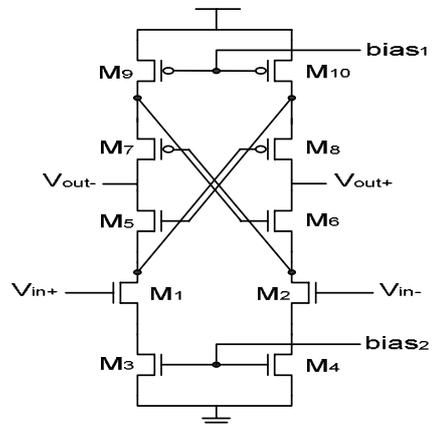

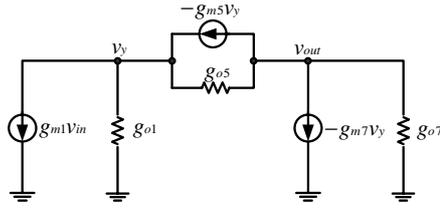Fig. 3. The proposed telescopic amplifier.

Fig. 4. Small signal model of the proposed amplifier.

Even though DC-gain depends on input common mode voltage and requires a replica biasing circuit to maintain the high DC-gain always, the proposed amplifier provides a potential to build fast amplifier with high DC-gain.

In the following section, we illustrate simulation results and present an application of the proposed amplifier.

5. Simulation Results

The proposed telescopic amplifier is simulated using CMOS 0.25um 1-Poly 5-Metal process. The amplifier consumes 1mA total current using 2.5V supply voltage and 0.5pF load capacitor. Simulation shows that the amplifier has 120dB DC-gain with 1.1GHz unity gain frequency. The result of AC analysis and the DC characteristic are shown in Fig. 5 and Fig. 6. A performance comparison between conventional [7] and proposed amplifier is shown in Table 1. Even though two amplifiers both exhibit a positive feedback property, we have implemented the negative feedback system to be embedded the positive feedback [8] to relax most of the disadvantages of the positive feedback technique implementation. That is, the proposed amplifier is applied to a sample and hold circuit with two non-overlapping clocks at frequency of 100MHz. The S/H circuit and the S/H differential output are shown in Fig. 7 and Fig. 9. Moreover, the simulation result of the settling time of the S/H circuit is presented in Fig. 10. The S/H circuit consumes a total current of 1mA and drives 0.5pF load capacitance. The sampling capacitor has a size of 0.74pF and the sample and hold circuit has a unity gain. Simulation results show that the amplifier is able to settle to an error less than 0.1mV for 1Vpp output swing within 2.1nsec, which is equivalent to 13 bits of accuracy. Timing diagram of S/H circuit is shown in Fig. 8. To minimize the charge injection and clock feedthrough effects, when switching from sample to hold mode, switch S3 opens first, and then S1 opens [9]-[10]. Therefore, the charge injection and clock feed through are independent of the input signals. The time between two clocks should be short compared to variations in the input signals.

Table 1. Comparison between conventional and proposed.

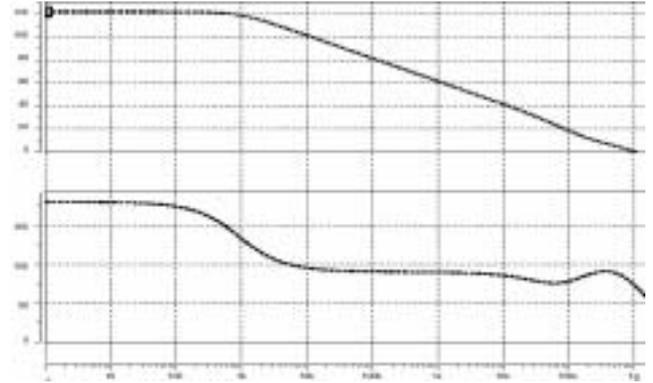| POSITIVE TEC.	CONVENTIONAL[7]	PROPOSED
DC-Gain	107.3 dB	120 dB
Unity Gain Freq.	805MHz	1.1GHz
Phase Margin	75 degrees	74 degrees
Total Current	1.2mA	1mA
Output Swing	0.3Vpp	2.5Vpp
Supply Voltage	2.5V	2.5V
Load Cap.	0.5pF	0.5pF

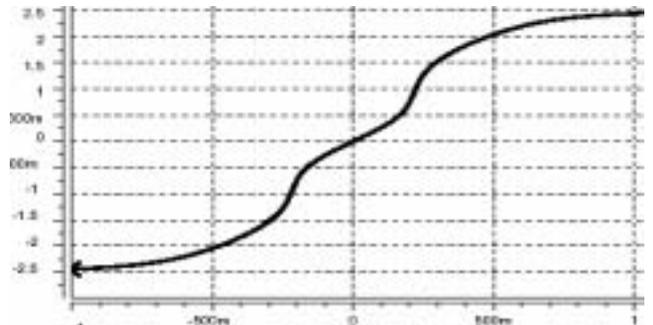Fig. 5. AC characteristic of the proposed amplifier.

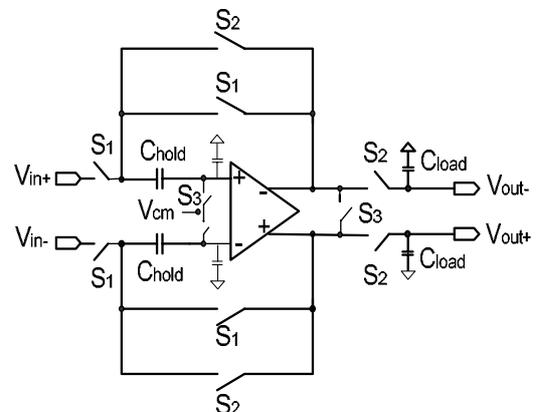
Fig. 6. DC sweep of the proposed amplifier.

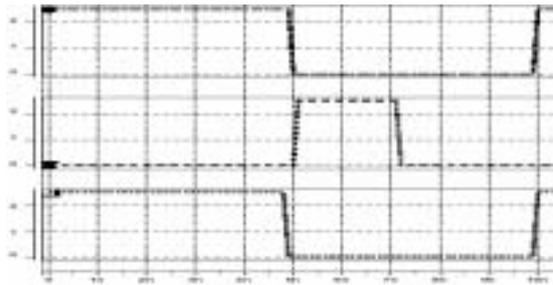Fig. 7. The S/H circuit using the proposed amplifier.

Fig. 8. Timing diagram of S/H circuit (S1, S2, S3).
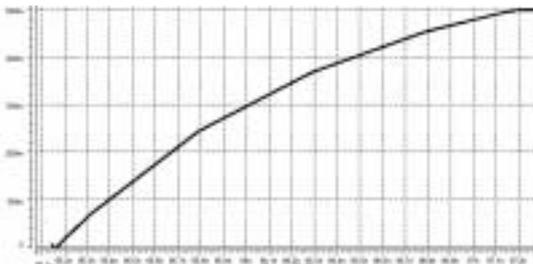

Fig. 9. The S/H differential output (@25MHz sine).

Fig. 10. Settling time of the S/H circuit.

Table 2. Simulated S/H performance.

Total Current	1mA
Error@2.1n sec	0.01%
Settling Time	2.1n sec
Sampling Capacitance.	0.74pF
Load Capacitance.	0.5pF
Output Swing	1Vpp
Supply Voltage.	2.5V

6. Conclusion

Even though the positive feedback technique offers potential for overcoming some of the obstacles that are inherent in conventional popular gain enhancement techniques, it has suffered from some problems. To overcome these problems, the telescopic amplifier that uses positive feedback technique has been proposed to obtain very high DC-gain with rail-to-rail output swing. By the proposed amplifier, we can obtain very high DC-gain under the certain condition. Moreover, it is applicable to charge-transfer circuit such as the sample and hold circuit for 10bits 100Ms/s ADC. Simulation results show that the amplifier has 120dB DC-gain with a unity gain frequency of 1.1GHz and that the S/H circuit is able to settle to an error less than 0.1mV for 1Vpp output swing within 2.1nsec.

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