

# Modeling charge injection non-linear effects in Sigma-Delta Modulators using SIMULINK

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**Abstract** - Sigma-delta ( $\Sigma\Delta$ ) modulators are the most suitable A/D converters for low to medium frequencies, high-resolution applications, in view of their inherent linearity, reduced antialiasing filtering requirements and robust analog implementation. Moreover, the growing market for asymmetrical digital subscriber line (ADSL) applications is a driving force for the development of high speed, high resolution, sigma-delta analog-to-digital converters (ADC's). In the wider development of ADC systems, a pre-eminent role has been played by modeling techniques. Modeling of ADC allows the device behavior to be predicted with a few of preventive experiments. For this reason, in the last years a great deal of scientific interest has been directed to ADC modeling.

In this work we present a SIMULINK model, which takes into account, for the first time, the non-linear effects due to switch charge injection in Sigma-Delta modulators. These effects are non-linearly proportional to the input voltage value. This brings about offset and harmonic distortion. Therefore adequate modeling of charge injection in terms of harmonic distortion is extremely important to predict and estimate the performance of Sigma-delta modulators.

**Keywords** - Charge injection modeling, Sigma-Delta converters, Switched-capacitor integrators.

## I. INTRODUCTION

First of all, we consider a second order Sigma-Delta modulator, shown in Fig. 1 [1]. One of the basic blocks is the discrete time integrator. In this work, we refer to the schematic of a single-ended Switched-Capacitor (SC) integrator shown in Fig. 2, where we suppose that all switches are nMOS transistors. During the sampling phase, the input signal of the switched-

capacitor integrator is sampled through switches  $S_1$  and  $S_2$  (driven by  $\phi_1$ ) on the sampling capacitance  $C_S$ .

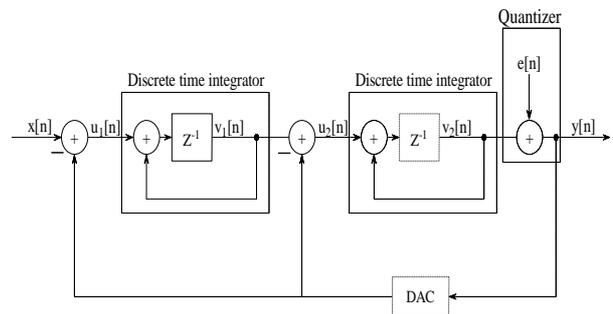


Figure 1: Second order sigma-delta modulator.

The resistance of switch  $S_1$  depends directly on the input signal [2] and therefore it causes harmonic distortion. Switch  $S_2$ , on the other hand, has always one terminal connected to a fixed voltage. So at the end of the sampling phase, the voltages at the source and drain of that switch are nearly constant during the clock period. Therefore, the distortion generated by this switch can be neglected compared to the distortion introduced by switch  $S_1$ . The same applies to switch  $S_3$  and  $S_4$ , which at the end of the integration phase are connected to a reference voltage or virtual ground of the operational amplifier, respectively.

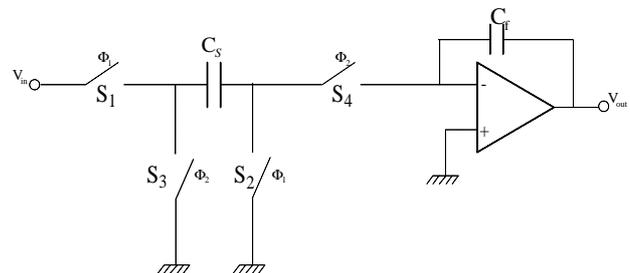


Figure 2: Non-inverting single-ended switched capacitor integrator.

Furthermore, during the integration phase, no time-varying input signal is driving the circuit. A charge, proportional to the input signal, is transferred from the sampling to the integration capacitance. Since this is like applying a dc signal (offset) during every clock phase,  $S_3$  and  $S_4$  generate considerably less distortion. Therefore, to study the distortion introduced by nMOS transistors, only the sampling operation through switches  $S_1$  and  $S_2$  is considered [2]. Distortion mechanisms in MOS switches include the effects of [2] [3] [4]: nonlinear MOS switch on-resistance, nonlinear switch parasitic capacitance and nonlinear signal-dependent switch charge injection. In particular the injection of charge caused by on-off transitions, critically affects the linearity and the SNR [3]. When on, an nMOS transistor carries a certain amount of charge in its channel that, under strong inversion conditions, can be expressed as [5]:

$$Q_{ch} \approx WLC_{OX}(V_{GS} - V_{TE})$$

where  $C_{OX}$  is the gate oxide capacitance per unit area,  $W$  and  $L$  are the effective width and length of the device, respectively,  $V_{GS}$  is the gate-source voltage ( $V_{GS} = V_G - V_{in}$ ) and  $V_{TE}$  is the effective threshold voltage including body effect [6]:

$$V_{TE} = V_{T0} + g(\sqrt{\Phi_B + V_{in}} - \sqrt{\Phi_B}) \quad (1)$$

$V_{T0}$  is the zero bias threshold voltage,  $g$  is the body factor and  $\Phi_B$  is a parameter related to the surface potential (it is often taken equal two times the Fermi potential  $\Phi_F$ ).

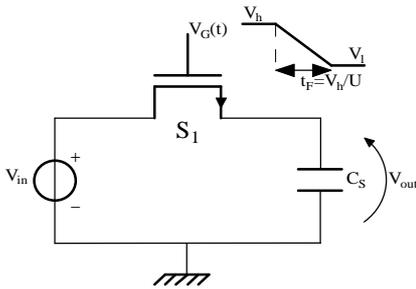


Figure 3: Simplified model used in the analysis of switch charge injection.

When the transistor turns off, the charge leaves the channel through the source and drain terminals, introducing an error voltage  $v_L$  on the sampling capacitor  $C_S$  (see Fig. 3). This error appears as a

nonlinear term since  $Q_{ch}$  has a nonlinear dependence on the input signal, which arises primarily from the nonlinear dependence of  $V_{TE}$  on the input voltage through body effect (see equation (1)). Therefore opening a switch produces a charge injection that is non-linearly proportional to the input voltage. This brings about offset and harmonic distortion.

The paper is organized as follows. In Section 2 we introduce the model approach for the estimation of charge injection non-linear effects in Sigma-Delta modulators. In Section 3 we present and we discuss simulation results obtained using SIMULINK. Finally the conclusions are drawn.

## II. MODEL DESCRIPTION

### A. Charge injection model formulation

To compute the error voltage due to charge injection, we propose the following formulation [7] by applying the Kirckhoff Current Law to the circuit shown in Fig.3:

$$C_S \frac{dv_L}{dt} = -I_D + \frac{1}{2} \frac{dC_G(V_G(t) - v_L)}{dt} \quad (2)$$

where  $v_L$  is the error voltage at the data-holding node,  $V_G(t)$  is a ramp function (see Fig. 3) which falls linearly from the high value  $V_h$  towards the low value  $V_1$  (in this work  $V_1 = 0V$ ) at the falling rate  $U$ :

$$V_G(t) = V_h - Ut$$

$C_G$  is the total gate capacitance, including both the channel and the overlap capacitances:

$$C_G = WLC_{OX} + 2C_{OV}$$

The MOS transistor operates in strong inversion (linear region), then:

$$I_D = b(V_G(t) - V_{in} - V_{TE})v_L$$

where

$$b = mC_{OX} \frac{W}{L}$$

Following [7], we can simplify the differential equation (2) to:

$$C_S \frac{dv_L}{dt} = -b(V_h - V_{in} - V_{TE} - Ut)v_L - \frac{C_G}{2}U \quad (3)$$

where we suppose that  $V_{in}$  assumes a constant value.

## B. Modeling charge injection in Sigma-Delta modulators

To visualize the non-linear effects introduced by charge injection in Sigma-delta converters, we consider as input a sine wave in the time domain ideally sampled at frequency  $f_s$  ( $T_s=1/f_s$ ), as depicted in Fig. 4.

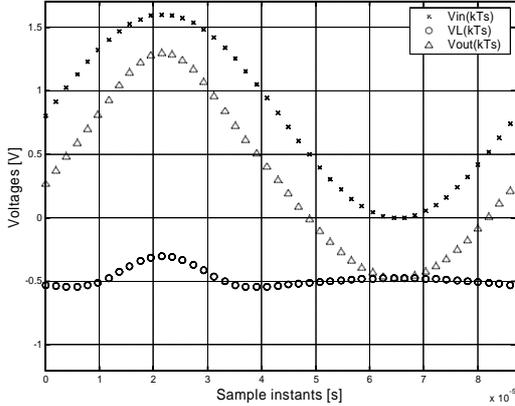


Figure 4: Sample behavior of the input signal  $V_{in}(kT_s)$ , error signal  $V_L(kT_s)$  and output signal  $V_{out}(kT_s)$ .

For each sample, we calculate the error voltage  $v_L$  due to the charge injected onto  $C_s$ , solving differential equation (3). Then we determine the behaviour of the injected charge for all samples in terms of the error voltage  $v_L(kT_s)$  (see Fig. 4). As we can see from Fig. 4, this behaviour is heavily nonlinear (we only show one period for simplicity) [8]. Finally, we reconstruct the output voltage waveform in the following way:

$$V_{out}(kT_s) = V_{in}(kT_s) - |v_L(kT_s)| \quad (4)$$

The SIMULINK model that we use is shown in Fig. 5. We start from the model presented in [9], but we add a new block named “Charge” that represents a signal source that loads the input voltage corrupted by charge injected onto  $C_s$ , i.e.  $V_{out}(kT_s)$  (see equation (4)). In this way, we can take into account charge injection non-linear effects and also a complete set of other sigma-delta modulator non-idealities, such as sampling jitter,  $KT/C$  noise and operational amplifier parameters (noise, finite gain, finite bandwidth, slew-rate and saturation voltages) [9].

## III. SIMULATION RESULTS

To validate our model concerning the effects of charge injection on the operation of an SC  $\Sigma\Delta$  modulator, we performed simulations with SIMULINK on the second order modulator shown in Fig. 5 [9], using ATMEL

0.24 $\mu$ m technology parameters. In all simulations parameters are  $V_h=2.5V$ ,  $C_s=0.5pF$ ,  $W/L=50\mu m/5\mu m$ .

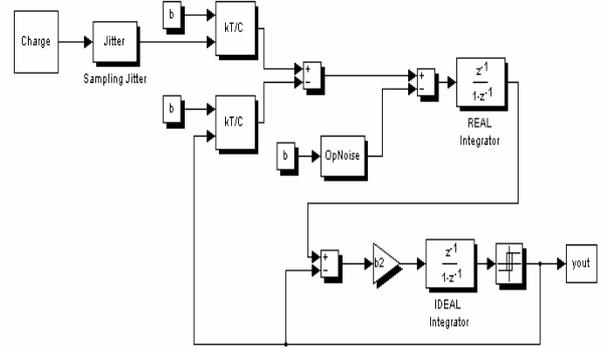


Figure 5: Second order  $\Sigma\Delta$  modulator model.

Fig. 6 shows the PSD (Power Spectrum Density) of an ideal 2<sup>nd</sup> order  $\Sigma\Delta$  modulator considering an input signal sine wave with amplitude  $Ampl = 0.8V$ . Fig. 7 shows the PSD of the same modulator only considering charge injection non-linear effects and not taking into account other non ideal effects. We can see that the SNDR is 70dB lower than the ideal case.

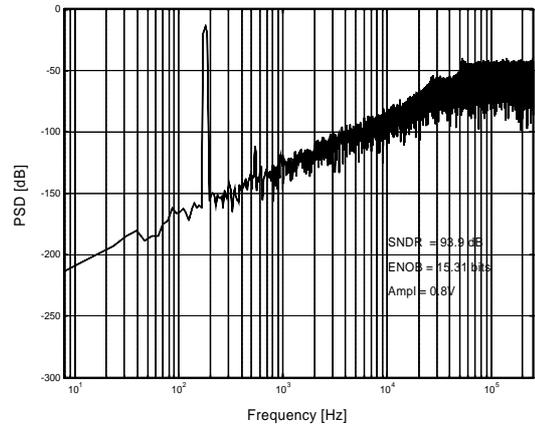


Figure 6: PSD of the ideal modulator.

As we can see comparing Fig. 6 with Fig. 7, the charge injection increases the in-band noise floor and also produces harmonic distortion. Fig. 8 shows the SNDR and ENOB against the fall time  $t_F$  of signal  $V_G(t)$  (see Fig. 3). We can see that both SNDR and ENOB decrease decreasing the values of  $t_F$ , i.e. increasing the slope of clock signal. The ENOB is calculated in the following way:

$$ENOB = \frac{SNDR - 1.76}{6.02}$$

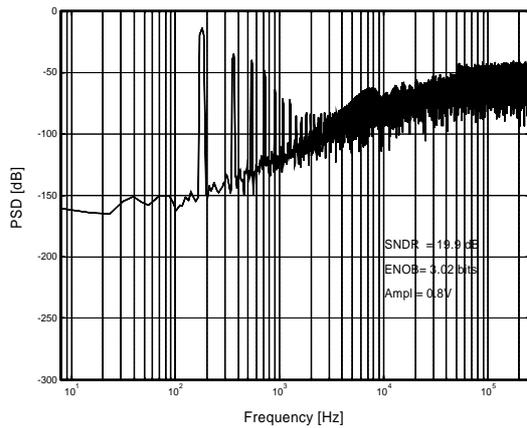


Figure 7: PSD considering charge injection effects.

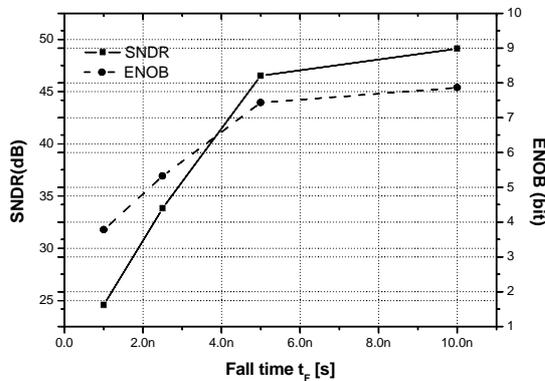


Figure 8: SNDR and ENOB against fall time  $t_f$ .

It must be noted from the above results that, because the charge injection non ideal effects result from practical circuit limitations, they can become a severe limitation to the performance achievable from a given architecture.

#### IV. CONCLUSIONS

In this paper we have introduced a novel methodology to take into account the nonlinearity effects introduced by charge injection in MOS sampling switches in SC sigma-delta modulators. The proposed approach extends current methods and gives results directly in terms of distortion parameters (i.e. SDR, SNDR). We implemented this approach in SIMULINK. Although only a 2<sup>nd</sup> order  $\Sigma\Delta$  modulator has been analyzed, the model is applicable to any kind of architecture. Finally, the model presented in this paper allows us to carefully predict, at the behavioral level, the performance of the real modulator.

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