# CLOSE-IN SPURS IN DIGITAL RECEIVER

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**Abstract** – In the paper, the importance of the purity of ADC clock is discussed. The clock signal may be contaminated with the spur sidebands or the phase noise. These imperfections are transferred to the acquired data.

**Keywords** – jitter, 50/60 Hz spurious, non-uniform sampling

## I. INTRODUCTION

The parameters of digital receivers have become quite competitive to the traditional analog radio architecture in the past few years, as the A/D converters (ADC) have been improved considerably. Until now, the dynamic range of ADC was the limiting factor of digital receiver. Now it seems, that the dynamic range of front-end amplifier, the quality of the sample-clock source and distribution and the proper system design become increasingly important. The digital receiver substitutes classical radio parts as mixers and filters by ADC and digital signal processor (DSP). In digital receiver, all the frequencies of the analog signals are quite distant from low-frequency interference, such as 50-Hz (or 60-Hz) power-net signals. It can cause that designers tend to neglect its impact. But, if the goal of digital receiver is to acquire the narrow-band signal with high dynamic range (100 dB), the 50-Hz related close-in interference may significantly contaminate the digitised signal. Another serious close-in interference is the phase noise. Both types of these imperfections are transferred from the ADC clock signal to the resulting (acquired) signal.

## II. SPECTRUM OF FM SIGNAL

The main origin of 50-Hz related disruption is the parasitic argument modulation of the sample clock signal. The interference signal applied on the clock source, mostly the crystal oscillator (XO), results in the frequency modulation. The harmonic signal with frequency $f_0$ modulated by another harmonic signal with frequency $f_m$ is described as:

$$v_s = A \cdot \cos\left[2\pi\left(f_0 + \Delta f \cdot \cos(2\pi\ f_m t)\right)t\right], \qquad (1)$$

where $\Delta f$ is the parasitic frequency deviation. The same signal can be expressed by means of phase modulation:

$$v_s = A \cdot \cos\left[2\pi f_0 t + m \cdot \sin(2\pi\ f_m t)\right], \qquad (2)$$

where $m=\Delta f/f_m$ is the modulation index. It's assumed that parasitic modulation is small ($m<<1$). The spectrum of such phase modulated signal is well described by means of Bessel functions. The spectral components related to Bessel coefficients of orders greater than 1 can be neglected due to small modulation index. Thus the spectrum of a real sampling (or mixing) signal contains just the carrier and two sidebands, whose amplitude related to carrier expressed in decibels is:

$$A_{FM} = 20\log\left(\frac{m}{2}\right) \qquad (3)$$

and their frequency is $f_0 \pm f_m$. Note, that for a random modulating signal inducing the phase jitter (rms) of $\theta j_{rms} = m/\sqrt{2}$, $A_{FM}$ represents the single-sideband noise-to-carrier ratio.

## III. ADC VERSUS MIXER

In a digital receiver, one or more mixers are replaced by ADC, which usually works in the undersampling mode. Likewise, the local oscillator (LO) for mixing is replaced by the clock signal for sampling. Therefore, the demands for the LO purity are generally expected to be valid for the sample clock and it is recommended to treat the sample clock signals as the analog input signals while designing the system and the printed circuit board (PCB).

However, the demands on the clock purity are in texts quantified only by means of random timing jitter $\Delta t_j$, which limits the signal-to-noise ratio (SNR) to [2]:

$$SNR_j = -20\log\left(2\pi\ f_{IN}\ \Delta t_j\right), \qquad (4)$$

where $f_{IN}$ is frequency of the input signal. The frequency spectrum of jitter is considered as a white noise. But in reality the power spectrum of the jitter is not constant - the spectrum of the phase noise is not flat and also some deterministic signals may be there.

Let's have ideally sampled signal with sampling period $T$:

$$s_{s1}(t) = \sum_i s(t) \cdot \delta(t - iT). \qquad (5)$$

In [1,2], the sampling process is described as the multiplication of the clock and input signal in time domain and the convolution in frequency domain. But it is not quite exact. The simple convolution would be valid only in the case, when the spectrum is measured on the output of the ideal D/A converter, which converts the digitised signal back to analog domain while using the same clock as the ADC. In this case, the sampled signal is:

$$s_{s2}(t) = \sum_i s(t) \cdot \delta(t - iT - t_j(t)), \qquad (6)$$

where $t_j$ is the time jitter.

Otherwise, the non-equidistant (non-uniform) acquired samples are considered as ideally equidistant. During this so created time alignment the convolution-based disruption of resulting signal is amplified (or rejected) proportionally to the input signal frequency. This is the case of all real acquisition systems:

$$s_{s3}(t) = \sum_i s(t + t_j(t)) \cdot \delta(t - iT), \qquad (7)$$

Fourier spectrum of signals like (5-7) is evaluated in [3], where more cases of DAC with non-uniform sampling is solved in general form. Although not presented in [3], it can be demonstrated that the parasitic sidebands of sampling signal (spurious or phase noise) caused by the time jitter $t_j$ in signal (7) are amplified in output signal by $\Delta$ dB:

$$\Delta = 20 \log\left(\frac{f_{IN}}{f_S}\right), \qquad (8)$$

where $f_{IN}$ and $f_S$ are input and sampling frequency.

Practical consequence of this rule is demonstrated in Figure 1.

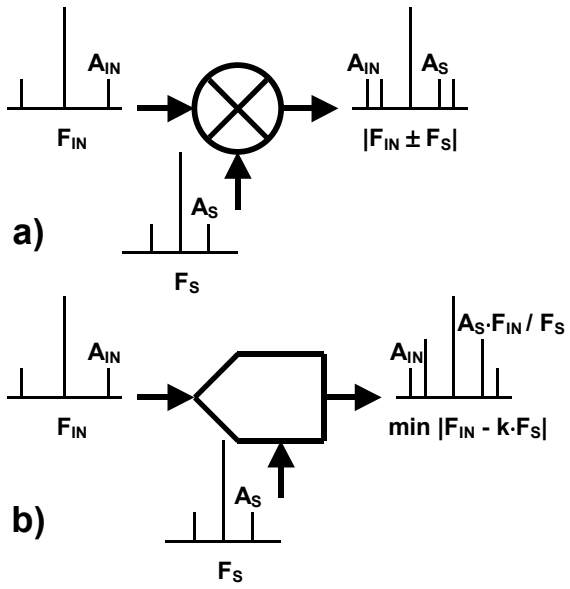



Fig. 1. Sensitivity of mixer **a)** and ADC **b)** to parasitic argument modulation of local oscillator / sample clock ($F_S$). $F_{IN}$ is frequency of input signal, $A_{IN}$ and $A_S$ are relative amplitudes of parasitic sidebands.

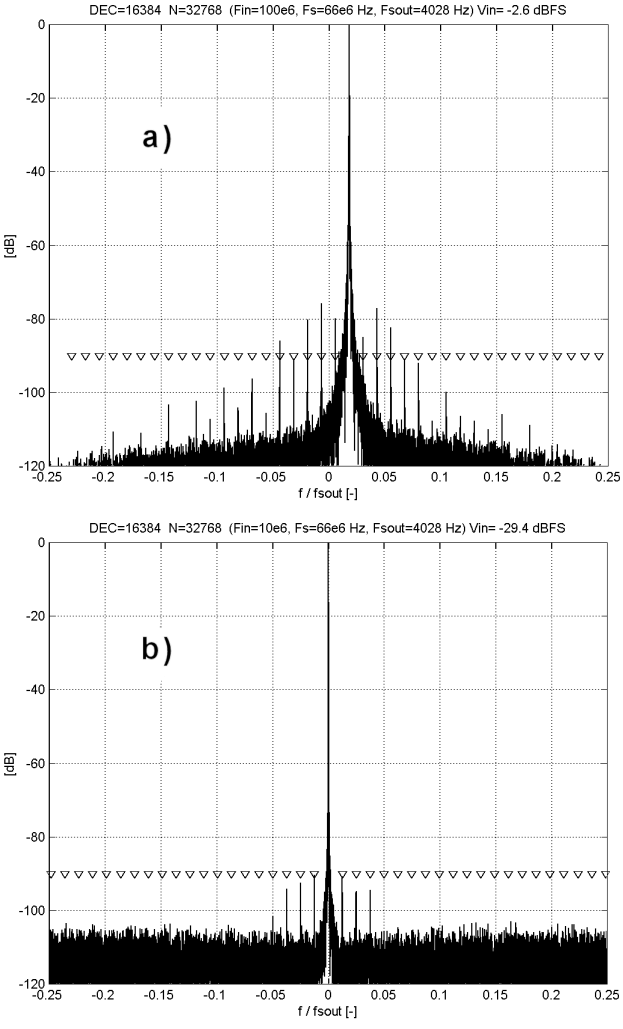
The rule is valid only for the clock parasitic sidebands induced by an argument modulation, because the ideal ADC is insensitive to the amplitude modulation of the clock.

## IV. Experimental Results

The n x 50 Hz modulation spurs and the phase noise amplification were observed during the measurement on our digital receiver [4], which was built for NMR application and ADC testing. The two-channel receiver is based on 14-bit ADC AD6644 and the digital-down-converter (DDC) AD6620, which digitally converts the band of interest to the base-band and decimate sample rate. The decimated signal is transferred to PC for further processing.

### *A. Sampling Clock with Spurs*

The modulation spurs were observed on acquired harmonic signal, when narrow-band was picked by DDC. Three different sources of those parasites were recognized (Fig. 2): the insufficient purity of the signal generator, the ripple of the power supply and the ground loops.



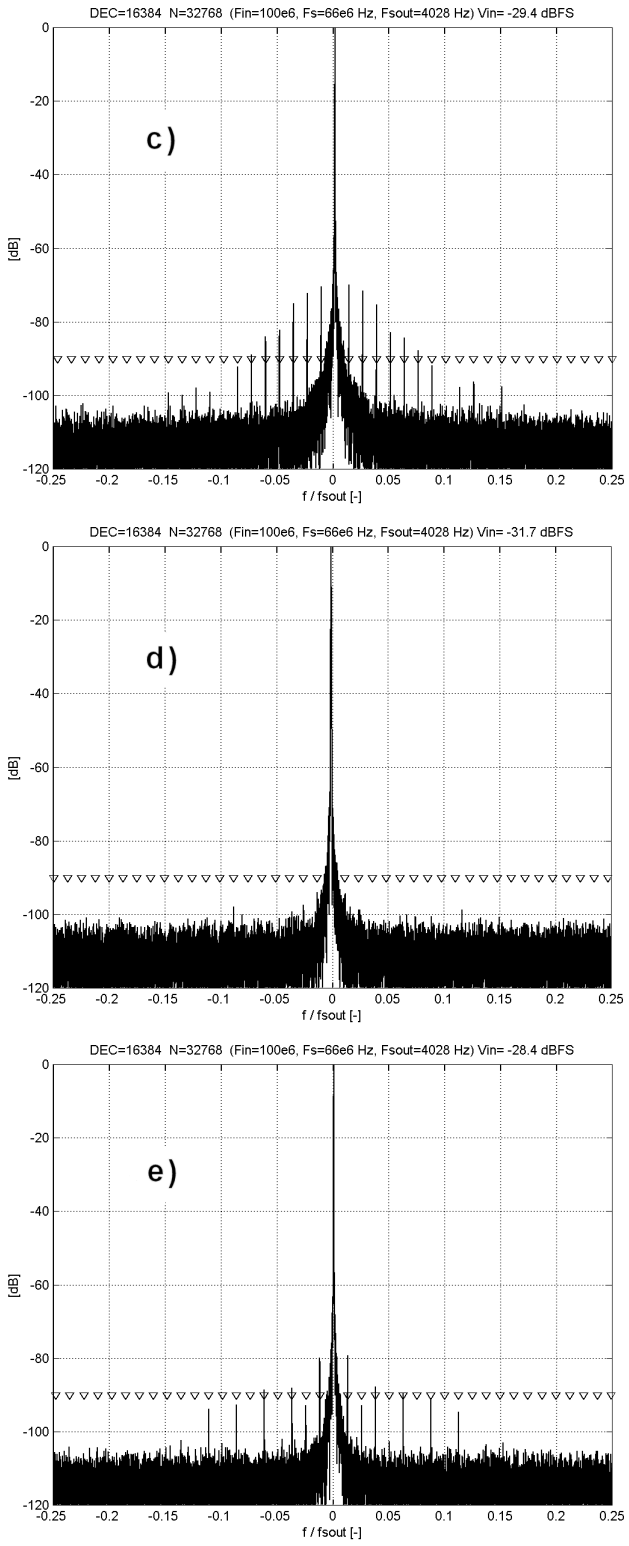



Fig. 2. Harmonic signals measured by digital receiver. a) PTS generator $f_0$ = 100 MHz; Good reference signals b) $f_0$ = 10 MHz; c) $f_0$ = 100 MHz; d) Excelent power supply, good refernce signal $f_0$ = 100 MHz; e) the same as d), but with ground loop. Symbols '∇' represent n x 50 Hz frequency offsets.

The first limiting factor of the digital receiver tests is lack of sufficiently pure input signal. A common, good RF generator (PTS, Anritsu) has specified spurious related to power about -80 to -40 dBc.

The second limiting factor is the limited purity of the sample clock. In our design, the source of clock signal is an onboard crystal oscillator or an external source. The clock signal produced by the onboard oscillator is modulated by ripple of the power supply. The static sensitivity of the oscillator to the power supply ripple was measured about 300 Hz/V. The ripple of the power supply was about 0.1 mV. The resulting frequency deviation of 30 mHz induces the parasitic side-band spurs of the clock of about -70 dBc (3). The spurs are further amplified (Fig. 2c) by the input-to-sampling frequency ratio (8) of about 4 dB. Note the spur side-band rejection of about 16 dB in Figure 2b due to low input frequency (8).

During all measurements except Fig. 2e the devices (receiver power supply, generator, PC) were plugged to the same power net outlet. Whenever one of the devices was plugged to a different branch of power supply net, the sidebands were picked-up (Fig. 2e) because of a ripple induced from a ground loop.

### *B. Sampling Clock with Phase Noise*

In order to test the influence of the clock phase noise on resulting sampled signal, we generated the sample clock signal with excessive phase noise by means of a phase modulator and a noise generator. The spectrum of this clock measured by the digital receiver with the pure sampling clock of 66 MHz can be seen in Figure 3b. The phase noise at 500 kHz offset was emphasized by means of a filter for clarity of the test. Note the small asymmetry of lower and upper sideband. It's caused by the amplitude and phase modulation superposition because of the imperfect phase modulator.

Three different analog harmonic signals with frequency 10, 70 and 130 MHz were used for the test. Their spectrum measured again with the receiver and a good sample clock 66 MHz is shown in Figure 3a. The noise floor of 10 MHz signal is almost out of the figure scale.

In Figure 3c is the spectrum of the same input signals acquired by the receiver with the imperfect sampling clock signal from Figure 3b. The phase noise amplified by the input-to-sampling frequency ratio (8) is clearly visible.

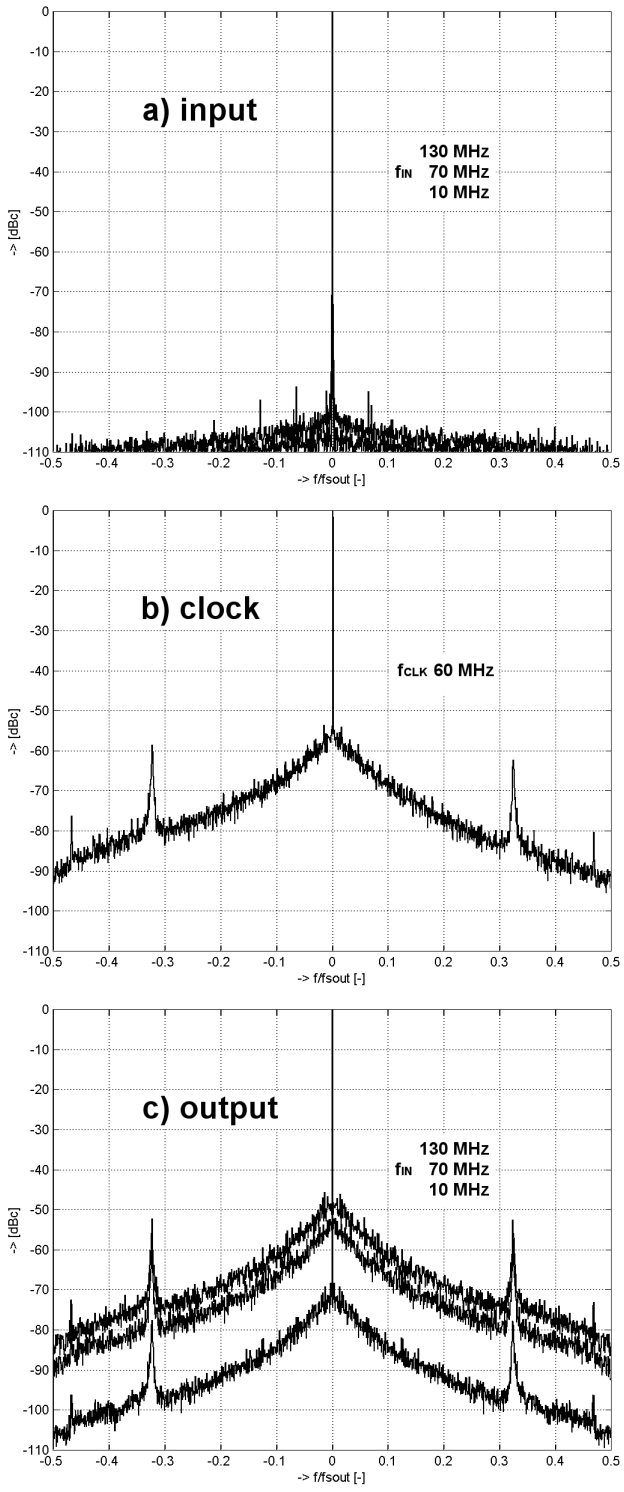



Fig. 3. a) Harmonic signals 10 MHz, 70 MHz and 130 MHz measured by digital receiver with good sample clock signal; b) sample clock signal 60 MHz with excessive phase noise measured by digital receiver with good clock signal; c) harmonic signals the same as a), but measured by digital receiver with noisy clock signal b).

[FFT 32k, bandwidth (fsout) 1.5 MHz.]

## V. Conclusions

For a wide-band acquisition system the well-known rule (4) for the SNR degradation by the jitter is useful, because the jitter with the constant spectral density (white noise) is considered. For the narrow-band high-dynamic-range system the phase noise of the sampling clock should be analysed.

The noise or spur side-bands of the sample clock is amplified by the input-to-sampling frequency ratio. This rule is important particularly in the under-sampling applications of ADC, where the mixers are substituted with ADC. Note that the similar rule is valid for the Direct Digital Synthesiser with jittered clock, the noise is amplified (in practice rejected) by the output-to-sampling frequency ratio [5].

In narrow-band application of ADC, the spurs related to power-supply net frequency (n x 50 Hz) can be a concern. With contemporary good ADC the close-in spurious-free-dynamic range can be achieved almost 100 dBc. It's not easy to test this parameter. These conditions should be fulfilled for the test: the pure signal source, the pure power supply and avoiding of a ground loop.

## VI. Acknowledgement

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