High Reliable DAQ for ADC On Line Testing

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Abstract

This paper describes a general purpose high reliable DAQ for widely used sensor families. The development of a system which allows performing fast multi-channel data acquisition and ACD testing by means of single and two tone tests grants high reliability [2].

INTRODUCTION

The problem of developing high reliable acquisition systems and cards is still an open research field. In this paper the authors propose A DAQ card architecture based on a redundant structure: three ADCs are mounted on the same card, one of the three devices is used for signal conversion while simultaneously an on-board system performs testing of the other ADCs. At the end of the test, if passed, the tested ADC is selected for acquisition, while the other two devices are available for a new test phase.
Some standard tests [1] have been implemented. In particular our attention is focussed, as suggested also by some authors [2], on the two tone test.
In order to understand the benefits introduced by the proposed solution a reliability analysis was performed. This can be achieved through different techniques. In terms of common analysis approach the authors apply a standard procedure consisting of the Flow Diagram construction, the RBD (Reliability Block Diagram) design and the reliability parameters characterization using of an universal data base on electronic devices such as the MIL-HDBK 217 FN2. The final purpose of such evaluation is to understand the performance of the proposed DAQ in terms of reliability or if the proposed solution is necessary.

DEVICE STRUCTURE

The basic idea is to develop an acquisition card able to self-test its ADC without suspending the acquisition phase. In particular three ADCs are placed on the card in redundant configuration (stand by), one performs acquisition and the other two tested in sequence (test time lower 1 s). In this way the system is able to determine whether the ADCs are properly working and consequently can be included in the acquisition process or not.
To perform this kind of operation we used the architecture shown in Figure 1.
The MUX structure has been implemented in order to obtain both a multi-channel sampling and a ADC selection tool. The samples are then collected through the PLD buffers and delivered to two blocks of 512x8 SRAM by “ping-pong” strategy. Data are then processed by a microcontroller (Hitachi – H8S2345) that generates also the test waveforms by means of the two external 12 bit D/A converters. The ADC used in the system are 8 bit AD1175 half-flash converters with a maximum sample rate of 20MS/s.

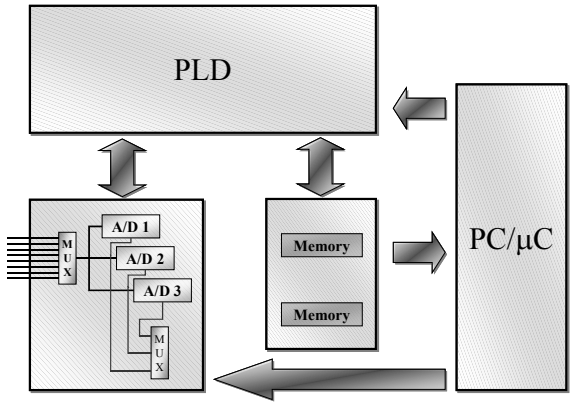

Figure 1. DAQ basic structure.

As said before the implemented tests are based on the single and two tones approaches; the last one is widely used in communication application to measure intermodulation products. The test consists in applying the sum of two sinusoidal signals of frequencies f1 and f2 (*y(t)*) allowing to test the ADC performance both as a function of the signal amplitude and slope. This kind of approach is able to provide a good coverage of the phase plain, once the proper signal frequencies have been selected. In particular the two tones signal general expression is the following:

$$y(t) = \frac{A}{2}\left(\sin\left(2\pi f_1 t + \Phi_1\right) + \sin\left(2\pi f_2 t + \Phi_2\right)\right) = x_1 + x_2 \qquad (1)$$

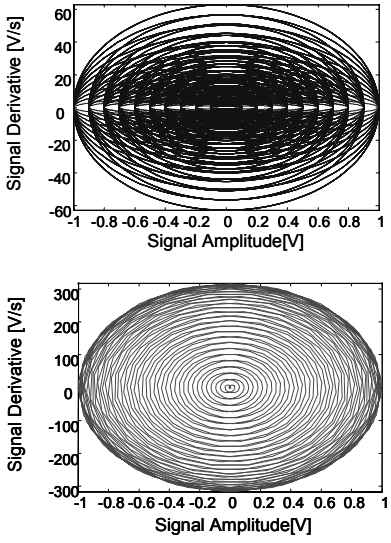

Figure 2. Phase plane covering with single sine (multi frquency) and two tone signal respectively.

The probability density function *(pdf)* of y can be expressed as:

$$pdf = \frac{1}{\pi^2}\int_{-\frac{A}{2}}^{\frac{A}{2}} \frac{1}{\sqrt{\frac{A^2}{4} - \left(y - x_2\right)^2}} \frac{1}{\sqrt{\frac{A^2}{4} - x_2^{\,2}}} dx_2 \qquad (2)$$

In figure 2 it is possible to observe how by means of the signal expressed in (2) it is possible to cover the whole signal phase plane. Moreover, in figure 3, the normalized histogram corresponding to the two tones signal is shown.

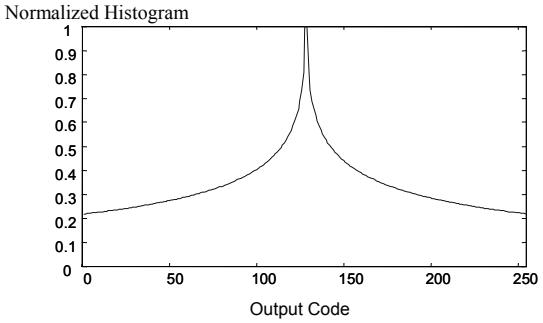

Figure 3. Two tone normalized Histogram.

In order to use in a simple and comparable manner the results coming from the two tone test the following expression for the DNL and INL parameter were derived:

$$pseudo\_DNL[k] = \frac{h_i[k] - h_r[k]}{h_r[k]} \qquad (3)$$

$$pseudo\_INL[k] = \sum_{i=0}^{k} pseudo\_DNL[i]. \qquad (4)$$

In (3) $h_i[k]$, $h_r[k]$ represent the ideal and the real (acquired) histogram value of the k^{th} code respectively. In particular expression (3) and (4) represent an approximation of the exact solution for DNL and INL as in the traditional histogram test.

EXPERIMENTAL DATA

To design the test section of the proposed DAQ, we used a flexible PC-based development system, that allows to generate test signal with an external signal generator (HP 33250A), read the test memories and transfer data to a PC for the processing. This allowed to perform some preliminary tests and to select the test system parameters, i.e. test signal frequencies, number

of acquired samples etc…Some of the results obtained with the development system, by applying both two tone and single tone tests are presented hereafter.

The DNL and the INL behaviors, obtained with a test frequency of 1.50003 kHz, are shown in figure 4 and figure 5. The peak periodicity in the DNL and INL are due to the half flash inner structure of the converter.

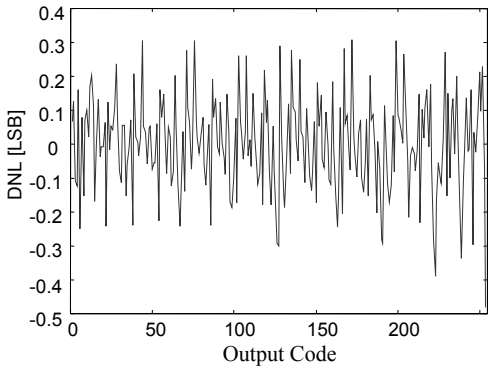

Figure 4. DNL for Traditional Histogram Test.

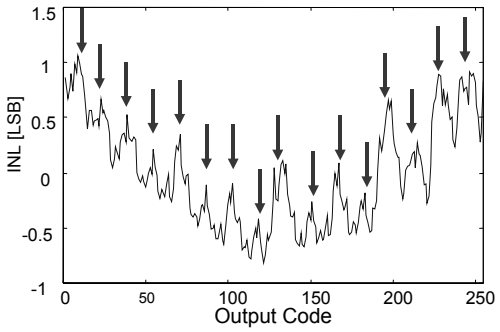

Figure 5. INL for Traditional Histogram Test.

In table 1 the summary of the single tone test signal frequencies is displayed with both the INL and the DNL parameters that are compared with the device specification.

From the results it can be seen that the DNL supplier constraints are well kept in range, while INL changes with frequency. So we decide to perform single tone histogram test at a frequency of 6 kHz, and to reject devices that does not respect the producer specifications.

	f_s [kHz]	$\|INL\|_{max}$ [LSB]	$\|DNL\|_{max}$ [LSB]
Test n°1	1.50003	1.41	0.65
Test n°2	6.29847	1.06	0.48
Test n°3	40.0876	1.62	0.74
data-sheet	**-**	**1.3**	**0.75**

Table 1. Summary of input signal frequency characteristics and INL and DNL Results.

In table 2 some results obtained by the two tones test are listed.

The two tones test coverage of the phase plane is shown in figure 6 for the test signal #1 (see table 2). It easy to understand that with such a signal it is possible to investigate the converter behaviour and characteristics in a wider range of conditions with respect to the single tone test.

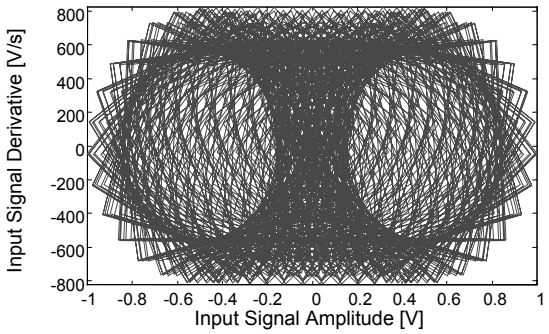

Figure 6. Two tone signal sample.

In figure 7 and 8 the pseudo_DNL and pseudo_INL are shown for the same test signal (#1).

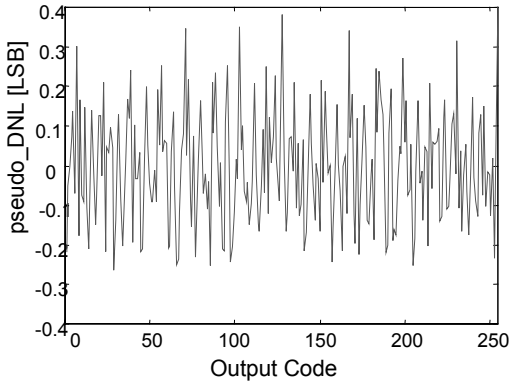

Figure 7. Pseudo_DNL for two tone signal Histogram Test.

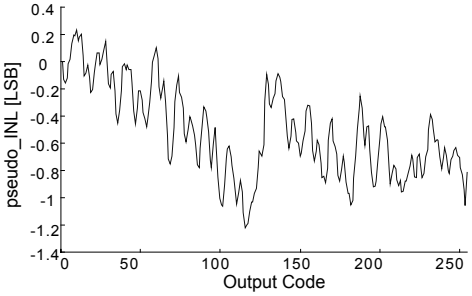

Figure 8. Pseudo_INL for two tone signal Histogram Test.

In figure 9 the INL (dashed line) and two pseudo_INL for the same ADC are compared. The continuous line plots correspond to signal #1 and test signal #2 respectively as shown in table 2. The figure shows that both tests are effective and give similar results, even if the two tones test results depend more than the single tone on the selection of the test frequency.

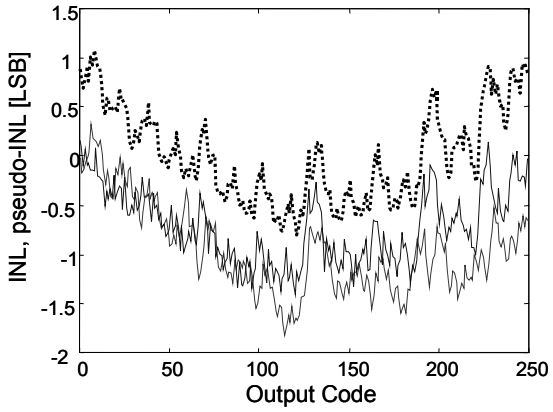

Figure 9. Comparison among the INL behaviour coming from both traditional sine signals and two tone ones.

	f_1 [kHz]	f_2 [kHz]	f_m [kHz]	*pseudo* $\lvert INL\rvert_{max}$[LSB]	*pseudo* $\lvert DNL\rvert_{max}$[LSB]
Test n°1	13.9613	0.71132	7.33632	1.13	0.47
Test n°2	49.7461	0.57621	25.1612	1.36	0.49
Test n°3	96.2271	47.0572	71.6421	2.21	0.56
data- sheet	-	-	-	**1.3**	**0.75**

Table 2. Summary of input signal frequencies characteristics for the two tone signals and INL and DNL Results.

RELIABILITY ANALYSIS

As suggested in the introduction and shown by [6], costs and the efforts to increase eletronic system reliability and availability with preventive maintenance are unbearable. So, in order to minimize the availiability the direction is to perform a quick diagnosis allowing by this way to control the system life cycle costs. The general analysis performed on our card shown the results in table 3 assuming the following hypothesis:

- Operative Temperature 23 °C;
- Operative Environment Ground Fixed (GF);
- Database MIL-HDBK-217H;
- (worst case design) Series Configuration;

Functional Block	*Failure Rate [FIT]*	*MTBF [h]*
Memories	3750.334	266643
Altera	1479.554	675879
Converter Card	2446.868	408686
ADC 1	433.478	2306921
ADC 2	383.870	2605044
ADC3	383.870	2605044
DA (AD667)	78.66	127129417
H8S2148	348.06	287310
SYSTEM	**3753.29**	**266432**

Table 3. Reliability results for the DAQ.

In table 3 we've considered that ADC1 has a different mission from the others and so it is justified the difference in terms of failure rate.

RESULTS

The authors designed a high reliable acquisition system by means of a stand by configuration on the ADC converters section. In particular in order to manage occasional ADC failure situations such as INL and DNL due to aging, the data from card are managed by a μC able to perform an histogram test and decide to jump a certain ADC on the basis of such test results.

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