Performance Analysis of PC-based Development Systems with Onboard ADCs/DACs for Digital Signal Processing Applications

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Abstract – This paper presents a general-purpose strategy to test and to compare the performances of PC-based, mixed-signal development systems for DSP applications, thus helping designers and project managers to select the best tool in terms of cost-to-performance ratio. The proposed approach, based on a simple data acquisition and signal generation design, has been implemented and validated experimentally.

Keywords – DSP development tools, FPGA, ADC, DAC.

I. Introduction

Today's Digital Signal Processing (DSP) applications require high-performance development tools that are able to cope with increasing bandwidth and real-time demands [1]. In particular, multifunctional Personal Computer (PC) development systems (e.g. PCI-based cards) provided with both mixed-signal devices (e.g. Analog-to-Digital Converters, ADCs, or Digital-to-Analog Converters, DACs) and embedded programmable resources such as Field Programmable Gate Arrays (FPGAs), are ideal tools for the rapid prototyping of involved DSP designs [2]. Unfortunately, the specifications of PC-based development tools for DSP applications, in the following referred to as PC-DSP kits, are usually insufficient to decide immediately whether a certain development system is suitable to implement efficiently a given application. In fact, not only are possible users concerned with the features of the single components embedded on the card, but they are above all interested in the overall system performances under actual operating conditions. Due to the major differences between the many PC-DSP kits available on the market, a testing strategy to compare thoroughly multiple solutions should be based on a suitable common reference design as well as on a small amount of consistent, reliable and easy-to-use performance metrics.

In this paper, after describing the characteristics of a possible reference design to be used as a benchmark application, a full explanation of the testing procedure employed to measure the PC-DSP kits' performances is provided. Finally, some experimental results validating the proposed approach are reported.

II. Description of the Reference Design

The actual performances of different PC-DSP kits can be analysed and compared only if all considered tools are stimulated by a real application under similar operating conditions. To this purpose, a different version of a common reference design chosen as a benchmark application must be implemented in each development tool on the basis of its specific characteristics. Even though the flexibility and the intrinsic re-programmability of PC-DSP kits allow the definition of various possible reference designs, all of them must be:

- *representative*, namely able to involve simultaneously all of the basic components of a given system (i.e. analogue, mixed-signal and digital devices);
- *portable* with minor modifications on a large number of different development kits;
- *easy to use* and *vendor-independent*, that is characterized by clear specifications, standard components and a simple architecture.

The specific reference design described in the following, whose block diagram is shown in Fig. 1, aims at satisfying these requirements. Practically speaking, it consists of two separate branches: a data acquisition chain and a signal generator section. The former part has been conceived to stimulate simultaneously an ADC-based input module and the onboard digital circuitry using an external test sine wave; the latter performs a dual task on an DAC-based output module by generating a sinusoid set via software. On the whole, the design is made up of:

- a First-In First-Out (FIFO) input buffer to store the *N*-bit data coming from the onboard ADC;
- a FIFO output buffer serving as a configurable lookup table to generate an *N*-bit output cyclic waveform through the DAC;

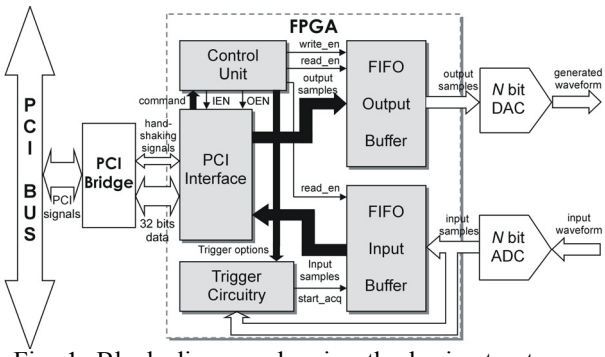

Fig. 1. Block diagram showing the basic structure of the benchmark design. The main design components and the connections between them are highlighted in grey and black, respectively.

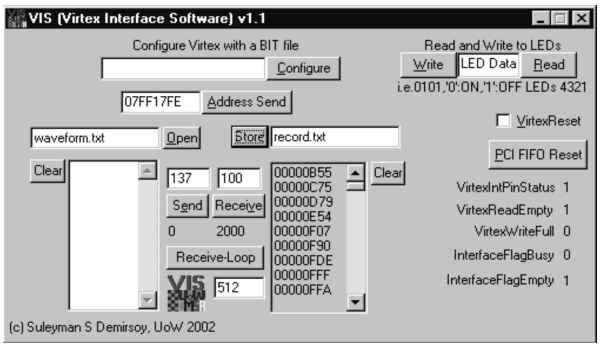

Fig. 2. Screenshot of the GUI window used to drive the benchmark application on a Virtex-based PCI card. Both data and command words are in hexadecimal format.

- a digital trigger circuitry which enables (start_acq) the data storage in the input buffer whenever the input signal reaches a pre-set level with a certain slope (trigger options);
- a general-purpose bus interface (e.g. PCI interface), possibly communicating with the main bus bridge through special handshaking signals;
- a control unit that receives and decodes the command sent over the bus, coordinates various functional sections, enables/disables the input-output operations of the bus interface (IEN, OEN) and drives the writing and reading signals to the memory (write_en, read_en).

In order to foster the applicability of the benchmark to different systems, a limited amount of memory has been employed in the implementation. As a rule of thumb, some kilobytes per each buffer seem to be a reasonable value as this is the minimum amount of memory which is available on most PC-DSP kits. The hardware part of the reference design shown in Fig.1 is managed at a high-level by means of a software Graphical User's Interface (GUI) that relies on the C++ driver functions usually supplied by PC-DSP kits' manufacturers in the form of dynamic link libraries (*dll*). Given that the implementation of the management software depends on the particular family of development systems considered, its complexity has to be kept as low as possible. Accordingly, the software tool has to carry out only three basic operations: reading and saving in a file the data temporarily stored in the input buffer; transferring the software-generated waveform samples into the output buffer and, finally, sending configuration commands to the control unit (e.g. trigger options and data acquisition or signal generation parameters). An exemplificative screenshot of a graphical software interface enabling the configuration and management of an FPGA-based design is shown in Fig. 2.

III. THE TESTING PROCEDURE

Despite the considerable complexity and internal heterogeneity of different DSP development systems, PC-DSP kits' performances can be expressed summarily in terms of processing accuracy and real-time data transfer speed. The performance metrics related to both aspects can be measured using a two-stage procedure applied to the design described in the previous section. For space reasons, in the rest of this paper only the data acquisition chain will be tested. In fact, the performance analysis of the signal generation branch is perfectly dual, i.e. it is based on the same parameters.

A. Accuracy testing of a PC-DSP kit

By generalizing the research results related to ADC testing criteria, the overall accuracy performance of a data acquisition chain can be determined using different techniques in the time-, frequency- and amplitude-domains [3-4]. Among them, frequency-based methods tend to be preferred in manufacturing [5]. In fact, various significant figures of merit such as signal-to-noise and distortion ratio (*SINAD*), signal-to-noise ratio (*SNR*), spurious free dynamic range (*SFDR*) and total harmonic distortion (*THD*) can be estimated quickly and effectively by processing small records of sinusoidal samples (e.g. 2-8 ksamples) with Fast Fourier Transform (FFT) algorithms. In testing PC-DSP kits, one of the spectral metric that provides most information about the accuracy of the whole acquisition chain is the *SINAD*, which is referred to as:

$$SINAD = \frac{\sigma_{X_1}^2}{\sigma_R^2 + \sigma_H^2 + \sigma_S^2}, \qquad (1)$$

where $\sigma_{X_1}^2$ is the power of the sine wave fundamental tone, σ_R^2 is the power of the wide-band random noise, while σ_H^2 and σ_S^2 are the powers of harmonics and spurious tones, respectively. An equivalent accuracy index expressing the connection between the analogue and the digital domain more clearly is the so-called effective number of bits (*ENOB*) that, under the assumption of a sinusoidal input waveform, is defined as [4]:

$$ENOB = \frac{10\log_{10} SINAD - 1.76}{6.02}. \qquad (2)$$

Using the benchmark application described in section II, *SINAD* and *ENOB* can be estimated from (1) and (2), respectively, by processing in the frequency-domain a certain amount of acquired data records. Each record is made up of high-accuracy sinusoidal samples which are stored into the input FIFO buffer as soon as a certain trigger condition set via software is met. The peak-to-peak amplitude of the test sinusoid should be chosen equal to the maximum value able to stimulate thoroughly the converter quantization levels without causing ADC overloading. When the input buffer is full, the samples are transferred into the PC's main memory so that they can be saved in a file. The previous steps are repeated R times until a given total amount N_T of samples is acquired. In order to stimulate all the ADC levels at least once, N_T should be a power of two satisfying the condition $RM \geq N_T > \pi 2^N$, where N and M are the ADC nominal resolution and the memory buffer size, respectively. After collecting data, the *SINAD* of the whole acquisition chain can be efficiently estimated using a robust algorithm, based on non-coherent sampling, that relies on the automatic selection of the optimal window minimizing the effect of spectral leakage [6]. In fact, as explained in [7], the spectrum of the acquired sequence of samples can be divided into independent sets of frequency bins indicated with B_R, for the wide-band noise, and with B_{X_i}, $i = 1 \ldots L$, for the L narrow-band components associated with the fundamental tone, the H harmonics and the S spurious tones, respectively (i.e. $L=H+S+1$). By referring to $|Y[\cdot]|$ as the module of the Discrete Fourier Transform (DFT) of the windowed data samples, the power estimators of the wide-band noise and the i-th narrow-band component are given by:

$$\hat{\sigma}_R^2 = \frac{1}{M \cdot N_R \sum_{n=0}^{M-1} w_{opt}^2[n]} \sum_{k \in B_R} |Y[k]|^2 \qquad (3)$$

$$\hat{\sigma}_{X_i}^2 = \frac{2}{M \sum_{n=0}^{M-1} w_{opt}^2[n]} \sum_{k \in B_i} |Y[k]|^2 - 2\frac{N_{X_i}}{M}\hat{\sigma}_R^2 \qquad (4)$$

where N_{X_i} and N_R are the number of DFT samples in each B_{X_i}, $i = 1 \ldots L$, and in B_R, respectively, while $w_{opt}[m]$, $m=0 \ldots M-1$, are the coefficients of the optimal window based on the Dirichelet kernel as defined in [6]. If $\hat{\sigma}_H^2 = \sum_{i=2}^{H+1} \hat{\sigma}_{X_1}^2$, $\hat{\sigma}_S^2 = \sum_{i=H+2}^{S+1} \hat{\sigma}_{X_1}^2$ and $\hat{\sigma}_{X_1}^2$ are the power estimators of the harmonics, of the spurious components and of the fundamental tone, respectively, by applying (1) and substituting the result in (2), the *SINAD* and *ENOB* parameters corresponding to the given frequency value of the input sinusoid can be estimated. Note that, in order to test the PC-DSP kit completely, the test described above should be repeated at various frequencies over the whole Nyquist bandwidth or, at least, in the frequency range of greatest interest.

B. Data transfer speed testing of a PC-DSP kit

Basically, the overall data transfer speed of a given PC-DSP kit can be estimated by counting the maximum number of samples N_e that can be transferred into the PC's main memory during a real-time data acquisition process of length T. Once N_e is known, the performance of the considered system can be expressed summarily by the so-called effective data rate (*EDR*), which is referred to as [8]:

$$EDR = b \cdot \frac{N_e}{T} \quad \text{[bit/s]}, \qquad (5)$$

where b is number of bits carrying useful information, namely the minimum between the data converter nominal resolution, the data path width of the onboard digital devices and the PC bus width. Since the basic purpose of this test is to assess whether the whole data transfer mechanism is slower or faster than the input sampling throughput, the real-time data acquisition process must be continuous. This means that the input samples, whose number K must be considerably larger than the FIFO buffer depth M, has to be transferred into the PC's main memory without stopping the acquisition process itself. From a practical point of view, if the input test signal is a stable sine wave of frequency f_0, the acquisition time interval T can be set equal to $T=J/f_0$, where J is a preset integer number of periods and f_0 should be chosen as small as possible to reduce the maximum phase uncertainty due to both quantization and digital input triggering. In the ideal case that the data sequence stored into the memory is a plain digitized version of the input sinusoid, the condition $T=J/f_0=K/f_s$ is satisfied, f_s being the sampling frequency. In practice, however, several factors such as software-related and bus latencies, clock frequency differences among various digital components and, finally, limited buffer dimensions, tend to alter the spectral content of the original signal either for a quasi-periodic loss of information in the output waveform (i.e. when the data transfer is slower than the sampling process), or for the interleaving of incorrect data between chunks of correct samples (i.e. when the data transfer is faster than the sampling process). While in the former case the period of the acquired digital waveform results to be shorter than the period of the input sine wave, in the latter, the opposite situation occurs. Accordingly, the fundamental frequency f_1 of a signal resulting from a real-time data acquisition process will be generally different from f_0, so that the apparent waveform duration will be equal to $T'=J/f_1=N_e/f_s \neq T$. Note that N_e represents the effective number of data transferred into the PC's main memory during the time interval T. Given that $N_e=J \cdot f_s/f_1$, by replacing the expression of N_e and the definition of T into (5), it results that:

$$EDR = b \cdot \frac{J \cdot f_s / f_1}{J / f_0} = b \cdot \frac{f_0}{f_1} \cdot f_s, \qquad (6)$$

where J, f_0, b and f_s are a priori known, while f_1 has to be measured. In particular, f_1 can be estimated by finding

algorithmically the frequency corresponding to the largest low-frequency peak in the DFT-based output spectrum. Observe that, due to frequency-domain sampling process and to the spectral leakage phenomena associated with any DFT computation, the number P of DFT points should be set large enough to detect the fundamental peak frequency with a resolution higher than a preset value ε_f. In order to meet this requirement and to apply an FFT algorithm, P should be chosen as the smallest power of two satisfying the condition $f_s/P \leq \varepsilon_f$.

IV. Experimental Results

The testing strategy described in section III has been applied to a Nallatech™ Ballynueys PCI card provided with an embedded Virtex™ XV300BG432 FPGA and a unipolar (0-1V), 12-bit ADC/DAC module running at 20 MHz. The reference design implemented in the Virtex™ FPGA runs at 40 MHz and contains two 12-bit wide FIFO buffers of 2 kilowords each. According to the mapping report, the whole design exploits 19% of the Configurable Logic Blocks (CLBs) and 93% of the Block RAMs (BRAMs) integrated in the FPGA. The accuracy test of the board has been carried out on R=100 records. Each record consists of M=2 kSa of a low-distortion 200 kHz sinusoidal signal produced by a Stanford Research DS360 function generator, after setting an amplitude value A=0.47 V. Due to the converter unipolar nature, a 0.5 V offset has been also superimposed to the input sine wave. Using the procedure described in section III.A, it results that the average *SINAD* of the system is equal to 55.32 dB (*ENOB*=8.9) with a standard deviation of about 0.47 dB. The DFT-based average spectrum calculated over all records is displayed in Fig. 3. By comparing such spectra with those reported in the Burr-Brown ADS805U ADC specifications (which is the onboard ADC) it is clear that the effective resolution of the whole data acquisition chain is roughly 12 dB lower than what expected. This is due to the influence of many parasitic factors (e.g. noise caused by PC's high-frequency digital components, power supply fluctuations, input circuitry nonlinearities and, finally, sampling oscillator jitter) that can not be detected unless a test on a real-world application is carried out.

Similar consideration can be also repeated in the case of speed testing. In particular, the *EDR* mean value of the Ballynueys PCI card has been estimated by averaging the results associated with 15 continuous acquisitions consisting of 16384 samples each. The number of periods J and the frequency f_0 of the test input sine wave are equal to 32 and 38.0625 kHz, respectively, while the output spectrum has been calculated over 2^{21} points, thus assuring an estimate of f_1 with a resolution of 10 Hz. Under these conditions, it results that the *EDR* mean value is equal to 10.308

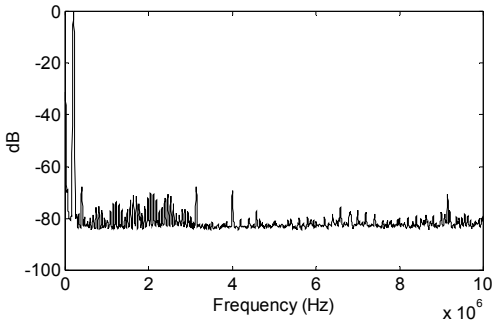

Fig. 3. Average DFT-based spectrum obtained by acquiring a 200 kHz sine wave with a Nallatech Ballynueys PCI card. Each record consists of 2 kSa of data.

MB/s (i.e. 6.872 MSa/s) with a standard deviation of about 40.7 kB/s. Therefore, the effective data rate speed of the whole acquisition chain is about 2.9 times slower than the actual sampling throughput (i.e. 30 MB/s).

Conclusions

In this paper, a testing strategy is presented to estimate univocally the performances of PC-based development systems for DSP applications provided with onboard mixed-signal devices. Such a strategy relies on the implementation of a simple reference design and it is based on a two-stage testing procedure that measures the processing accuracy and the data transfer speed of a PC-DSP kit under actual operating conditions.

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