Effects of pipelined ADC architecture and ΣΔ modulator on Digital Down Conversion

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Abstract - *The paper reports on the investigation and simulation about the influence on the Digital Down Conversion (DDC) output signal of (i) the ΣΔ modulator, (ii) the pipelined ADC architecture and (iii) some relevant non-idealities of their model such as the sampling jitter, thermal noise and finite gain of the operational amplifier. The investigation is performed in the case that the digital filters of the DDC are in accordance with the GSM mask.*
Keywords - ΣΔ ADC, pipelined ADC, Software Defined Radio.

1. Introduction

The development of an Analogue to Digital Converter (ADC) for the Software Radio (SR) solution is not feasible with the current state of the art [1]. Several converter architectures, however, are on their way to achieve high resolution at high sampling rates.

Important progress has been made in the last two years due to the availability of modern deep-submicron technologies. Two ADC architectures are very important in this context: pipelined and ΣΔ converter architectures.

The pipelined ADC architecture is capable of achieving the highest possible conversion rate, if the full flash architecture, which is only feasible for resolutions up to about 8 bit, is not taken into consideration. The resolution of a typical pipelined ADC, however, is limited to about 13–14 bit at several tens of MSample/s [2], [3]. With careful optimisation of the entire architecture as well as the individual pipeline stages both conversion speed and resolution can be increased. Furthermore, sophisticated calibration circuitry and the employment of error-correcting algorithms will further increase the achievable resolution to a 16 bit level for increased dynamic range [4].

Owing their characteristics, the pipelined ADC architecture is commonly employed in the industrial application of the Software Defined Radio (SDR) [5]. In particular, the m bit pipelined ADC digitises at Intermediate Frequency (IF) the output signal from the Radio Frequency (RF) section. Successively, the Digital Down Converter (DDC) [6] operates both the digital conversion at the base band frequency with n (n>m) bit and the canalisation process.

The ΣΔ ADC architecture which is able to provide high dynamic range and high linearity, but was confined to low input bandwidth in the past, has taken advantage of the increase in speed. Conversion rates of several MSamples/s have been reported lately [7]-[12]. The advantage of the ΣΔ ADC architecture is the high achievable dynamic range with relatively low effort, but the conversion speed is somewhat limited. The employment of new fast technologies has led to a significant increase of the achievable conversion speed of the ΣΔ ADC architecture and has promoted this architecture from a slow audio-type converter to a direct competitor of pipelined ADCs. Significant further employment of the ΣΔ ADC regards the advanced use in the analogue front ends for SDR type applications. Recently, the ΣΔ ADC architecture is employed in GSM/GPS [13] and UMTS/GSM [14] dual standard receiver for IF digitising.

The key factors assuring the large employment of the ΣΔ architecture in SDR are architectural enhancements in improving the conversion speed such as: (i) the decrease of the Over Sampling Ratio (OSR), the decrease of multi-bit loops, the cascaded loops and stability issues of high-order loops as well as optimising the bandwidth of the required operational amplifiers [13]. A further advantage is that the ΣΔ ADC architecture has the potential of lower power consumption compared with other ADCs [15]-[18].

Consequently, the ΣΔ ADC technique employed in the SDR system is a promising new scenario which brings new perspective on the process of developing the SR.

Moving from such a view, further topics of research investigation concern both architectural and hardware specifications such as: (i) the effects of the ΣΔ ADC architecture on the SDR structure, (ii) the critical parameters of the architecture as the resolution and the order of the modulator, (iii) the hardware design, (iv) the choice of the IF and the sampling rate, and (v) the power optimisation.

In the paper, the effects of both (i) the band-pass ΣΔ modulator, and (ii) the pipelined ADC architecture upon the DDC output signal in the base band frequency are investigated. At first, the effect of the noise upon the output Signal to Noise and Distortion Ratio (SINAD) is evaluated. Then most non-idealities of the ΣΔ modulator and the pipelined ADC, such as the sampling jitter, thermal noise and finite gain of the operational amplifier are taken into account and their influence upon the DDC output signal are analysed.

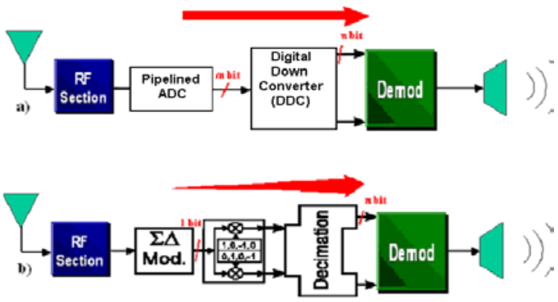


Fig.1 Block scheme of the Software Defined Radio in the case of a) pipelined ADC architecture, and b) ΣΔ modulator.

2. Basic considerations on DDC, pipelined ADC and ΣΔ modulator

Both the block schemes of Fig.1 a) and b) are taken into account, analysed and compared in order to better explore the advantages and the limits of each one.

In the block scheme of Fig.1 a) the m bit pipelined ADC architecture digitises at IF the output signal from the RF section. The m bit digital mixer of the DDC translates the signal at the base band frequencies. Successively, the multi-rate filters into the DDC operate (i) the frequency reduction and (ii) the signal shaping in accordance both to the chip-rate and mask characterizing the telecommunication standard.

In the block scheme of Fig.1 b) the one bit band-pass ΣΔ modulator digitises at IF the output signal from the RF section. The one bit digital mixer translates the signal at the base band frequencies. Successively, the decimation filter operates both the increment of the bit resolution and the signal shaping according to the mask of the selected telecommunication standard. Therefore, at the output the signal is characterized by n bit and spectrum in accordance to the selected standard.

The comparison between the two block schemes of Fig.1 a) and b) is made on the base of the output Signal to Noise and Distortion Ratio (SINAD) by imposing the same values to the following fundamental characteristics: (i) value of IF, (ii) base band frequencies of the input signal at the demodulation block, (iii) signal shaping according to the GSM standard. Moreover, the filter parameters in both the DDC and Decimation blocks are set in order to obtain the two signals characterised by equal amplitude and equal bit number.

The ADCs employed are assumed ideal and, in particular, the ideal 10 bit pipeline ADC and the one bit band-pass second order ΣΔ modulator are simulated.

2.1 The DDC filter

The DDC filter is realised by the three sections shown in the block scheme of Fig.2. The input signal is translated at the base band frequencies by means of the digital mixer.

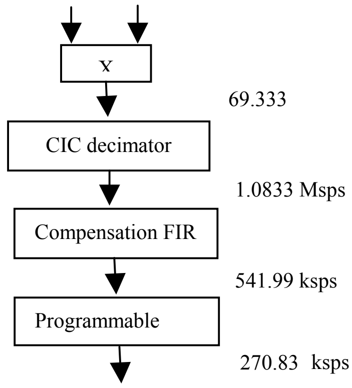


Fig.2 Decimation operates by the cascade of the CIC filter, CFIR filter and PFIR filter.

The Cascaded Integrator Comb (CIC) filter decimator is constituted by L cascaded integrator stages followed by a rate change by a factor N, and by L cascaded comb stages. The transfer function is

$$H_{CIC}(z)=\left(\sum_{n=0}^{N-1} z^{-nM}\right)^{L}, \qquad (1)$$

where: N is the decimation factor, M the differential delay and L the filter order. Then, the CIC filter is equivalent to L FIR filters, each having a rectangular impulse response. Consequently, the gain at the last comb is given by

$$G=(NM)^{L}, \qquad (2)$$

and the output bit number is

$$bit_{out}=[L\ lg_2(NM)+bit_{in}], \qquad (3)$$

where bit_{in} is the input bit number.

In the CIC Decimator filter used in the following, the input signal at the value of IF equal to 69.333 MHz is decimated by the factor N=64, with L=5 and M=1. Therefore the output is characterised by the frequency equal to 1.0833 MHz.

In both the Compensation FIR (CFIR filter) and Programmable FIR (PFIR filter), the signal is decimated by the factor 2. Therefore the output signal from the CFIR is characterised by the frequency equal to 541.99 kHz and, consequently, the output signal from the PFIR is characterised by the frequency equal to 270.83 kHz. In this manner, the over all decimation of the DDC filter is 64x2x2.

In the cascade of the three filters is operated the signal shaping according to the GSM standard. Fig.3 shows the frequency response of each of the three sections of the filters and the over all response of the cascade compared with the mask of the GSM standard.

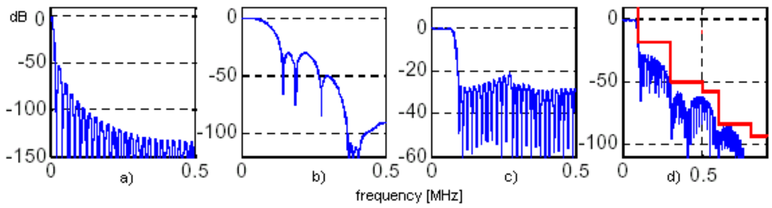


Fig.3 Frequency response of the CIC filter a), CFIR filter b), PFIR filter c) and cascade of the three previous filters compared with the GSM spectral mask d).

3. Simulation results

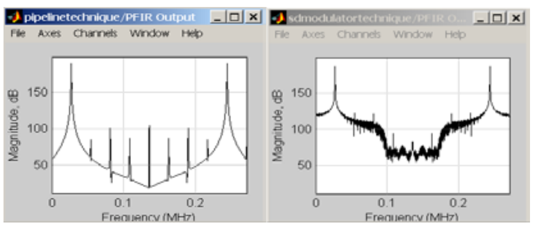
The two conversion structures shown in Fig.1 was simulated in the SIMULINK ® environment. Once is constituted by the cascade of the pipelined ADC converter and DDC. The ADC resolution is 10 bit at sampling frequency equal to 69.333 MHz. The second is constituted by the ΣΔ modulator, the one bit digital mixer and the decimation filter. The ΣΔ modulator sampling frequency is equal to 69.333 MHz. Others parameters are: (i) second order modulator, (ii) over sampling ratio equal to 4, and (iii) integrator gain equal to 1. The signal bandwidth of the two structures is according to the GSM standard.

As an example in the case that the two simulated structures are constituted by ideal blocks, the Fig. 4 compares in the frequency domain the output signals when the input signal is the modulated signal characterised by: (i) the sinusoidal carrier frequency equal to 17.333 MHz and (ii) the frequency of the sinusoidal base band signal equal to 270.833 kHz. As predicted by the theory, the Fig.4 b) highlight the noise shaping in the case of the ΣΔ modulator.

A number of simulations and tests are performed in the cases: (i) all the blocks are ideals and noise is added to the input signal, (ii) non-idealities are considered, and (iii) both the sampling jitter and noise are taken into account. In all the tests the SINAD of the output signal is evaluated.

3.1 Effect of the input noise on the SINAD

Fig.5 shows the trend of the SINAD versus the input noise variance normalised to the ADC Full Scale (FS). Both the ΣΔ modulator and the pipelined ADC are assumed ideal, the



a) b)

Fig.4 Output spectrum for the simulation of the cascade of a) the pipelined ADC and DDC, b) ΣΔ modulator and decimation filter.

noise is a wideband Gaussian. The upper curve referees to the structure employing the ΣΔ modulator, the lower to the pipelined ADC.

3.2 Effects of the non-idealities

In Fig.6 the ratio $SINAD_{id}/SINAD_{ji}$, between the $SINAD_{id}$ in the case of ideal structure and the $SINAD_{ji}$ in the case of the sampling jitter, is shown versus the percentage of the sampling jitter. This percentage is evaluated by referring to the sampling time. The upper curve referees to the structure employing the ΣΔ modulator, the lower to the pipelined ADC. It can be observed that the pipelined ADC is more sensitive than the ΣΔ modulator to the sampling jitter.

Moreover, a number of simulations and tests are performed by considering others non–idealities as the thermal noise and the amplifier gain error. By imposing variation in the range suggested by the manufactures, it can be noted that both the conversion structures show low sensitivity to these non–idealities.

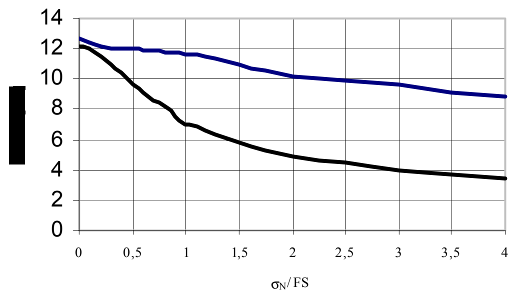


Fig.5 Trend of the SINAD versus the input noise variance σ_N in the case of the ΣΔ modulator (upper) and pipelined ADC architecture (lower).

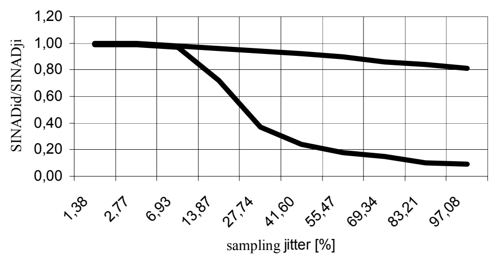


Fig.6 Trend of the ratio $SINAD_{id}/SINAD_{ji}$ versus the percentage of sampling jitter in the case of the ΣΔ modulator (upper) and pipelined ADC architecture (lower).

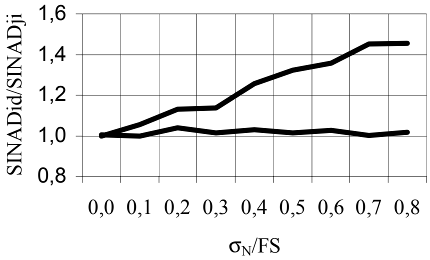


Fig.7 Trend of the ratio $SINAD_{id}/SINAD_{ji}$ versus the noise variance in the case of sampling jitter equal to 0.2ns. The upper curve referees to the ΣΔ modulator, the lower to the pipelined ADC architecture.

3.3 Effects of noise and non idealities

In Fig.7 the ratio $SINAD_{id}/SINAD_{ji}$, in the case of the sampling jitter equal to 0.2ns, is shown versus the input noise variance normalised to the FS. The upper curve referees to the structure employing the ΣΔ modulator, the lower to the pipelined ADC. It can be observed that the pipelined ADC is more sensitive than the ΣΔ modulator to the inclusive effects of the sampling jitter and the noise.

4. Conclusions

By means of simulation in SIMULINK environmental has been investigated about the influence on the Digital Down Conversion (DDC) output signal of (i) the ΣΔ modulator, (ii) the pipelined ADC architecture and (iii) some relevant non-idealities of their model such as the sampling jitter, thermal noise and finite gain of the operational amplifier. The criteria to compare the effects of the two conversion structures has been presented and discussed.
As a result, the structure employing the ΣΔ modulator outperforms that with the pipelined ADC architecture.

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