A Novel Approach for Testing and Improving the Static Accuracy of High Performance Digital-to-Analog Converters

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Abstract – This paper deals with a novel strategy to face effectively cost and complexity issues associated with the static testing of last generation digital-to-analog converters (DACs). The proposed approach is based on a high-level model that takes advantage of the basic structural features common to most high-performance DACs, thus enabling a major reduction in the total number of input test vectors. The efficiency improvement resulting from this procedure not only decreases the overall testing time, but it also promotes the design of both inexpensive Built-In Self-Test (BIST) architectures and digital self-calibration schemes.

Keywords – DAC, Integral Non-Linearity (INL), FPGA.

I. INTRODUCTION

The rapid diffusion of emerging high-performance standards for communication, measurement and entertainment purposes urges electronic device manufacturers to develop digital-to-analog converters (DACs) able to keep pace with the growing performance of Digital Signal Processing (DSP) technologies. Unfortunately, the higher the speed and accuracy requirements of a converter are, the more challenging both its design and test become. This is due not only to the scaling of transistor dimensions and supply voltages, which cause an inherent reduction in DAC static and dynamic performances, but also to the exponential growth in DAC internal complexity that mirrors in a major increment in testing time and equipment costs [1]. In order to reduce the total time necessary to carry out the static testing of a given N-bit device, parameters such as offset error, gain error, integral nonlinearity (*INL*) and differential nonlinearity (*DNL*) should be estimated by measuring the analog outputs corresponding only to a suitable subset of all possible 2^N input codes. This approach is increasingly convenient as the converter nominal resolution grows and it becomes particularly valuable when high volumes of production are considered. However, a reduction in the number of input test vectors requires the definition of appropriate mathematical models able to describe the influence of each elementary part of a given DAC architecture on its actual output voltages [2-4]. Once this data is known, the static testing efficiency can be improved by selecting only the input codes which enable the estimation of the most significant errors of the DAC characteristic. Although several published results describe interesting methods to minimize the number of input codes aimed at testing both specific device families [5] and basic DAC schemes [6-7], in this paper a more general approach is proposed and justified. In particular, after describing a new DAC model in section II, the testing procedure itself and some experimental results are reported in section III. Finally, a digital error cancellation technique to correct the DAC static characteristic is explained in section IV.

II. DESCRIPTION OF A STATIC MODEL FOR HIGH-RESOLUTION, HIGH-SPEED DACS

In spite of many technological and architectural differences, most high-performance DACs are characterized by the following common features:

- they run at sampling frequencies of hundreds of MSa/s with a nominal resolution in excess of 10 bits;
- they are usually built using submicron Complementary Metal-Oxide-Semiconductor (CMOS) processes, as this technology allows an easier integration between mixed-signal and digital components;
- their internal structure is based either on multi-bit delta-sigma solutions [8], or on appropriate combinations between the two simplest DAC basic schemes, namely the binary-weighted and the linear segmented (thermometer-encoded) topologies [9-10].

While the former solutions are preferable in many respects, the latter ones are still prevalently used in most applications. Generally speaking, combined architectures are based on the tradeoff between two contrasting requirements. In fact, on one hand, thermometer-encoded topologies show monotonic static characteristics whose maximum *INL* is usually lower than the *INL* achievable with binary-weighted schemes having the same nominal resolution. On the other, the circuital complexity of purely segmented architectures grows exponentially with the converter resolution. Accordingly, partitioning high-accuracy DACs into multiple, independent slices fosters a reduction in the overall design size, a high effective static resolution (maximum *DNL* and *INL* lower than ½ Least Significant Bit, LSB) and a significant decrease in the output glitch energy [11]. The parametric block diagram of this kind of DACs is shown in Fig.1. Such a scheme is absolutely general, i.e. independent of low-level structural or technological details, and consists of $M \leq N$ sections of

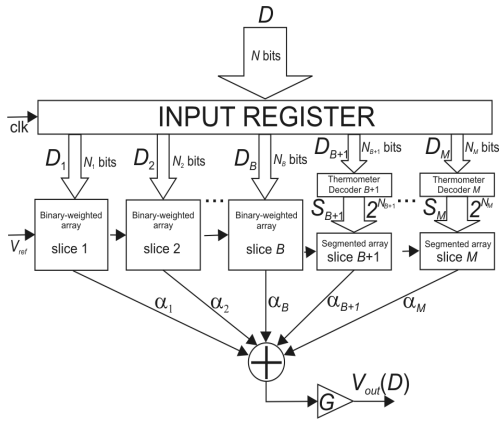

Fig. 1. General block diagram showing the structure of high accuracy DACs based on the combination of binary-weighted and thermometer-encoded sections.

N_m bits each, so that $\sum_{m=1}^{M} N_m = N$. In practical implementations, M is usually equal to 2 (single-segmented architecture) or 3 (double-segmented architecture) [9-10]. The bits belonging to the B least significant slices control binary-weighted voltage or current sources (e.g. a R-2R ladder), whereas the M-B most significant sections are thermometer-encoded (e.g. they drive an array of unit current sources). In virtue of this structure, the converter digital input code $D=(b_1 \ldots b_N)$ can be partitioned into M independent subcodes D_m, $m=1,\ldots,M$, whose binary expressions $(d_{m1} \ldots d_{mN_m})$ are given by:

$$D_m = \left(d_{m1} \ldots d_{mN_m}\right) = \left(b_{\sum_{i=1}^{m} N_{i-1}+1} \ldots b_{\sum_{i=1}^{m} N_i} \right), \; m = 1,\ldots,M \quad (1)$$

where $N_0=0$ by convention. Within the m-th binary-weighted slice ($m=1,\ldots,B$), each bit $d_{m\cdot}$ of D_m drives directly a dedicated output circuital element. Conversely, the output from each segmented section (i.e. when $m=B+1,\ldots,M$) results from the summation of the unit contributions controlled by the bits $(s_{m1} \ldots s_{m2^{N_m}})$ representing the thermometer-decoded value of the subcode D_m. Using these definitions, the ideal output voltage $V_{ideal}(\cdot)$ of the converter is given by:

$$V_{ideal}(D) = V_{ref} \cdot \left\{ \sum_{m=1}^{B} \left[\alpha_m \sum_{i=1}^{N_m} \left(\frac{d_{mi}}{2^i} \right) \right] + \sum_{m=B+1}^{M} \left[\alpha_m \sum_{j=1}^{2^{N_m}-1} \left(\frac{s_{mj}}{2^j} \right) \right] \right\} \quad (2)$$

where V_{ref} represents the DAC's reference voltage and $\alpha_m = \prod_{k=0}^{m-1} 2^{N_k}$ is a binary-weighted coefficient that expresses the significance level (i.e. the position) of the m-th slice within the considered DAC. Note that (2) does not keep into account the influence of random and systematic mismatch contributions (e.g. manufacturing process and temperature gradients) which cause offset, gain and nonlinearity errors. As a consequence, a relationship that describes more correctly the actual output voltage $V_{out}(\cdot)$ is:

$$V_{out}(D) = G \cdot V_{ideal}(D) + O + INL(D), \quad (3)$$

where G is the terminal-based gain error, O is the offset error and $INL(\cdot)$ is the integral nonlinearity as a function of the digital input code. While G and O do not affect the actual linearity of the converter and they can be easily compensated, $INL(\cdot)$ contributions can have a serious impact on the DAC characteristic. In fact, $INL(\cdot)$ depends not only on the mismatch between any individual electronic parameter and its nominal value (first-order errors) but also on the complex interactions between multiple circuital elements driven by different bits (higher-order errors) [4][6]. As the various slices of the converter shown in Fig. 1 are designed to be ideally independent of each other, it is reasonable to assume that, for any input code D, $INL(D)$ is given by the binary-weighted superimposition of the nonlinearity errors associated with each slice m when such a section is stimulated by the corresponding subcode D_m. This intuitive hypothesis is also confirmed by the mathematical proof that higher-order errors due to multi-bit circuital interactions are usually negligible [7]. Hence, if the terms ε_{mk} represent the elementary INL contributions associated with the k-th decimal input subcode of the m-th slice ($m=1,\ldots,M$ and $k=0,\ldots,2^{N_m}-1$) it results that:

$$INL(D) = \sum_{m=1}^{M} \alpha_m \sum_{k=0}^{2^{N_m}-1} \varepsilon_{mk} e_{mk}(D_m), \quad (4)$$

where the function $e_{mk}(\cdot)$ is defined by:

$$e_{mk}(D_m) = \begin{cases} 1 & \text{when } D_m = k \\ 0 & \text{otherwise} \end{cases}. \quad (5)$$

Since each slice can be considered offset-free, all terms ε_{m0} can be set equal to 0. Accordingly, the model described by (3) and (4) consists only of $\sum_{m=1}^{M} 2^{N_m} - M + 2$ unknown, independent parameters.

III. Description of the Testing Procedure

The main advantage of the model described in the previous section is that it enables a thorough test of a given DAC using only a small subset of all possible input vectors. To this aim, first of all the converter output values corresponding to the decimal codes 0 and 2^N-1 are measured to estimate $O=V_{out}(0)$ and $G=[V_{out}(2^N-1)-O]/[V_{ref}\cdot(1-2^{-N})]-1$. After that, the elementary INL contributions $\varepsilon_{\cdot\cdot}$ can be calculated from:

$$\varepsilon_{mk} = \frac{V_{out}(E_{mk}) - G \cdot V_{ideal}(E_{mk}) - O}{\alpha_m} \quad m = 1,\ldots,M;\; k = 1,\ldots,2^{N_m} \quad (6)$$

where $V_{out}(E_{mk})$ are the measured output voltages associated with the input test vectors $E_{mk}=[z_1, z_2, \ldots, D_m, \ldots, z_M]$, $D_m=k$ ranges from 1 to $2^{N_m}-1$ and z_i, $i \neq m$, represents a one-dimensional array made up of 2^{N_i} zeros. Once the parameters O, G and $\varepsilon_{\cdot\cdot}$ are known, the INL values corresponding to all the remaining input codes can be calculated simply applying (4).

Compared with the typical exhaustive testing approach,

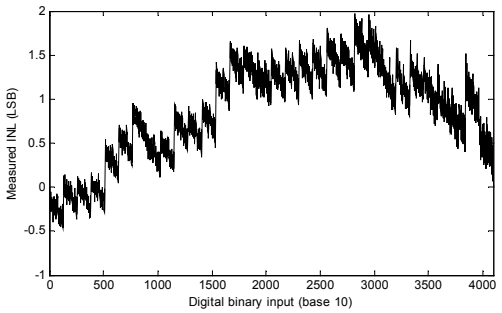

Fig. 2. Measured *INL* error pattern of a 12-bit AD9762 DAC after removing offset and terminal-based gain error.

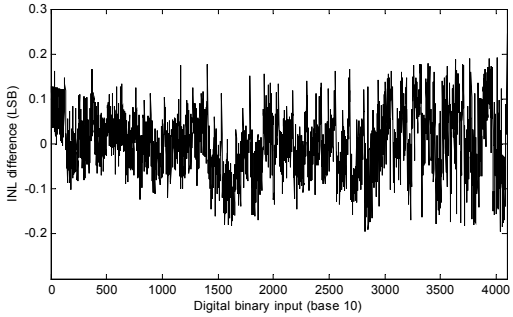

Fig. 3. Difference between the measured *INL* values and the model-based *INL* error pattern reconstructed using only 55 test vectors.

which requires the use of 2^N vectors, the relative testing time θ associated with this strategy is given by:

$$\theta = \frac{\sum_{m=1}^{M} 2^{N_m} - M + 2}{2^N}. \qquad (7)$$

Note that when the total amount of test vectors diminishes, not only θ tends to become very little, but also the code values may be stored at a low cost in small on-chip banks of memory, thus promoting the implementation of effective BIST solutions.

In Fig. 2 the measured *INL* error pattern associated with an Analog Devices™ 12-bit AD9762 DAC is shown. Since the device under test consists of a double-segmented structure with N_1=3, N_2=4 and N_3=5, only the 55 test vectors shown in Table I out of 4096 possible input codes have been employed to estimate the full *INL* pattern ($\theta \cong 1.34\%$). The point-by-point difference between the measured *INL* errors and the *INL* values estimated using the procedure described above is shown in Fig. 3. Note that the modulus of such a difference is always lower than 0.2 LSBs. As this value is smaller than the amplitude of the background noise affecting the measurements, the proposed model is validated.

IV. A DIGITAL CANCELLATION SCHEME TO IMPROVE DAC STATIC LINEARITY

Basically, the goal of any static error cancellation scheme is to compensate the effects of circuital imperfections, thus producing an actual output characteristic that is closer to the ideal one [12]. To this purpose, the nonlinear behavior associated with each input code D, for D=0…2^N–1, can be reduced by applying to the converter inputs a new code D_1 satisfying the condition $V_{out}(D_1)=G\cdot V_{ideal}(D_1)+O+INL(D_1)=V_{ideal}(D)$. If both terms of this equation are divided by V_{ref} and quantized with $L \geq N$ bits, it results that:

$$D_1^L = \left\{ D^L - \left[O^L + INL^L\left(D_1\right) \right] \right\} / G^L, \qquad (8)$$

where the superscripts L denote the finite precision with which the corresponding quantities are digitally processed before feeding the DAC input. As a rule of thumb, L should be chosen as the smallest number of bits able to keep round-off errors below a given threshold, while minimizing the cost of possible hardware implementations. Whatever L, the maximum accuracy achievable with the proposed technique is hard-limited by the DAC nominal resolution N. In fact, only the N most significant bits of D_1 become the new input to the converter, whereas the remaining L–N bits can be used either to round the value of D_1 or to feed another DAC for the fine tuning of the reference voltage V_{ref} [11]. Note that, as (8) is nonlinear, an estimate of D_1 within a preset tolerance interval should be calculated iteratively. However, since this approach is not suitable to hardware implementations, a simpler and more useful solution can be obtained under the assumption, usually satisfied in practice, that $|INL(D_1)| \ll D_1$. Thus, by neglecting the $INL(D_1)$ values in (8) and by using the D_1 estimates $\tilde{D}_1^L \cong \left(D^L - O^L\right)/G^L$ as argument of the $INL(\cdot)$ function, the equation (8) becomes:

$$D_1^L = \left\{ D^L - \left[O^L + INL^L\left(\tilde{D}_1\right) \right] \right\} / G^L. \qquad (9)$$

As the amplitude of the random noise affecting the DAC operation is usually larger than the maximum difference between $INL(D_1)$ and $INL(\tilde{D}_1)$, the approximate solutions provided by (9) can be considered sufficiently accurate for correction purposes. For instance, by assuming that the peak-to-peak amplitude of the environmental noise is about 2 mV and that V_{ref}=1 V, the previous condition is met when the DAC nominal resolution is 12 bits (i.e. 1 LSB≈244 μV). In Fig. 4, the block diagram of a digital circuit for the static correction of the 12-bit AD9762 DAC mentioned in section III is shown. The data path width L of the processing circuitry, which has been implemented in a

TABLE I. List of the input codes employed to test the 12-bit AD9762 DAC.

Test vector purpose	Test Vector Code (in decimal value)
ε_0	0
G	4095
$\varepsilon_1(\cdot)$	1, 2, 3, 4, 5, 6, 7
$\varepsilon_2(\cdot)$	8, 16, 24, 32, 40, 48, 56, 64, 72, 80, 88 , 96, 104, 112, 120
$\varepsilon_3(\cdot)$	128, 256, 384, 512, 640, 768, 896,1024, 1152, 1280, 1408, 1536,1664, 1792, 1920, 2048, 2176, 2304, 2432, 2560, 2688, 2816, 2944, 3072, 3200, 3328, 3456, 3584, 3712, 3884, 3968

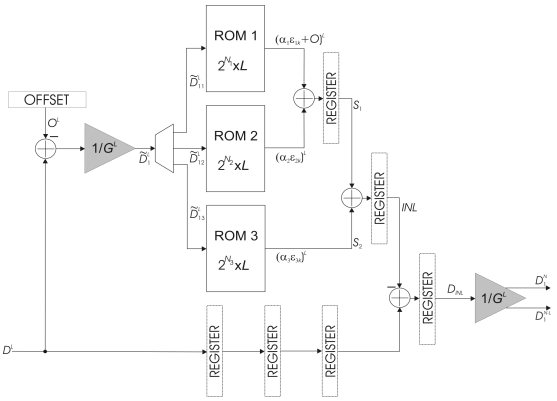

Fig. 4. Block diagram of the circuit used to improve the static linearity features of a 12-bit AD9762 DAC.

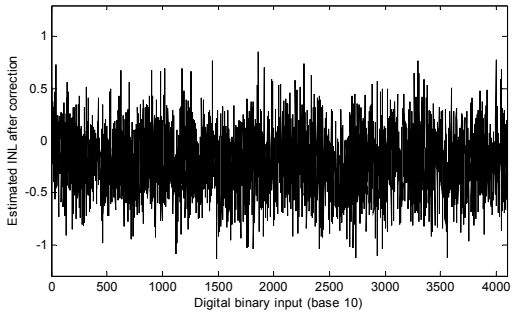

Fig. 5. *INL* error pattern of a 12-bit AD9762 DAC after the application of a 20-bit digital error cancellation scheme.

Virtex™ Field Programmable Gate Array (FPGA), is equal to 20 bits. On the whole, the design consists of four adders/subtracters; a read-only register to save the offset value O^L; three small banks of ROM to store the $\sum_{m=1}^{M} 2^{N_m} - M$ *INL* elementary contributions $(\alpha_m \varepsilon_{m\cdot})^L$ (m=1,2,3); some pipeline registers to increase the processing speed and, finally, two constant multipliers by $1/G^L$=0.6223=2549/2^{12} (shaded blocks). These multipliers have been implemented by cascading a canonic signed digit (CSD) multiplier and a barrel shift register. Note that the terms $\alpha_l \varepsilon_{l\cdot}$ are added to the offset error O before digitizing and storing the results into the first bank of memory, thus reducing the overall quantization effects. In Fig. 5 the corrected *INL* pattern of the AD9762 DAC is shown under the assumption that all measurements are affected by a zero-mean normal white noise with a standard deviation equal to 1.5 mV. Compared with the measured *INL* graph displayed in Fig. 2, not only the maximum value has been roughly halved, but also the whole pattern has considerably improved. In fact, the total *INL* power $P = \sum_{i=0}^{4095} INL^2(i)/4096$ associated with the corrected pattern is about 8.3 times lower than the original one. Consider that, as the considered circuit exploits only 10% of the FPGA resources, a self-calibration scheme based on this solution could be integrated together with the DAC on the same chip at a reasonable cost.

V. Conclusions

In this paper a model-based technique to decrease the static testing time of high-performance, multi-sliced DACs is presented. The proposed approach has been validated experimentally and it can be employed to design inexpensive digital built-in schemes for both static automatic testing and self-calibration purposes.

VI. Acknowledgments

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References

[1] A. Grochowski, D. Bhattacharya, T. R. Viswanathan, K. Laker, "Integrated Circuit Testing for Quality Assurance in Manufacturing: History, Current Status, and Future Trends," *IEEE Trans. Circ. Syst. II*, vol. 44, no. 8, Aug. 1997.

[2] A. Van den Bosh, M. Steyaert, W. Sansen, "An Accurate Statistical Yield Model for CMOS Current-Steering D/A Converters," Proc. *IEEE Int. Symp. on Circuit and Systems* (ISCAS), Geneva, Switzerland, May 28-31, 2000.

[3] P. Crippa, C. Turchetti, M. Conti, "A Statistical Methodology for the Design of High-Performance CMOS Current-Steering Digital-to-Analog Converters," *IEEE Trans. Computer-aided design of integrated Circuits and Systems*, vol. 21, no. 4, Apr. 2002.

[4] B. Vargha, J. Schoukens, Y. Rolain, "Static Nonlinearity Testing of Digital-to-Analog Converters," *IEEE Trans. Instr. and Meas*., vol. 50, no. 5, Oct. 2001.

[5] P. P. Fasang, "An optimal Method for Testing Digital to Analog Converters," Proc. *10th IEEE Inter. ASIC Conf. and Exhibit*, Portland, USA, Sep. 7-10, 1997.

[6] Analog Devices, *Analog-to-Digital conversion Handbook*, Prentice Hall, Englewood Cliffs, NJ, pp. 297-342, 1986.

[7] B. Vargha, J. Schoukens, Y. Rolain, "Using Reduced-order Models in D/A converter testing," Proc. *IEEE Instr. Meas. Tech. Conf.* (IMTC), Anchorage, USA, May 21-23, 2002.

[8] T. Kuo, K. Chen, H. Yeng, "A Wideband Sigma-Delta Modulator with Incremental Data Weighted Averaging," *IEEE Journal of Solid-State Circuits*, Vol. 37, no. 1, Jan. 2002.

[9] J. Hyde, T. Humes, C. Diorio, M. Thomas, M. Figueroa, "A floating-Gate Trimmed, 14-bit, 250 Ms/s Digital-to-Analog Converter in Standard 0.25 µm CMOS," Proc. *IEEE Symp. on VLSI Circuits*, Honolulu, USA, Jun. 2002.

[10] J. Bastos, A. M. Marques, M. S. J. Steyaert, W. Sansen, "A 12-bit Intrinsic Accuracy High-Speed CMOS DAC," IEEE Journal of Solid-State Circuits, vol. 33, no. 12, Dec. 1998.

[11] R. J. Baker, *CMOS Mixed-Signal Circuit Design*, New York, USA, IEEE Press - J. Wiley & Sons, 2002, pp. 311-342.

[12] Un-Ku Moon, G. C. Temes, J. Steensgaard, "Digital Techniques for Improving the Accuracy of Data Converters," *IEEE Communication magazine*, Vol. 37, no. 10, Oct. 1999.