Adaptive Filtering For ADC Spectral Analysis

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Abstract – In this paper, we present an adaptive filter structure for Analog to Digital Converters (ADC) spectral domain analysis. A digital filter bank is commonly used to decompose an ADC output signal into its main spectral components. However, this method requires a priori accurate knowledge of the output characteristics. It implies that a slightly deviation from the calculated resonant frequency results in a drastic decrease in the parameters estimation precision. In order to solve this problem, we propose a promising adaptive structure for a Built-In-Self-Test (BIST) approach for ADC and Mixed-Signal Integrated Circuits (IC).

Keywords – ADC Characterization, Filter Bank, Adaptive Filter.

I. Introduction

In today's competitive global market, high-technology manufacturers have made strong effort to reduce the cost, size, and power consumption of their electronic products. Traditionally, analog and digital functions have been performed on separate integrated circuits, with interconnections taking place on the board level. In the last decade, efforts have been made to implement both analog and digital circuits on the same ICs (Mixed-Signal ICs).
The result is a significant reduction in circuit-board area, size, and cost. However, this positive innovation does not come without a price. Indeed, manufacturers have found that the cost associated with high-volume production of ICs are strongly affected by their testing [1]. Until now, the semiconductor industry has been testing them mostly upon the use of sophisticated signal processing algorithms to separate errors due to the ADC from those due to the instrumentation, (fig. 1). In addition, manufacturers employ a high-speed test equipment to minimize the test duration for each ADC in the manufacturing process. Therefore, integrating the test directly into the chip has several advantages. The main aim of ADC testing is to separate the output signa sinusoids from noise. Besides that, it should estimate the Signal to Noise Ratio (SNR), the signal to noise-plus-distortion ratio ($SINAD$), the Harmonic Distortion (THD) and the number of effectif bits (n_{eff}). Many methods, like FFT or fitting algorithms, already perform those tasks but they present highly complex implementation. Digital filtering can be an alternative method. It consists in designing a system that calculates the signal spectral components [2]. The system is basically a network of second order filter where each biquad cell extracts a sinusoidal line (fundamental or harmonic) [3]. The power of sine wave components can be determined using registers, adders and multiplier. The chip control flow during the ADC test is shown in fig. 2. The main inconvenient for this method is the strong dependency of the filter bank results on the static input frequency values set at the beginning of the test. Therefore, the ADC under test has to be fed with an input signal and clock features that fulfill the filter bank characteristics. Since this is complex and not really efficient, we introduced the use of an adaptive structure to fit the filter parameters to the input frequency value.
Two main parts compose this paper. First, we remind the principle of filter bank to extract spectral parameter of ADCs and outline the influence of the input frequency value in the SINAD estimation. Then, we present the adaptive structure used to estimate the SINAD and its performances according to the input frequency value.

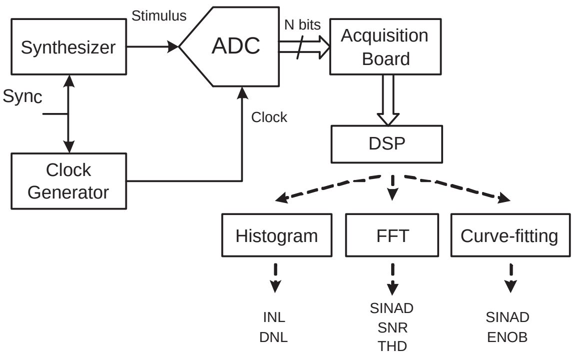

Fig. 1. Test setup for ADC testing.

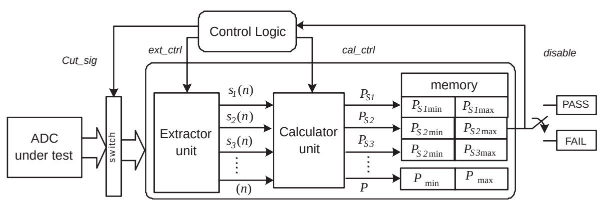

Fig. 2. The proposed test scheme.

II. The notch filter

Fig. 3 depicts the notch filter architecture based on a second order bandpass filter, which is derived from bilinearly transformed second order continuous time transfer function (fig. 4). In [4], authors present an

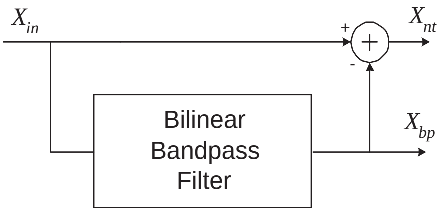

Fig. 3. The notch filter.

IIR bandpass filter that has exactly unity gain and zero phase shift at resonance. The transfer function from the input to the bandpass output is given by

$$H_{bp}(z) = \frac{-k_2}{2} \cdot \frac{(1+z^{-1})(1-z^{-1})}{1-(2-k_2-k_1^2)z^{-1}+(1-k_2)z^{-2}} \tag{1}$$

and has a peak unity gain at the resonance frequency given by

$$\omega_r = 2\sin^{-1}\left(k_1 \Big/ 2\sqrt{1-\frac{k_2}{2}}\right) \tag{2}$$

The filter pass-band width can be set through the parameter k_2 and then the desired resonance frequency is determined by the parameter k_1. The digital notch filter, presented in fig. 3, is connected to the output of the ADC as shown in fig. 2. Let $y(n)$ be the digital sequence applied to the filter input X_{in}. The signals $\hat{s}$ and $\hat{\eta}$ will denote respectively the digital outputs from the bandpass output X_{bp} and the notch output X_{nt}. The digital notch filter, presented in fig. 4, is connected to the output of the ADC as shown in fig. 3. Since the sequence $\hat{s}(n)$ emerging from the bandpass output is zero- mean, the estimated power $\hat{P}_s$ is computed as a sum of squares, given by (3) where M is the number of samples.

$$\hat{P}_s = \hat{\sigma}_s^2 = \frac{1}{M-1}\sum_{n=1}^{M}\left(\hat{s}\left(n\right)\right)^2 \tag{3}$$

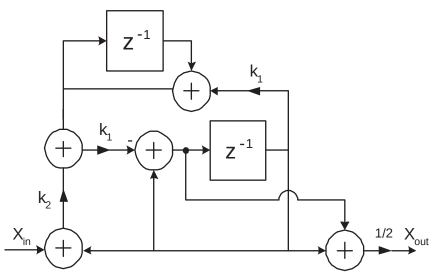

Fig. 4. The second order bandpass filter.

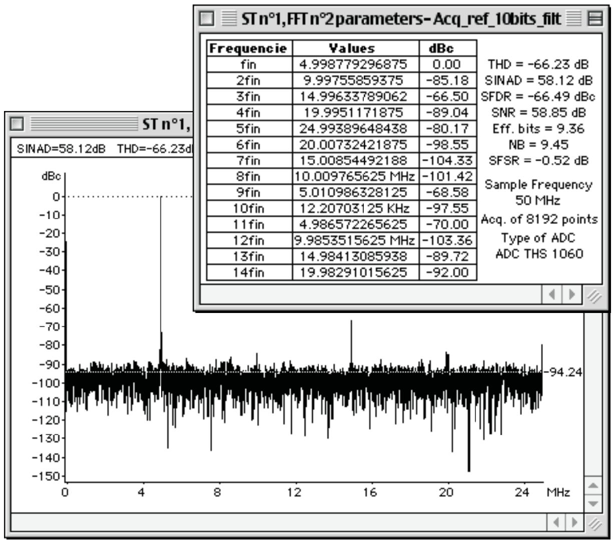

Fig. 5. Features of the ADC test setup with spectral parameters.

The sequence $\hat{\eta}(n)$ emerging from the notch output X_{nt} is not zero-mean so it variance, which is the estimated noise power $\hat{P}_\eta$, is calculated as

$$\hat{P}_\eta = \hat{\sigma}_\eta^2 = \frac{1}{M-1}\sum_{n=1}^{M}\left(\hat{\eta}\left(n\right)\right)^2 - \frac{\left(\sum_{n=1}^{M}\hat{\eta}\left(n\right)\right)^2}{M\left(M-1\right)} \tag{4}$$

From these, we can estimate the $SINAD$ from :

$$\widehat{SINAD} = 10Log_{10}\left(\frac{\hat{\sigma}_s^2}{\hat{\sigma}_\eta^2}\right) = 10Log_{10}\left(\frac{\hat{P}_s}{\hat{P}_\eta}\right) \tag{5}$$

This method has been validated with a high speed low noise $10\,bit$ CMOS pipelined ADC. It has a maximum sampling rate of $60\,MHz$. The chip (THS1060)

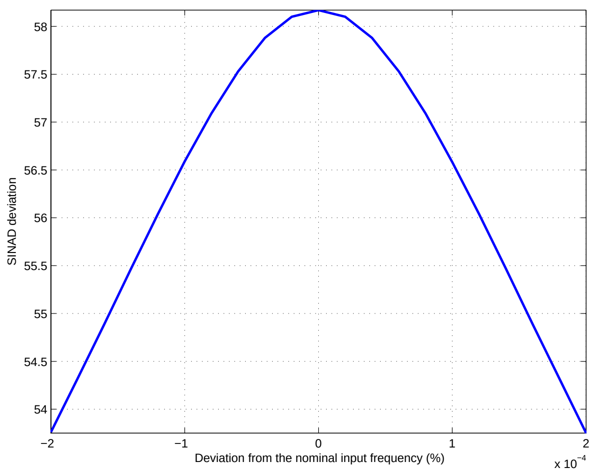

Fig. 6. Deviation of the estimated SINAD as function of the input frequency value.

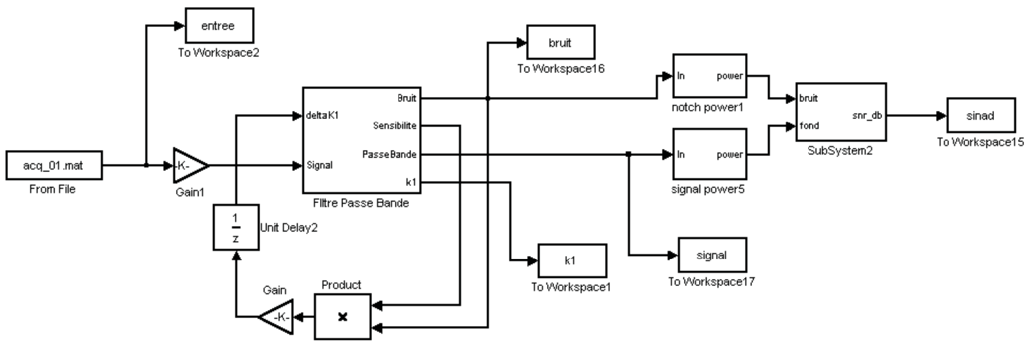

Fig. 7. SIMULINK model of the adaptive bank filter.

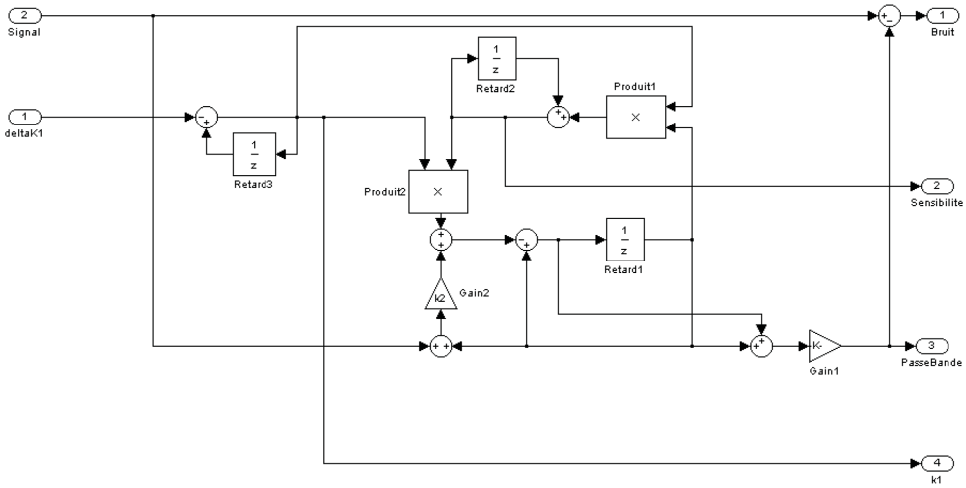

Fig. 8. SIMULINK model of the adaptive notch filter.

was a full custom proprietary of Texas Instruments design. An input signal level of $-0.5\,dB$ was chosen and the test frequency was $4.998\,MHz$ sampled at $50\,MHz$. A 8192-point signal FFT of the ADC output is shown in fig. 5. When using a SIMULINK model and the acquisition file the $SI\hat{N}AD$ is about $58.17\,dB$, which is very closed from the estimated one by FFT. The bandwidth of the notch filter was set by $k_2 = 0.00153$ leading to $k_1 = 0.61765$.

III. Adaptive filtering

A. Sensibility to Resonance Frequency

First, we have to remind the aim of the bank filter. The goal of this filter is to test quickly and accurately ADCs. Unfortunately, it is highly probable that all ADCs will not present the same resonance frequency. Therefore, some of them will be rejected as "out of range" even though they give totally acceptable results. It is obvious that the notch filter is not adapted and that it would reject the ADC because the $SINAD$ will be disastrous. The solution is to use adaptive filters to track the ADC resonance frequency to notch the the signal afterwards. Fig. 6 shows the deviation of the estimated $SINAD$ as function of the input frequency. A variation of $2e-4\%$ of the input frequency causes a decrease of $4\,dB$. These results show us the need of using adaptive filter structure.

B. Adaptive Filters

The structure shown in fig. 7 and fig. 8 represents the Adaptive Notch Filter selected for our bank filter.

The parameter k_1 is adapted following the relation:

$$k_1\,(n+1) = k_1\,(n) - \mu \times s\,(n)\,e\,(n) \qquad (6)$$

where μ is a constant set by the user, s is the filter sensibility and e is the error.
It is noteworthy to observe that the filter does not need outside help to calculate the new parameter k_1. The structure finds every term it needs for adapting k_1 at the filter outputs [2]. The performance of this structure is given from fig. 9, which shows the

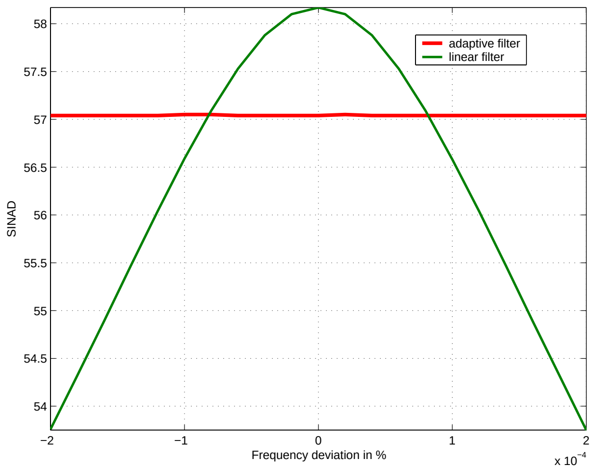

Fig. 9. Deviation of the estimated SINAD with both filter as function of the input frequency value

$SINAD$ of ADC output signal for each input frequency deviation.

IV. Conclusions

The LDI filter studied is absolutely accurate to test ADCs because it has two parameters allowing the user to set both the bandwidth and the resonance frequency. Additionally, its legitimacy domain is large enough for this application. We described the essential need of an adaptive filter, and both simulation and testing of the designed structure have given excellent results. The filter is able to track the resonance frequency far from its initial implemented value even with a very noisy signal. The parameter μ gives us the opportunity to increase the convergence speed with a respectable final resolution.
To finalize this project it is still necessary to test the bank filter, in order to cover ADCs testing. However, this structure seems to be very promising.

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