MODELING AND DESIGN OPTIMISATION FOR HIGH-RESOLUTION, HIGH-SPEED PIPELINE ADC'S

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Abstract-This paper describes a suitable mathematical model for the design of high-speed, high-resolution pipeline ADC's.

1. INTRODUCTION

Pipeline Analog-to-Digital Converters (ADC's) are widely used in many high-speed, high-resolution applications such as wireless communications because of their higher sampling rate and dynamic range. Switched-capacitor implementation in CMOS technology is more attractive than bipolar and BiCMOS ADC's for high resolution applications, but their linearity decreases when the sampling frequency is higher than few MHz. At these frequencies analog or digital calibration is commonly used for linearity enhancing.

The bit partitioning between the ADC stages and the selection of the stages that require the calibration should be made according to an appropriate model, depending on the maximum tolerable DNL, INL and noise.

This paper describes the model and the methodology followed in the design of a 14-bit, 100MS/s CMOS ADC.

2. PIPELINE ARCHITECTURE

The pipeline architecture chosen is shown in Fig. 1. Each stage consists of a sample-and-hold amplifier (SHA), a low-resolution flash ADC with $2^{N_i} - 2$ comparators, a DAC, a subtractor and a residue amplifier. The switched capacitor multiplying DAC (MDAC) drawn in Fig. 2 plays the role of SHA, DAC, subtractor and residue amplifier at the same time. The input voltage V_{INi} is sampled by the coarse sub-ADC and the MDAC at the same clock phase ϕ_1. In this phase all the 2^{N_i-1} capacitors of the MDAC are connected to V_{INi}, so that the charge at the input of the amplifier is $Q = V_{INi}C_{MDAC}$, where C_{MDAC} is the total capacitance of the MDAC. In a second phase ϕ_2 the capacitor C_0 is switched in the op-amp's feedback

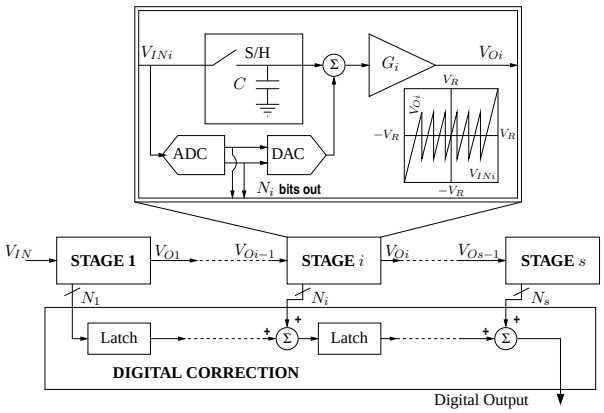

Figure 1. Pipeline ADC block diagram.

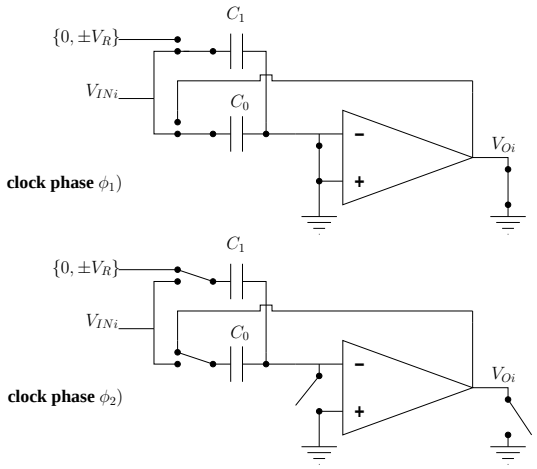

Figure 2. Simplified model of a 2-b MDAC.

loop while the other capacitors are switched to ground or $\pm V_R$ depending on the value of the input code [1], and the charge is transferred to the output. Therefore, in the

ideal case, the value of the output residue will be

$$V_{Oi} = \frac{C_{MDAC}}{C_0} V_{INi} \pm \frac{C_{sel}}{C_0} V_R \quad (1)$$

where C_{sel} is the sum of the capacitance connected to $\pm V_R$. Since all capacitors have nominally the same value C, the gain G_i of the MDAC is $C_{MDAC}/C_0 = 2^{N_i-1}$.

The pipeline ADC is susceptible to several non-idealities which can limit the resolution to 10-12 bits if calibration or trimming are not used. In particular, the finite gain and the incomplete settling of the op-amp, and the mismatch in the capacitors that set the interstage gain are the most relevant sources of nonlinearity [2], while thermal noise arises from sampling switches and op-amp [3]. The nonlinearities of the i^{th} sub-ADC, if not exceeding $2V_R/2^{N_i}$, are tolerated thanks to the digital correction. Similarly, the offset of the op-amp has a negligible effect if an offset cancellation technique is used.

3. MATHEMATICAL MODEL

3.1. DNL

Because of the incomplete settling, the finite op-amp gain and the capacitor mismatch, the residue of the generic sub-ADC becomes

$$V_{Oi} = (1-\varepsilon_S-\varepsilon_A)\left(G_i(1+\varepsilon_C)V_{INi} \pm D_i(1+\varepsilon_D)V_R\right) \quad (2)$$

where

$$\varepsilon_S = \exp(-2\pi T_S f_T/G_i) \quad (3)$$

$$\varepsilon_A = \left(1 + \frac{C_p + \sum_{k=0}^{G_i-1} C_i}{C_0 A}\right) \quad (4)$$

$$\varepsilon_C = \sum_{k=1}^{G_i-1} \frac{\Delta C_k}{G_i C} - \frac{G_i-1}{G_i}\frac{\Delta C_0}{C} \quad (5)$$

$$\varepsilon_D = \sum_{k=1}^{D_i} \frac{\Delta C_k}{D_i C} - \frac{\Delta C_0}{C} \quad (6)$$

and T_S, f_T, ΔC_k, and D_i are, respectively, the settling time, the unity gain frequency, the mismatch error of the capacitor C_k, and the number of capacitors connected to $\pm V_R$. Finally, C_p is the parasitic input capacitance of the op-amp. Therefore, the error on the sampled residue is:

$$\Delta V_{Oi} \approx (-\varepsilon_S-\varepsilon_A+\varepsilon_C)G_i V_{INi} \mp (-\varepsilon_S-\varepsilon_A+\varepsilon_D)D_i V_R \quad (7)$$

Let suppose that the i^{th} MDAC only is affected by mismatch, finite gain, and settling time errors. In this case, all the quantization cells of the final ADC will have the same width, but the cells including the thresholds of the i^{th} MDAC. It is possible to demonstrate that the DNL (in LSB) of the former cells are given by

$$DNL = \varepsilon_S + \varepsilon_A - \sum_{k=1}^{G_i-1} \frac{\Delta C_k}{G_i C} + \frac{G_i-1}{G_i}\frac{\Delta C_0}{C} \quad (8)$$

The DNL error of the cells close to the threshold of the MDAC under evaluation can be estimated from (7). Let assume, in fact, that $E_{U,J}$ and $E_{D,J}$ are the errors in the residue when the input value $V_{INi} = V_R(J-0.5)/G_i$ is approximated from the left and, respectively, from the right side. Therefore, the DNL of the cell including the threshold J of the i^{th} MDAC is given by

$$\begin{aligned} DNL_J &= (E_{U,J} - E_{D,J})\frac{2^{m_i-1}}{V_R} \\ &= 2^{m_i-1}\left[-(\varepsilon_S+\varepsilon_A) + \frac{\Delta C_J}{C} - \frac{\Delta C_0}{C}\right] \end{aligned} \quad (9)$$

where m_i is the overall resolution of the stages following the i^{th} MDAC. From (8) and (9), it is apparent that the DNL of the whole ADC reaches its maximum value close to the thresholds of the first MDAC, and the worst case DNL can be estimated to be

$$DNL_w = 2^{m_i-1}\left[-(\varepsilon_S+\varepsilon_A) - 2\frac{\Delta C}{C}\right]. \quad (10)$$

The standard deviation of the capacitor mismatch, evaluated by recalling an approximated form of the Pelgrom's law, is given by $\sigma_{\Delta C} = k_c\sqrt{C}$, where k_c is a technology dependent parameter.

3.2. INL

The INL errors corresponding to a generic quantization cell can be evaluated by summing the DNL errors of the previous cells. Assuming a positive DNL for the quantization cells (but the ones bounded by the threshold of the i^{th} MDAC), the INL is a steadily increasing function of the cell's position along the ADC characteristic, until we arrive at the threshold of the MDAC under evaluation. At this point the INL function exhibits a step, see(9)). Since it is easy to prove that the INL is maximized at one of the cells including the threshold of the involved MDAC, the analysis can be restricted to such cells. The INL of the cell corresponding to the threshold $V_{INi}/V_R = (J-0.5)/G_i$ is given by

$$\begin{aligned} INL_J &= \frac{3}{2}2^{m_i-1}(\varepsilon_S+\varepsilon_A-\varepsilon_C) + \sum_{k=J}^{G_i-1} DNL_k \\ &\quad + (G_i-J)2^{m_i-1}(\varepsilon_S+\varepsilon_A-\varepsilon_C) \end{aligned} \quad (11)$$

The worst-case INL_w can be found for $J = G_i/2$, thus leading to

$$INL_w = 2^{m_i-1}\left[\frac{\varepsilon_S+\varepsilon_A}{2} + \frac{G_i-1}{2}\frac{\Delta C}{C}\right] \quad (12)$$

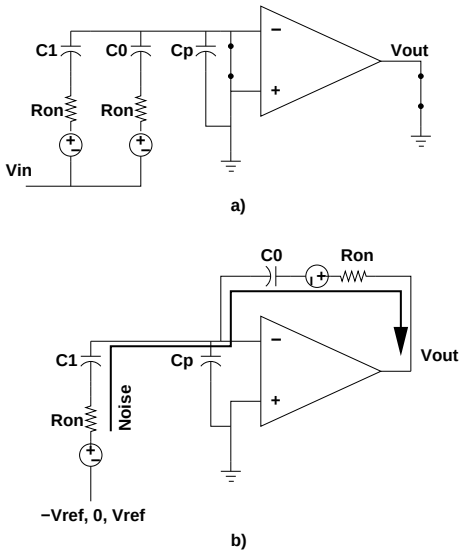

Figure 3. A simplified noise model for the MDAC.

3.3. Noise

A simplified noise model for the MDAC is reported in Fig. 3. The main noise source of the MDAC in Fig. 2 are the input-referred noise voltage of the opamp, e_{n-REF}, the thermal noise of the on-resistance of the switches, and the noise voltage contributed by the reference generator.

As referred in the Introduction, the MDAC exhibits two phases which correspond to two different circuit arrangements. The noise voltage affecting the converter's SNR is the sum of the rms noise voltage evaluated at the end of the residue amplification phase at the output of the MDAC's. As a first approximation let we assume that the noise contributions of the i^{th} MDAC in the two phases are almost independent. This assumption allows to obtain the overall MDAC noise, by superposition of the two noise power terms.

In the *sampling* phase the inputs and the output of the opamp are shorted to ground, thus the contribution of the opamp noise is negligible in this phase. On the contrary, the thermal noise of the on-resistance of the switches is integrated by the total MDAC capacitance, $C_{tot} = G_i C_0$, at the bottom-plate terminal of the capacitors [3], Fig. 3-a,

$$v_{nS-IN} = \sqrt{\frac{kT}{C_{tot}}} \tag{13}$$

At the transition from the *sampling* to the *residue amplification* phase, v_{nS-IN} is sampled and transferred to the opamp output, leading to the noise contribution from the sampling phase, v_{nS}, equal to:

$$v_{nS} = G_i v_{nS-IN} = \sqrt{\frac{G_i kT}{C_0}}\,. \tag{14}$$

Notice that the opamp input capacitance, C_p, does not contribute to the overall noise, the input terminals being shorted to ground.

During the *residue amplification* phase, Fig. 3-b, a voltage feedback is established and both the thermal noise voltage due to the switches and the input opamp noise are transferred to the output and their spectra are shaped by the transfer-function of the amplifier. Assuming a single-stage opamp and considering the feedback factor in the circuit of fig. 3-b, $H_r = 1/G_i$, the noise bandwidth of the amplifier is given by

$$B_{eq} \approx \frac{\pi}{2}\frac{g_m}{2\pi\, C_L\, G_i} \tag{15}$$

g_m being the transconductance of the input pair and C_L is the overall loading capacitance of the opamp in this phase.

$$C_L = \frac{(G_i - 1)C_0 + C_p}{G_i + \frac{C_p}{C_0}} + C_{MDAC} + C_{ADC} \tag{16}$$

C_{MDAC} (C_{ADC}) being the input capacitance of the next MDAC stage (of the next flash ADC, respectively).

The opamp input noise is mainly contributed by the output noise current from the MOS input pair

$$i_n = \sqrt{4\gamma kT g_m B_{eq}}\,, \tag{17}$$

with γ ranging from 2/3 to 3 depending on the process and on the gate length. The input noise voltage is readily evaluated from i_n as $e_{n-OA} = i_n/g_m$. The contribution of the noisy reference generator $\pm V_R$ is modelled with an equivalent noise resistance, R_R. Therefore, the rms noise voltage at the opamp output related to the residue amplification phase is

$$v_{nRA}^2 = G_i^2 B_{eq}\left(4KTR_{ON} + 4KTR_R + \frac{4\gamma kT}{g_m}\right) \tag{18}$$

where R_{ON} is the on-resistance of the switches connecting the top plates of all the capacitors $C_1, \cdots, C_{G_i-1}$. Assuming that the switch size is scaled together with the capacitance value, $R_{ON} \approx R_{on}/\ G_i$. Finally, the overall output noise of the MDAC stage is obtained by summing the contribution related to the sampling and to the residue amplification phase [5]

$$v_{nO}^2 = \left[\frac{G_i kT}{C_0} + 4kT\,(R_{ON} + R_R)\,\frac{g_m G_i}{4C_L} + \frac{\gamma kT G_i}{C_L}\right] \tag{19}$$

4. MODEL-BASED DESIGN METHODOLOGY

In a reasonable design approach for high-resolution pipeline ADC's, the maximum allowed INL, DNL, and output noise should be evaluated at first. In order to achieve

an effective resolution higher than $N-1$ bit, where N bit is the nominal resolution, both the DNL and INL should be below 0.5 LSB and the total output noise should be well below the quantisation noise.

It has to be remarked that, commonly, the design is carried out by using a simplified relation for the DNL, without the contribution arising from the finite op-amp's gain and bandwidth [4]. Moreover, the INL contribution is not considered even though it can limit the overall linearity.

From the proposed equations (10) and (12) it is possible to see that, in order to ensure a maximum INL (DNL) less than INL_w (DNL_w, respectively), the DC gain, the unity-gain frequency of the amplifier, and the minimum value of the capacitors of the MDAC's should be

$$A \geq \frac{G_i 2^{m_i+1}}{\min\{DNL_w, INL_w\}}\ , \tag{20}$$

$$f_T \geq \frac{G_i}{2\pi T_S}((m_i+1)\ln 2 - \ln(\min\{DNL_w, INL_w\})) \tag{21}$$

and, respectively,

$$C \geq \left(k_c \Big/ \min\left\{\frac{DNL_w}{2^{m_i+1}},\ \frac{3INL_w}{(G_i-1)2^{m_i}}\right\}\right)^2 \tag{22}$$

Similarly, a different constraint on the minimum value of the sampling capacitors can be obtained from (19).

Nevertheless, while the noise contribution cannot be removed, the nonlinearities arising from capacitor mismatch and op-amp limitations can be removed by either background or foreground calibration. Therefore two lower bounds for the feedback capacitance of each stage can be determined by noise and linearity requirements. While the former should be always satisfied, the latter can be removed by digital calibration of the stage. Because of its impact in terms of silicon area and power consumption, the calibration will be introduced only when the minimum capacitance imposed by linearity requirements is larger than a threshold, that can be considered a design parameter.

5. SIMULATION RESULTS

The procedure described in the previous Section has been automated by means of a dedicated software and has been applied to the design of a 14-bit, 100 MS/s ADC. Some results for several ADC bit partitioning are reported in Fig. 4. Architectures $422\ldots23$ and $332\ldots23$ are two sub-optimal choices with respect to the ADC input capacitance (which impacts the input track-hold requirements) and the OTA requirements (load capacitance C_{MDAC} and f_T) for the first stage MDAC. Such OTA requirements can be fullfilled using a $0.18\ \mu m$ CMOS technology.

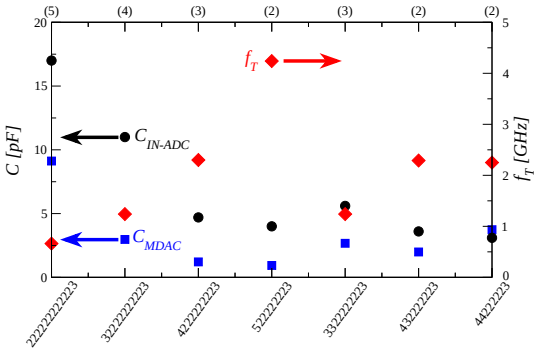

Figure 4. Total input capacitance and OTA GBW (first MDAC) for different bit partitioning of the ADC. The number of stages requiring calibration is reported at the top of the figure.

In order to validate the mathematical model, a MATLAB model of the ADC was implemented based on the eq.s (2) to (6) toghether with (19). Capacitor mismatch parameter k_c and γ noise factor were derived from a digital $0.18\ \mu m$ CMOS technology.

The mathematical model points out that, assuming $\Delta C = 3\sigma_{\Delta C}$, the $422\ldots23$ architecture exhibits a worst-case maximum INL of approximately 4.5 LSB if the first 3 stages are not calibrated. A maximum INL of approximately 3.5 LSB has been obtained after 100 MATLAB Montecarlo simulations, in agreement with the mathematical model.

Finally, a complete converter model in a high level circuit description (Verilog-A) was implemented. This electrical model allowed to verify the performances of the MDAC with a relatively short simulation time. The simulated MDAC output are in a good agreement with the mathematical model implemented in MATLAB. Notice that the Verilog-A model allows the simulation of the complete 14-bit ADC, even though the required simulation time does not permit an extensive Montecarlo simulation.

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