Toward Software Defined Radio : The ADC Goes from Baseband to Antenna

Yann Deval, Dominique Dallet and Jean-Baptiste Bégueret
Laboratoire IXL – UMR 3858 – ENSEIRB - University of Bordeaux , FRANCE
Phone: +33 5 40 00 65 40, Fax: +33 5 56 37 15 45, E-mail: deval@ixl.u-bordeaux.fr

Abstract — A general overview of radio receivers and transmitters is presented. Introducing the principle of frequency translation, classical heterodyne and homodyne RX and TX architectures for analog telecommunications are discussed. Digital telecommunications are addressed and, with them, modern polyphased transceiver architectures and the insertion of an ADC within the receiver chain. First the ADC is considered at the baseband level, then at higher frequency stages, and up to the antenna yielding to the ultimate Software Defined Radio (SDR) principle. At each location of the ADC within the receiver chain, the converter characteristics are reviewed, leading to the choice of a possible architecture. Nonidealities are discussed in order to highlight problems that researchers will have to address in the future to fulfill the SDR concept.

I. INTRODUCTION

As telecommunication is a mass market, modern radiofrequency transceivers are highly integrated. The reason is, of course, for the overall system cost to be as low as possible. This cost reduction also mandates the integrated circuits to be manufactured in as low cost a technology as possible. Following this paradigm, several silicon RFICs have been proposed in the last decade, ranging from 1 GHz up to few tens of GHz [1].

The fact of the matter is that silicon ICs are not well suited to fulfill the performance level required by an RF system. This is mostly due to poor passive components [2], a consequence of the low resistivity substrate on which submicron transistors are manufactured. Therefore, novel approaches are required in either system architectures or circuit topologies, for silicon RFICs to be successfully implemented in telecommunication systems. Taking advantage of the advances in ADC to design as digital as possible a receiver is among the possible solution, as presented in this paper.

II. RECEIVER

A. Frequency conversion

To describe the architecture of a receiver, one have to first consider the frequency conversion process which is brought into play using an analog multiplier, as depicted in Fig. 1.

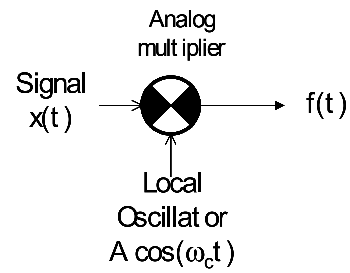

Figure 1 : Frequency conversion – the mixing process

The output signal $f(t)$ is expressed as :

$$\begin{aligned} f(t) &= A\cdot\mathbf{cos}(\omega_c t)\cdot x(t) \\ &= A\cdot x(t)\cdot\frac{\mathbf{exp}(j\omega_c t)+\mathbf{exp}(-j\omega_c t)}{2} \\ &= \frac{A}{2}\cdot x(t)\cdot\mathbf{exp}(j\omega_c t)+\frac{A}{2}\cdot x(t)\cdot\mathbf{exp}(-j\omega_c t) \end{aligned} \quad (1)$$

with ω_c the frequency of the local oscillator (LO) and A its amplitude.

Applying the Complex Fourier Transform (CFT) $F(\omega)$ of $f(t)$ defined as

$$F(\omega)=\int_{-\infty}^{+\infty} f(t)\mathbf{exp}(-j\omega t)dt \quad (2)$$

it leads to

$$\begin{aligned} F(\omega) &= \frac{A}{2}\int_{-\infty}^{+\infty} x(t)\cdot\mathbf{exp}(j\omega_c t)\mathbf{exp}(-j\omega t)dt \\ &\quad +\frac{A}{2}\cdot\int_{-\infty}^{+\infty} x(t)\cdot\mathbf{exp}(-j\omega_c t)\mathbf{exp}(-j\omega t)dt \\ &= \frac{A}{2}\int_{-\infty}^{+\infty} x(t)\cdot\mathbf{exp}(-j(\omega-\omega_c)t)dt+\frac{A}{2}\int_{-\infty}^{+\infty} x(t)\cdot\mathbf{exp}(-j(\omega+\omega_c)t)dt \end{aligned} \quad (3)$$

and, as it comes from (2) that

$$X(\omega+A)=\int_{-\infty}^{+\infty} x(t)\mathbf{exp}(-j(\omega+A)t)dt \quad (4)$$

expression (3) merely expresses as :

$$F(\omega)=\frac{A}{2}\cdot X(\omega-\omega_c)+\frac{A}{2}\cdot X(\omega+\omega_c) \quad (5)$$

with $X(\omega)$ the CFT of the input signal $x(t)$.

It can be demonstrated that the CFT is related to the Power Spectral Density (PSD), *i.e.* the spectrum of a given signal. Therefore, Eq. (5) demonstrates that the fact of multiplying an input signal *x(t)* with a LO of frequency ω_c acts like translating the input signal in frequency, simultaneously up and down converted, the shift in frequency being ω_c in both cases.

B. The Direct Conversion Receiver (DCR)

Assuming Eq. (5), it appears quite easy to implement a DCR barely adding a mere Low Pass Filter (LPF) to the abovementioned analog multiplier, a matter of selecting the down-conversion term alone. The corresponding spectrum shift is depicted in Fig. 2.

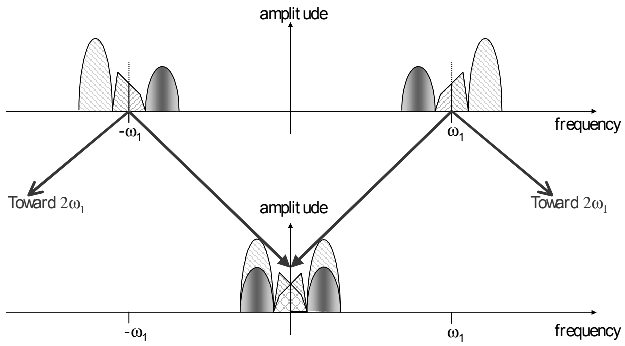

Figure 2 : The Direct Conversion Receiver principle.

Fig. 2 highlights some drawbacks of the DCR approach :

- The wanted signal is its own image, so unsymmetrical RF spectrum will result in a symmetrical baseband spectrum, which is a problem of its own,
- It can be seen that a very high order channel selection filter is mandatory in order to separate the wanted channel from both the adjacent channels,
- The baseband signal includes DC, and as a matter of consequence the system is very sensitive to offset of all sort.

C. The Polyphased DCR

To counteract the unsymmetrical spectrum fold up, one can take advantage of polyphase frequency conversion. In addition, such an operation make the DCR independent of the instantaneous relative phase of the LO and the received signal. Indeed, if we assume that the LO is no longer *A.cos*($\omega_c t$) but rather *A.sin*($\omega_c t$), Eq. (1) becomes

$$\begin{aligned} f(t) &= A \cdot \mathbf{sin}(\omega_c t) \cdot x(t) \\ &= A \cdot x(t) \cdot \frac{\mathbf{exp}(j\omega_c t) - \mathbf{exp}(-j\omega_c t)}{2j} \\ &= \frac{A}{2} j \cdot x(t) \cdot \mathbf{exp}(-j\omega_c t) - \frac{A}{2} j \cdot x(t) \cdot \mathbf{exp}(j\omega_c t) \end{aligned} \quad (6)$$

and thus, applying the CFT once again, we have

$$F(\omega) = \frac{A}{2} j \cdot X(\omega + \omega_c) - \frac{A}{2} j \cdot X(\omega - \omega_c) \quad (7)$$

which means that the down-converted signal is in phase quadrature with regards to the one we previously obtain thanks to Eq. (5).

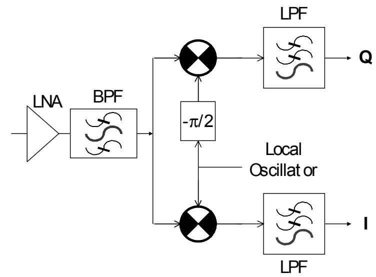

Figure 3 : The Polyphased Direct Conversion Receiver.

Also, its phase is either positive or negative, depending on its relative position with regards to the LO frequency. It is thus easy, having both the cosinus and the sinus paths, to process an unsymmetrical RF spectrum. These two sections are typically named the I (In-Phase) and Q (Quadrature Phase) paths, respectively.
It yields the DCR architecture depicted in Fig. 3.

D. Digital vector demodulator

When the RF signal is at a higher frequency than that of the LO, *i.e.* it is in the Upper Side Band (USB), it leads to the baseband spectrum depicted in Fig. 4.

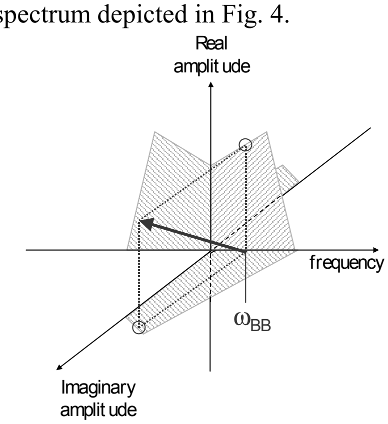

Figure 4 : Instantaneous baseband signal when the signal is higher in frequency than the LO.

The IQ vector corresponding to the ω_{BB} instantaneous frequency is obviously very different than the one of the same baseband instantaneous frequency coming from the Lower Side Band (LSB) as a consequence of an RF signal at a lower frequency than that of the LO, as depicted in Fig. 5.
Such a DCR is therefore able to process asymmetrical spectrum, at the price of an increased complexity of both the RF paths and the synthesizer topology, as the latter will have to provide the receiver with high precision polyphased local oscillators [3,4].
On the other hand, it can be seen from Fig. 4 and Fig. 5 that being able to characterize the baseband IQ vector allows to compute not only the instantaneous frequency of the RF signal, but also and in the same time its phase and amplitude. Doing so yields to a very versatile demodulator, able to deal with almost any kind of modulation scheme.

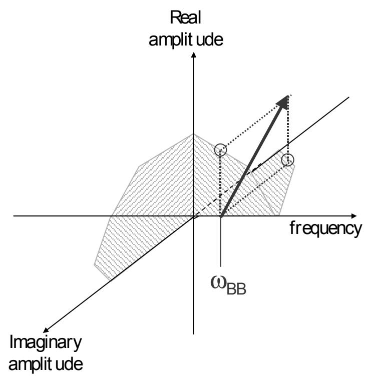

Figure 5 : Instantaneous baseband signal when the signal is lower in frequency than the LO.

III. DIGITAL RECEIVERS

A. DCR

As a vector computation is easily performed in the digital domain thanks to CORDIC-like algorithms [5,6], the analog baseband signal is converted with an Analog-to-Digital Converter (ADC), to allow a DSP to process the signal and demodulate the message. The architecture is depicted in Fig. 6.

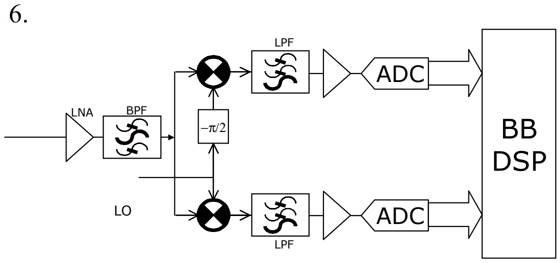

Figure 6 : DCR with a general purpose digital demodulator.

Thanks to Automatic Gain Control (AGC) circuits included in the RF front end and in the baseband section, the dynamic range of the RF signal is typically reduced to as low as 30 dB, *i.e.* 5 bits. On the other hand, DC-offset compensation as well as blocking signal and high power adjacent channel capabilities usually strengthen the dynamic constraint, and a 8 bit ADC is mostly common for such a topology [7]. As the baseband frequency of interest is usually quite low, even if some new standards such as the 802.11a no longer verify this assumption, almost any kind of ADC architecture is suitable to perform the conversion.

B. The Low Intermediate Frequency (LIF) receiver

While the constraint regarding the ADC characteristic is somewhat low in DCR, this is mostly due to the use of the high order channel selection filters which reduce the dynamic range one can observe in the baseband section. Filter orders as high as five are common [8], which yields a huge silicon area for total integration and, typically, a severe bottleneck in the power budget of the overall system. To overcome this drawback, one can increase the number of bit of the ADC and implement digital filtering [7], but the LIF receiver is to be considered, too.
The LIF architecture is depicted in Fig. 7.

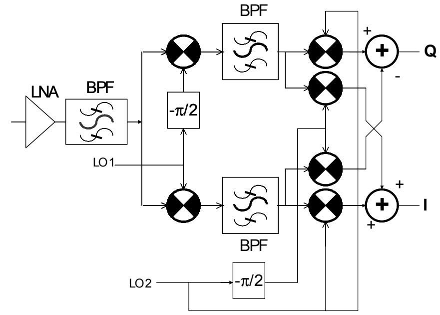

Figure 7 : The LIF receiver.

In this topology, the RF signal is first down-converted to an intermediate frequency which is roughly equal to the channel frequency width. Image Rejection Mixers (IRM) are used, as a strong image is expected. The final down-conversion step is performed with a complex mixer [9] to further reduce the image conversion. Acting so, the system is no longer sensitive to neither DC-offset nor stringent channel selection filtering, and a mere first order band pass filter is still suitable. The drawback is for the ADC, which have to provide a minimum 11 bit resolution as shown in [9]. Due to the high resolution and the otherwise still quite low frequency of interest, the choice of a ΣΔ ADC is typical. The ΣΔ can be implemented as a passband [10], though the ADC is always a high resolution one.
This approach is popular as it consists of reducing the amount of analog circuitry in favor of digital circuitry, which is a good trend for a mass market like the one the radiocommunication products are addressing. Nevertheless, this approach is not only true for LIF receivers, as high resolution ΣΔ ADCs are now used in DCR too, the excess converter bits being used to reduce the constraints on both the analog and RF sections of the system [7].

IV. SOFTWARE DEFINED RADIO SDR

A. The Software Defined Radio receiver

The fact of the matter is that the above presented LIF receiver is nothing else but a classical superheterodyne receiver with an otherwise uncommonly low intermediate frequency.
Therefore, a so-called Software Defined Radio (SDR) can be designed based on the architecture depicted in Fig. 8.
In this receiver, the intermediate frequency signal directly feeds the ADC, the baseband down-conversion being performed in the digital domain. A digital demodulator is expected to assume any kind of demodulation at a given time, receiving from a neighbor ROM the code source required to implement the wanted demodulation scheme.

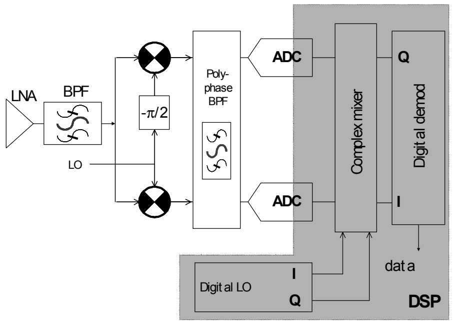

Figure 8 : The basic SDR receiver principle.

Such a system is even capable to *receive* a new demodulation scheme code source, and to store it in a memory of his own. Acting so, the system is able to demodulate signals from a telecommunication standard which was not even defined at the time the system was manufactured, making it very compliant.

The architecture of the ADC depends, among others, of the intermediate frequency and the dynamic range. At moderate IF, an interleaved flash topology is sometimes brought into play, such as the 8 bits ADC used in [11] to deal with wideband code division multiple access.

B. The ultimate SDR receiver

Pushing the principle further leads to the ultimate SDR receiver, depicted in Fig. 9. In this ideal architecture the antenna is directly connected to the input of the ADC, and the baseband DSP deals with the demodulation process on a compliant basis, as previously stated.

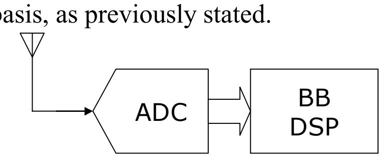

Figure 9 : The ideal SDR receiver – a dream still to come.

Such an ultimate RF receiver is, however, still to be designed successfully. Indeed, not talking of the challenge in designing the DSP able to deal with several gigabits per second, too many bottlenecks in the ADC diminish the interest of the proposed topology. Indeed :

- The ADC will have to provide a roughly 100dB dynamic range, *i.e.* a 16 or even 17 bit ADC, with input frequency extending from 1 up to 10 GHz,
- The ADC power consumption will have to be tiny,
- The ADC sample and hold (S/H) will have to provide low parasitic charge injection, as the signal is weak, while clocked at several gigahertz.

Several attempts to fulfill some of these requirements have been done in the past when designing ADC [12], but notwithstanding SDR is becoming more and more popular because of the flexibility the digital circuitry offers, today the ultimate SDR receiver is still closer to a paradigm than to a practical product.

V. CONCLUSION

The ultimate SDR receiver is currently quite far from the mass production level, but some heavily digital system are already available. Because of the mass market it is dedicated to, though, a lot of research is addressing the field, and therefore the RFIC community can expect rapid progress in the field, and at least has to try to be prepared to face the challenge.

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