True N-Bit Calibration of Pipeline A/D Converters: Trends and Challenges[1]

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Abstract ***– The digital calibration algorithm for conventional 1-b/stage pipelined analog-to-digital converters introduced by Karanicolas et al. [1] occasionally leads to missing or non-monotonic digital codes. In this paper, we show that an extension of that algorithm to 1.5-b/stage architectures actually leads to more frequent code errors. We also describe two methods to improve A/D performance in the presence of non-linear operational amplifiers. The first method uses a calibration that assures monotonicity in the presence of arbitrary comparator offset voltages. The second method employs an input-dependent level-shifting stage to achieve high linearity.***

I. INTRODUCTION

CMOS pipeline analog-to-digital converters at lower supply voltages are widely used in applications that require both high speed and high resolution. With the continuing exponential advances of integrated circuit process technology and the emerging trend toward system-on-chip solutions, data converters must be integrated with, and operated at, the same low supply voltages as complex digital circuitry. However, the use of modern sub-micron CMOS transistors results in poor active device matching and high output conductance, and correspondingly large dc offset voltage errors in precision operational amplifier and voltage comparator circuits. Specifically, in typical CMOS switched-capacitor implementations, precision capacitor mismatches, charge injection errors, finite operational amplifier gain errors, and comparator random offset voltages are major limitations on accuracy. Hence, to achieve a high-accuracy A/D, analog or digital calibration techniques are used to correct these non-ideal effects [1]-[4].

It is well known that the Karanicolas method [1] corrects differential non-linear (DNL) errors to the n-bit level in a pipelined A/D, and improves, but does not fully correct integral non-linearity (INL) errors. These attributes are vividly illustrated in Table I for the example of a one-bit-per-stage 10-bit pipeline A/D plus four calibration stages in 0.18μm CMOS with V_{DD} = 1.8V. Furthermore, assuming low gain and low linearity opamps representative of future technology nodes, the Karanicolas approach does not assure converter monotonicity as will be discussed in section II.

Other correction methods have been reported. Ingino and Wooley [3] use analog calibration to adjust the comparator switching threshold and one of the reference voltages. Ming and Lewis [4] use an extra DAC, a delta-sigma ADC, and a random number generator to remove DNL and gain errors. These correction approaches require sophisticated overhead circuitry to perform the calibrations and do not address the effects of opamp non-linearity on converter performance.

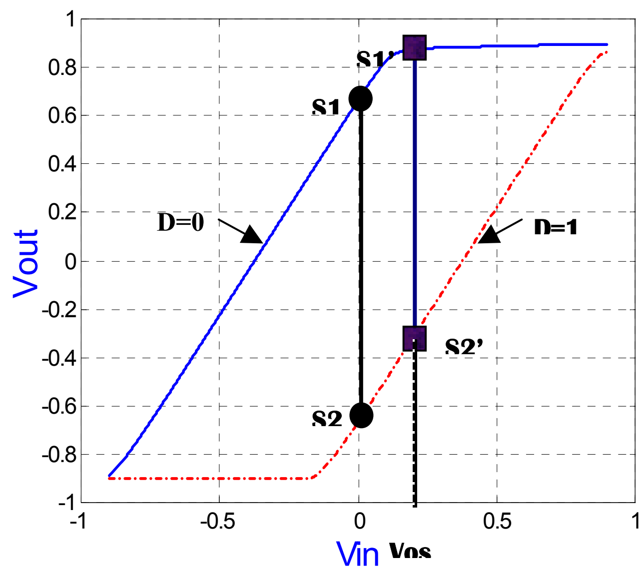

Fig. 1. The conventional digital calibration factor is determined by forcing Vin=0 and measuring the difference between S1 and S2. The actual transition occurs at Vin=Vos. Due to opamp nonlinearities, the difference between the actual transition points S1' and S2' is different from S1-S2.

Table I. Karanicolas Calibration Method (V_{DD} = 1.8V) for various full-scale ranges.

FSR	Calib.	DNL (LSB)	INL (LSB)	SNDR (dB)	ENOB (bits)
1.5V	Before	-1.00 to 0.98	-32.1 to 33.8	30.80	4.83
	After	-0.43 to 0.28	-2.09 to 2.12	51.16	8.21
1.1V	Before	-1.00 to 0.99	-28.9 to 30.6	30.75	4.81
	After	-0.23 to 0.26	-1.18 to 1.28	55.27	8.89
0.7V	Before	-1.00 to 0.80	-27.1 to 28.2	30.57	4.79
	After	-0.41 to 0.36	-0.80 to 0.69	58.76	9.47

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In this paper, we extend the calibration algorithm to correct for non-monotonicity and opamp non-linearity errors.

II. CONVENTIONAL DIGITAL CALIBRATION

A pipelined A/D is made up of several stages. Ideally, the input and output residue voltages for each stage range from *-Vr* to *+Vr* where *Vr* is the converter reference voltage. However, non-idealities perturb the residue characteristic including comparator dc offset voltages, reference voltage errors, operational amplifier dc offset voltages, opamp finite gain errors, etc. Figure 1 shows a typical residue plot for a 1b stage with and without comparator offset voltage.

In the Karanicolas approach, the correction factor for the m^{th} stage, *COR(m)*, of an n-bit A/D is determined by applying a 0V input voltage. The digital input, D_m, to the intra-stage one-bit DAC is forced to *Logic 0*, and the residue voltage is converted by the lower (n-m) stages resulting in a (n-m+1) bit word, S1. S2 is determined similarly with D_m set to *Logic 1*. Finally, *COR(m)* = S2-S1+1 (ideally, *COR(m)* = 0). The algorithm starts with the penultimate stage (n-1), and proceeds sequentially to the MSB stage. All coefficients are found using the previously determined factors; e.g., *COR(m)* uses *COR(m+1)* through *COR(n-1)*, etc. However, the major transition actually occurs at the offset voltage, $V_{in}(m) = V_{os}(m)$, not at $V_{in}(m) = 0$. The correct calibration coefficient is actually *COR'(m)* = S2'-S1'+1, not *COR (m)* = S2-S1+1.

Figure 2 shows that all possible converter errors can result from using the inexact *COR(m)* values rather than the accurate *COR'(m)* coefficients: *COR(m) = COR'(m)* is correct, *COR(m) = COR'(m) + q,* where $q \geq 1$ yields a missing code, *COR(m) = COR'(m) – 1* gives increased transition width, and *COR(m) = COR'(m) – p,* where $p \geq 2$ creates a non-monotonicity.

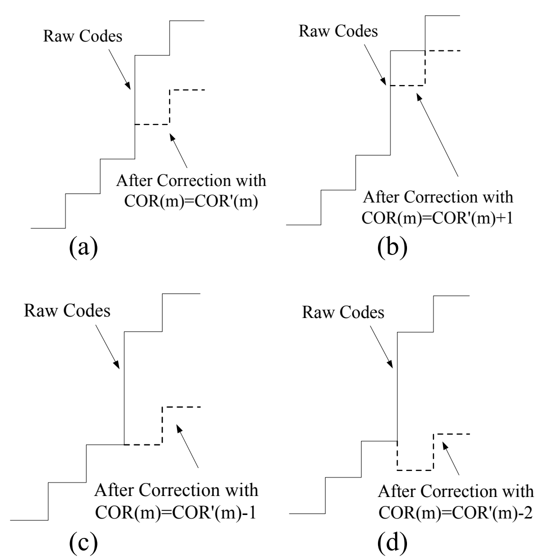

Fig. 2. Converter errors. (a) Correct, (b) missing codes, (c) increased transition width, and (d) non-monotonicity.

To quantify this effect, a behavioral model of a 14-stage pipeline converter was simulated using a *linear* inter-stage gain of 1.8X. The comparators were assigned random dc offset voltages. One example of the resulting 14-bit codes before applying *COR(1)* are shown in Fig. 3. The solid line shows the codes with a comparator offset $V_{os}(1)$ = -12.3mV. The dashed line is used to calculate *COR(1)* with the comparator bypassed as described above. The full-scale range is 1.5V, and the least significant bit (LSB) is 92μV.

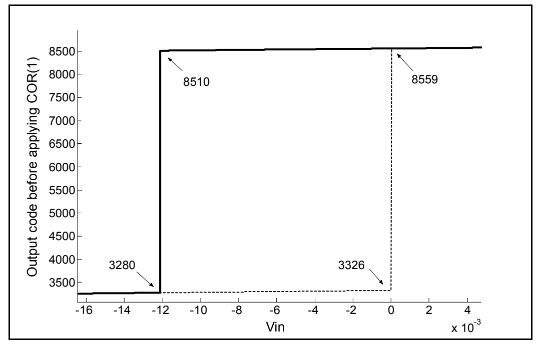

Fig. 3. Codes for the actual (solid) and forced (dashed) transitions with COR(2) through COR(13) applied.

Note that in the conventional Karanicolas calibration algorithm, *COR(1)* = 3326-8559+1 = -5232 determined at $V_{in}(1) = 0$. If the *actual* transition point is applied instead, i.e. $V_{in}(1) = V_{os}(1)$ = –12.3mV, the calibration factor becomes *COR'(1)* = 3280-8510+1 = -5229. The difference is due to the non-linearity of the overall ADC which remains even after applying COR or COR'.

Using *COR(m)* rather than *COR'(m)* leads to converter errors as illustrated in Fig. 4. Adding *COR(1)* to the first code after major transition (8510) gives an incorrect count of 3278 and creates a non-monotonicity at the major transition as shown in Fig. 4. Likewise, the appearance of missing codes (e.g., 3281 in Fig. 4) means that *COR(m)* = *COR'(m) + 1* for one or more of the other stages.

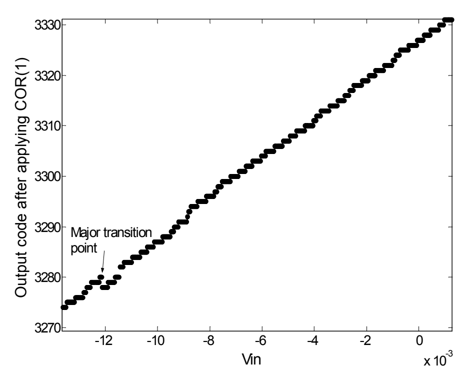

Fig. 4. Converter errors after conventional correction.

In addition to using correction factors, one may also use redundancy [2]. In a 1.5-b per-stage pipelined A/D, two bits are generated per stage. After the conversion is completed by all stages, the digital bits are combined to produce the final output codes. As the power supply voltages are scaled to sub-1V levels, opamp gain non-linearity becomes significant resulting in a high probability of non-monotonicity as illustrated in Fig. 5

Although fully differential architectures are used to cancel even-order harmonic distortion terms, odd harmonics are not suppressed. Consequently, third-order harmonic distortion usually dominates opamp gain non-linearity. In conventional A/D converter design, the maximum signal swings are often reduced to avoid the highly non-linear regions of the opamp gain characteristic. Voltage headroom requirements preclude the use of cascode and gain-boosted configurations in ultra-low-voltage designs. An alternative approach is to use two- or multi-stage opamp configurations, but significant speed potential is sacrificed in frequency compensating these amplifiers for closed-loop stability.

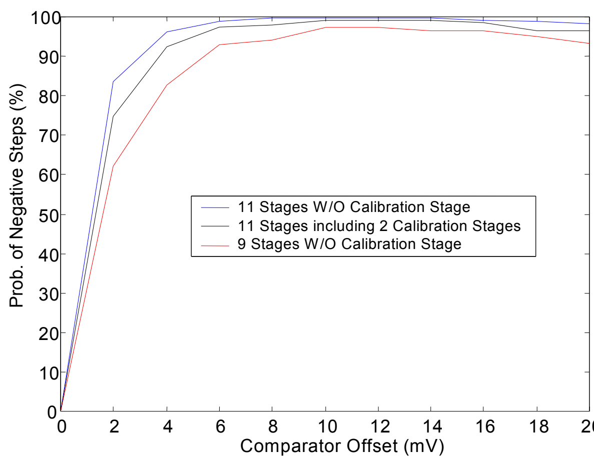

Fig. 5. Simulated probability of non-monotonic codes versus comparator standard deviation for 1000 simulations of three 1.5-b/stage architectures.

III. DIGITAL CALIBRATION FOR MONOTONICITY

To overcome the non-montonicity and remaining missing code problems, we employ a simple DAC to apply an input voltage that enables determination the digital output codes just before and just after the actual transition. It is very important to note that the actual transition voltage is not needed in this algorithm. Using these two digital codes, *COR'(m)* is determined as in the Karanicolas method. Figure 6 shows a signal flow graph for measuring *COR'(m)*.

Figure 7 shows the output codes near the actual transition point after using the new correction factors, *COR'(m),* on all stages. There are no missing codes or non-monotonicities. Although this calibration is presented for a 1bit/stage pipeline A/D for simplicity, it is easily extended to a 1.5bit/stage A/D.

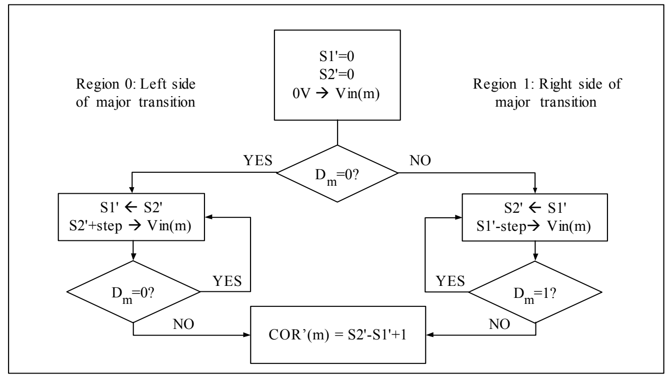

Fig. 6. Algorithm to locate the exact major transition codes.

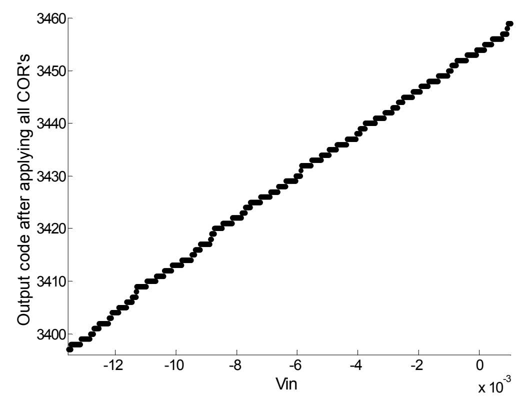

Fig. 7. Output codes near the major transition point after improved calibration.

IV. MIXED-SIGNAL CALIBRATION

In terms of linearity requirements, the ideal residue graph of a 1.5-bit per stage pipeline converter exhibits a very important feature: if the analog signal applied to the first stage is limited to the region from $-V_{ref}/2$ to $+V_{ref}/2$, all of the following stages operate between $-V_{ref}/2$ and $+V_{ref}/2$. The operational amplifiers are usually highly linear in this "sweet spot." To avoid the highly non-linear regions of the opamp gain characteristic while maintaining a full-scale voltage range for the analog signal V_{in} to the front-end S/H stage, we employ an *input-dependent* level-shifting stage as an interface between the analog input and the 1.5-b/stage pipeline A/D as illustrated in Fig. 8.

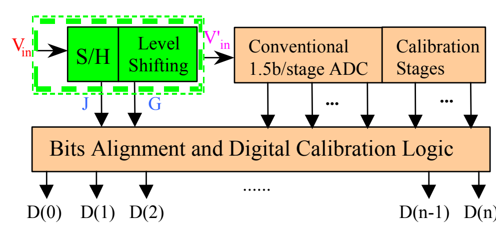

Fig. 8. Architecture of a 1.5-bit-per-stage pipeline converter with mixed-signal calibration.

The objective of input-dependent level shifting in the analog domain is to limit the input voltage range of the first stage, and hence all subsequent stages, to the high linearity region from $-V_{ref}/2$ to $+V_{ref}/2$. The front-end stage performs the following level-shifting operations: if $V_{in} > +V_{ref}/2$, J=1, G=1, and $V_{in}' = V_{in} - V_{ref}/2$, and if $V_{in} < -V_{ref}/2$, then J=0, G=0, and $V_{in}' = V_{in} + V_{ref}/2$; otherwise, J=1, G=0, and $V_{in}' = V_{in}$.

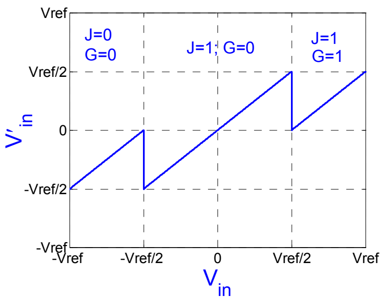

Fig. 9. Transfer characteristic of the front-end stage showing the level-shifted analog input voltage V_{in}' that is applied to the converter v/s the raw input voltage V_{in}.

Two comparators are used in the level-shifting stage to detect the input voltage range; the resulting 1.5-bit digital word (J and G) drives the level-shifting DAC and is used for signal reconstruction in the digital domain. The level-shifting operation is incorporated into a switched-capacitor 2X gain stage that also performs the front-end sample-and-hold function. The transfer function is shown in Fig. 9.

Since the input-dependent level shifting in the analog domain is a compression operation, the expansion function is accomplished in the digital domain after calibration.

Calibration begins with the penultimate stage applying a version of [1] modified for the 1.5-bit/stage topology. The calibration coefficient of a stage is determined using the previous calibration factors for the lower stages. After determining the calibration coefficients for the regular converter stages, the output codes (without truncation) for the first stage corresponding to the voltages at *-Vref/2* and *+Vref/2* are found. Similar to the technique for measuring the correction coefficients, $V_{in}' = -V_{ref}/2$, J=0, and G=0 are set, and S1 in Fig. 9 is digitized; keeping V_{in}' and G unchanged with J=1, S2 is found. S1-S2 corresponds to a digital representation of the level-shift amount $V_{ref}/2$ in the analog domain. S3 and S4 are determined in a similar fashion, and the difference S4-S3 corresponds to the level-shift voltage of $-V_{ref}/2$ in the analog domain. Hence,

$$D(V_{in}) = \begin{cases} D(V_{in}^{'}) + S2 - S1 - 1 & if\ J = 0, G = 0 \\ D(V_{in}^{'}) & if\ J = 1, G = 0 \\ D(V_{in}^{'}) + S3 - S4 + 1 & if\ J = 1, G = 1 \end{cases}$$

where $D(V_{in})$ denotes the digital representation of the analog input voltage V_{in} after calibrating to eliminate missing codes, etc. Figure 10 shows the relationship between V_{in}' and V_{in} in the digital domain. Ideally, $D(-V_{ref}/2)$ = S1-S2 = S3-S4**.**

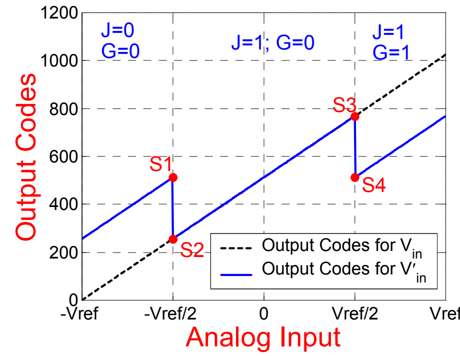

Fig. 10. Signal reconstruction in the digital domain.

V. 1.5-BIT SIMULATION RESULTS

For the behavioral simulations, nine 1.5-bit converter stages followed by two 1.5-bit calibration stages are cascaded with the input sample-and-hold/level-shifting stage described earlier. To guarantee monotonicity, the digital calibration technique described in section III is also used. All the 1.5-bit stages have a nominal inter-stage gain of 2X. The voltage transfer function of the opamp is extracted from *HSPICE* simulations for the folded-cascode amplifier operating with a 1.8*V* power supply voltage. The general relationship between the output and input voltages of the amplifier is $V_{out}=A_3*V_{in}^3+A*V_{in}+V_{off\text{-}set}$. In the fully differential implementation used for this study, the third-order harmonic term, $A_3 = -0.24768$ is the dominant non-linearity coefficient, and $V_{off\text{-}set} = 0$. The overall performance results are summarized in Table II.

Table II. Performance summary.

Resolution	10bits
ENOB	9.62
INL	<+/-0.57 LSB
DNL	<+0.24/-0.68 LSB
Power Supply	1.8V
Input FSR	+/-1.5v differential
LSB	366.21 μV

VI. REFERENCES

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