Delta-Sigma Data Converters for Wireless Applications

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Abstract - This paper gives an over view of the Delta-Sigma (ΔΣ) converters for wireless applications. First an overview of data converters is presented, followed by Fractional-N frequency synthesizers. The aim is to give an overview of the subject, and present sufficient level of detail while covering all essential aspects.

I. INTRODUCTION

Delta-Sigma(ΔΣ) Data Converters have become a de-facto industry standard for high-resolution data conversion, specially for wireless applications. ΔΣ data converters use Oversampling and Noise-shaping to reduce the quantization noise in the signal-band. The noise is spectrally shaped to be outside the frequency band of the signal. Section II explains the concepts of Oversampling and Noise-shaping, and develops the subject of ΔΣ data-conversion. Section III presents examples of ΔΣ ADCs/DACs and compares and contrasts the different designs. Section IV presents general conclusions.

II. ΔΣ DATA CONVERSION

ΔΣ data converters use oversampling and noise-shaping techniques to increase the output signal-to-noise ratio (SNR) by filtering out quantization noise. A Quantizer is a non-linear device which approximates it's input to the nearest discrete output level. The quantization noise e(n) is assumed to be white, and uniformly distributed between ±Δ/2, where Δ=quantization step, with the variance

$$\sigma_v^2 = \frac{\Delta^2}{12} \tag{1}$$

The power spectral density of the quantization noise is

$$S_e = \frac{\left(\Delta^2/12\right)}{\left(f_s/2\right)} = \frac{\Delta^2}{6f_s} \tag{2}$$

A. Low Pass Delta—Sigma

In architectural terms, ΔΣ data converters use a coarse Quantizer connected in a negative feedback loop to spectrally shape quantization noise away from the signal frequency. The feedback loop typically does not disturb the signal (all-pass signal transfer characteristic).

The digital base-band signal $x_d(n)$ is converted to a continuous-time, continuous-amplitude analog signal $x_a(t)$. The interpolator block is the digital equivalent of the analog sample-and-hold and performs the same function: it up-samples the signal before being input to the ΔΣ modulator. The transfer function of the 1st order ΔΣ ADC, and it's linear model [1] is

$$STF(z) = \frac{H(z)}{1+H(z)} \tag{3}$$

The Noise Transfer Function (NTF) is

$$NTF(z) = \frac{1}{1+H(z)} \tag{4}$$

Typically, H(z) is a discrete-time Integrator.

$$H(z) = \frac{z^{-1}}{1-z^{-1}} \tag{5}$$

The STF & NTF are, therefore

$$STF(z) = z^{-1} \tag{6}$$

$$NTF(z) = (1-z^{-1}) \tag{7}$$

Note that $STF(z) = z^{-1}$ represents a unit delay in the signal path. Using

$$z = e^{j\omega} = e^{j(2\pi f)/f_s} \tag{8}$$

it can be shown[1]

$$\left|NTF(f)\right| = 2Sin\left(\frac{\pi f}{f_s}\right) \tag{9}$$

which represents a high-pass characteristic.
Defining the Oversampling ratio to be

$$OSR = \frac{f_s}{2f_0} \tag{10}$$

the peak SNR is shown [1] to be

$$SNR(dB) = 6.02*N - 3.41 + 30*\log(OSR) \tag{11}$$

Doubling the OSR results in a 9dB improvement in SNR.
For a 2nd order ΔΣ ADC, the STF & NTF are

$$STF(z) = z^{-2} \tag{12}$$

$$NTF(z) = (1-z^{-1})^2 \tag{13}$$

$$\left|NTF(f)\right| = \left(2Sin\left(\frac{\pi f}{f_s}\right)\right)^2 \tag{14}$$

The peak SNR is shown to be [1]:

$$SNR(dB) = 6.02N - 11.14 + 50Log(OSR) \tag{15}$$

Doubling the OSR results in a 15dB improvement in SNR. For any increment in OSR, a 2nd order modulator shows a more drastic increase in SNR than a 1st order.

Band-Pass ΔΣ modulators are ideally suited for wireless data conversion, because of their ability to digitize signals that are not baseband-centric. In a superheterodyne receiver, the pair of low-pass modulators for the I/Q channels may be replaced by a single band-pass modulator digitizing the intermediate frequency directly.

Band-Pass ΔΣ modulators shape quantization noise away from an intermediate (non-zero) frequency. This is achieved using a band-pass characteristic for H(z). A simple low-pass to band-pass transformation[3] is

$$z \to -z^2 \qquad (17)$$

The transformation of Eq. (17) results in an NTF notch at $(f_s/4)$ and is very commonly used. Note that the band-pass modulator obtained using the transformation of Eq. (17) has twice the order of its low-pass counterpart but the same performance. A more generic low-pass to band-pass transformation is shown in [18]

Bandpass converters are gaining importance in RF design because of their immunity to flicker noise, and simplification of the heterodyne architecture, as mentioned before.

B. ΔΣ Fractional-N PLLs

ΔΣ modulators find applications in frequency synthesizers, for generating fractional multiples of a reference frequency. Frequency Synthesizers typically use a phase-locked loop (PLL) for synchronizing a local clock to an external reference.

A typical integer-N Charge-pump PLL[4] is shown in Fig. 2. The Phase-Frequency Detector (PFD) generates 2 signals Up/Down controlling 2 switches to the Charge

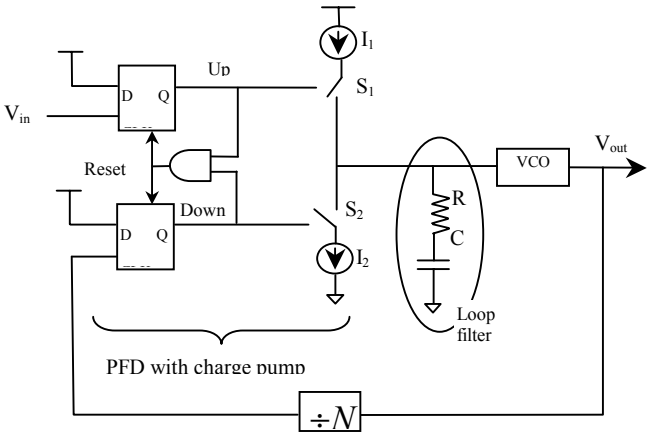


Fig. 2: A charge-pump integer-N. PLL.

Pump, which indicate whether the VCO needs to be speeded up (Up) or slowed down (Down). The charge pump voltage is low-pass-filtered and controls the oscillation frequency of the VCO. The feedback forces $f_{out}=Nf_{ref}$. When the PLL is in lock, the loop filter voltage equals the VCO voltage necessary for the VCO to run at the N^{th} multiple of the reference clock frequency. N needs to be an integer. To generate a fractional multiple of the reference, the circuit in [5] is used. The multi-modulus divider can divide by any of the numbers $\{N+m(t)\}$, where m(t), the output of the ΔΣ modulator, can take any of the discrete values from a finite set, say {-1,0,+1}. The concept is that division by (N+1) occasionally, (N) at other times, and (N-1) at still other times is equivalent to division by an n such that $N-1<n<N+1$, thereby achieving fractional division *on-average*. With this arrangement, the VCO frequency is then $(N+m(t))$ times the reference frequency. For a 3 bit output from the modulator, the divider needs to be capable of division by 2^3 different moduli, {N-3, N-2, N-1, N, N+1, N+2, N+3, N+4}, with the modulator output selecting the division modulus. The input sequence x(t) is typically also from a finite set, and in the implementation of [5] only 2 values are used. The channel spacing is a function of x(t), since x(t) controls the bit output from the modulator. In [5] the channel spacing is $(f_{ref})/2M$, where 2M is the difference of the 2 discrete inputs which comprise x(t). The quantization noise of the ΔΣ modulator which is within the bandwidth of the PLL degrades the phase noise of the PLL. Therefore, it is advantageous for the PLL to have a narrow bandwidth, however, this has an adverse impact on the acquisition time. A detailed analysis of PLL phase noise is beyond the scope of this paper. Having developed the subject of ΔΣ modulation, the following section is devoted to the use of these techniques for wireless devices.

III Applications to Wireless Communications

The main requirements for wireless devices are that they consume very low power, have high linearity and have sufficient dynamic range to amplify signals whose strengths can vary over several orders of magnitude. The low-power requirement arises from the desire to prolong battery life, and the linearity criteria comes from the need to reject very strong blocking signals which may intermodulate with higher-order harmonics and give rise to spurious components in the signal band.

The dynamic range requirements come from the need to be able to receive signals whose strengths can vary from 10μV to several tenths of a Volt. Commercial considerations dictate that as much of the signal processing be performed in the digital domain as possible, since VLSI processes are optimized for digital circuits, and considerable savings in chip area are possible. The goal is to shift the ADC block up the receiver chain so that it feeds directly from the antenna, but present VLSI technology has not matured enough to

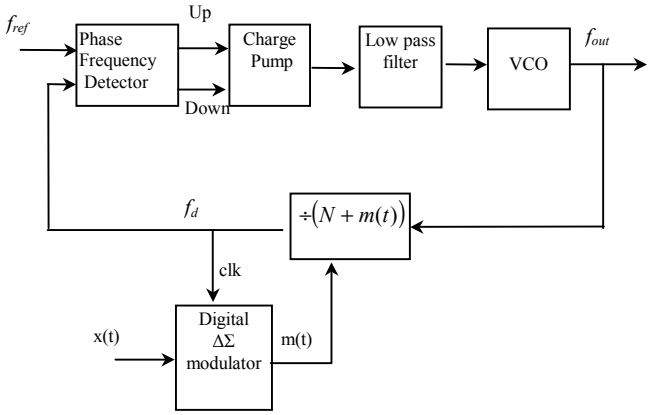


Fig. 3: A ΔΣ modulated multimodulus divider in a PLL for generating fractional multiples of f_{ref}.

be able to digitize analog signals to 16bits at sampling rates in excess of 1GHz.

Fig. 4 shows the design options available in a superheterodyne architecture. Choice (a) downconverts the RF signal to a single IF before conversion to baseband. 2 low-pass ΔΣ ADCs digitize each of the I/Q channels. Down-conversion to baseband through an IF stage eases the requirements on the IF filters, which tend to occupy a large fraction of the chip area. Each extra IF stage requires a mixer & filter. There is a stringent matching requirement on corresponding components on each of the I/Q channels. Choice (b) is a direct-conversion receiver, wherein the VCO operates directly at RF and mixes the RF signal directly to baseband. 2 low-pass ΔΣ ADCs are needed as before. Direct Conversion receivers suffer from dc offset and flicker noise problems, and research is under way to improve performance. In addition, the base-band components must be highly linear since they must block potentially large interference, since these are not filtered by previous stages. Instead of downconversion to dc, the designer may opt to convert to a very low IF, and then digitize the signal. Such an architecture would avoid the dc –offset and flicker noise problems of direct conversion schemes. Choice (c) optimizes the architecture of (a) by using a single band-pass ΔΣ ADC to digitize the signal directly at the intermediate frequency. The subsequent DSP must then be performed at IF. Removing a mixer-filter pair from (a) results in some savings in chip area and power consumption, but the complexity of the bandpass ΔΣ ADC is roughly comparable to a pair of low-pass ΔΣ ADCs.

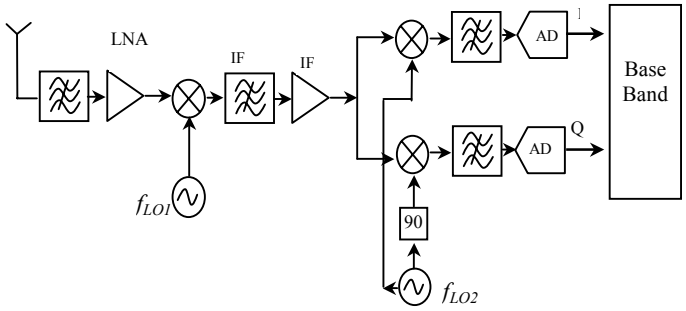
ΔΣ modulators are suited to wireless applications since they are narrow-band converters. A/D conversion is performed to high accuracy only in the signal band. The quantization noise is shaped to be outside this band and adds to adjacent channels, which need to be removed anyway.

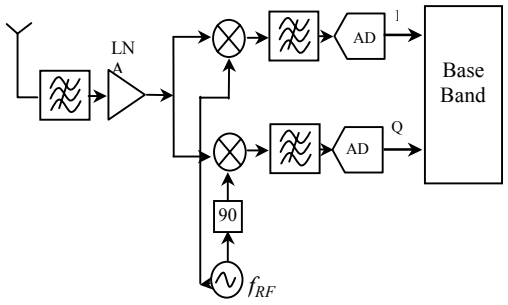
A. ΔΣ ADCs for radio applications

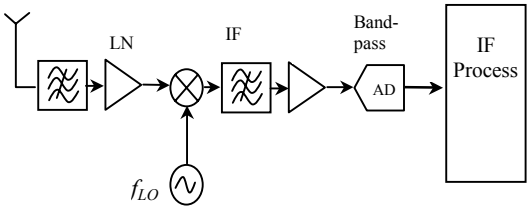
Two particular classes of ADCs have been optimized for radio receivers: 1) Band pass ΔΣ ADCs, and 2) Continuous-time ΔΣ ADCs. In addition, other modulator architectures like MASH, and cascade-of-resonators have also been designed to meet commercial specifications.

A 4th order band pass ΔΣ ADC making use of 9-level quantization, implemented in 0.6μm BiCMOS is described in [7]. The ADC integrates an anti-alias filter and VGA. A digital $(1+z^{-4})$ mismatch-shaping transfer function attenuates DAC mismatch errors. The modulator has an NTF notch at $(f_s/8)$ to obtain extra attenuation at the alias frequency (which is $(7/8)f_s$ away). Implementing the NTF notch at $f_s/4$ would have resulted in a closer first alias at $(3/4)f_s$. The ADC output SNR is 88dB in a 10KHz bandwidth, and 75dB in 200KHz bandwidth. The ADC clock frequency is programmable from 12-24MHz, and decimation factors are also programmable from 60-960.

A design using continuous-time ΔΣ modulators is described in [8]. Continuous-time ΔΣ modulators can be optimized for very low power consumption and are typically fed from a mixer output. The mixer is generally implemented using passive components to







consume very little power. As against switched-capacitor implementations, SNR of continuous- time modulators is not limited by capacitor size[3], but is limited by clock jitter, op-amp linearity/noise, and switching characteristics of (typically) 1-bit feedback waveform. The modulator of [9] is a 5th order low-pass cascade-of-integrators with complex conjugate poles to provide extra notches in the NTF. The modulator is implemented using g_m-C integrators. Decimation is done in 3 stages, first a (↓16), then a shift to dc, finally a (↓2). The ADC was implemented 0.25µm CMOS and achieved carrier-to-noise ratio of 94dB in 9KHz(AM mode) and 79dB in 200KHz bandwidth (FM).

A design which combines a mixer with a continuous-time bandpass ΔΣ ADC is presented in [11]. The modulator uses an LC tank filter, and 2 cascaded resonators, an RC resonator and a switched-capacitor resonator to perform loop-filtering, and a 9 level quantizer as a comparator. 2 external 5.6µH inductors are used. The mixer-ADC combination is able to achieve 89dB and 77dB SNR in 35KHz and 333KHz bandwidths respectively, and consumes 16mA from a 3V supply.. The modulator operates at a clock frequency variable from 9-36 MHz. Table 1 summarizes the performance of the 4 designs.

Reference	Process	Architecture	Sampling Rate	Performance	Power Consumption
R.Schreier et all, , "A Flexible 10-300MHz Receiver IC employing a bandpass ΔΣ ADC", 2001 IEEE RFIC Symposium.[7].	0.6µm BiCMOS	4th order band pass with 9 level quantizer, implemented using switched-capacitors.	Variable from 12-24 MHz	88dB SNR in 10KHz bandwidth, 75dB SNR in 200KHz bandwidth.	8mA from 2.7V supply.
E.J. van der Zwan et all, "A 10.7-MHz IF-to-baseband ΔΣ A/D conversion system for AM/FM Radio Receivers", IEEE JSSC, vol. 35, no. 12, Dec2000[8].	0.25µm CMOS	5th order Continuous time modulator with complex conjugate loop filter poles.	21.07 MHz	Peak carrier-to-noise 94dB in 9KHz band width(AM), 79dB in 200KHz bandwidth(AM).	8mA from 2.5V supply (Each).
O.Oliaei et all, "A 5mW Sigma-Delta Modulator with 84-dB Dynamic Range for GSM/EDGE", IEEE JSSC, vol.37, no. 1, Jan 2002[10].	0.4µm BiCMOS	2-2 MASH structure, implemented using switched-capacitors.	13MHz	Peak SNR 83dB in 180KHz bandwidth (ENOB=13.5 bits).	5mW from 1.8V & 2.4V supplies.
R.Schreier et all, "A 50mW Bandpass ΔΣ ADC with 333KHz BW and 90dB DR", IEEE 2002 Solid-state circuits conference, Digest of Tech. papers, vol. 1, 2002[11].	0.35µm BiCMOS	Continuous time Bandpass ΔΣ, with RC, SC resonators & LC filter (L off-chip).	Variable from 9-36 MHz	$@f_{clk}$ = 32 MHz: DR=90dB @ OSR=48 DR=105dB @ OSR=960 $@f_{clk}$ = 26 MHz: SNR = 81dB SFDR = 103 dB	16mW from 3V supply.

Table 1: Comparison of ΔΣ ADC designs.

B. ΔΣ DACs for Transmit sections

DACs are needed in radio transmitters to convert the digital base-band signal to analog form suitable for transmission. A pair of DACs may be used to convert each of the digital I/Q channels to analog form, or the I/Q channels may be converted digitally to IF and then fed into a DAC. Since the digital input to the DAC has no interferers & no extraneous noise, lower-order ΔΣ modulators can be used in the DAC. Note that the low-pass filter following the DAC must sufficiently attenuate high frequency quantization noise components so that they do not corrupt adjacent channels. Mismatch shaping DACs are often used in multi-bit DACs to spectrally shape errors caused by element mismatch out of the signal band. The motivation is to boost the linearity of multi-bit converters (simulations indicate a 1% mismatch in nominal unit-current elements can degrade the SNR of a 17-bit converter from 96dB to 62dB[12]). The technique uses the output of a ΔΣ modulator in a feedback loop to average out the mismatch errors in

the DAC elements. The mismatch transfer function M(z) must be designed appropriately[12].

A tree-structured noise-shaped Dynamic Element Matched (TNSDEM) 9-bit DAC implemented in 0.6µm CMOS is described in [13]. The DAC is clocked at 5MHz and achieves a DR of 80dB in a 100KHz bandwidth, while dissipating 5.2mW.

An optimized ΔΣ modulated transmit section is described in [14]. A complex (I/Q) digital baseband signal is interpolated to IF, and then mixed to final IF(@ f_{IF}). A digital bandpass modulator operating at 4 f_{IF} then quantizes this signal to 1 bit. This 1bit signal is filtered by a 4-tap FIR filter and sent to the Tx driver to be sent off-chip. An external LC filter is also used to filter the output of the modulator and remove spectral images. Even with minimal arithmetic processing on-chip, the design is able to achieve 62dB DR in 12.5 KHz bandwidth.

In conclusion it may be remarked that DACs in wireless transmitters are rarely implemented as ΔΣ DACs, since precisions required are in the range of 4-10bits[6], and other architectures offer better power-performance trade-offs.

C. ΔΣ Fractional-N Frequency Synthesizers

Fig. 3 shows a block diagram of a fractional-N frequency synthesizer using a ΔΣ modulator. For n-bit ΔΣ modulators, it is necessary for the divider to be capable of division by 2^n different moduli. This complicates the divider design. One approach that avoids multi-modulus dividers (MMD) is described in [15]. The MMD is replaced by a dual-modulus divider (DMD) and a modulus extension circuit (MEC). It consists of a divide by 5 counter, and a shift register that multiplexes 2 control signals C_0 and C_2 into the modulator bit-stream. The shift register outputs a 5bit serial bit-stream that controls the divide sequence of the DMD. The ΔΣ modulator is a 3rd order MASH with 1b output, implemented as a cascade of 3 1st order modulators. The synthesizer achieves a phase noise of -90dBc/Hz at 30KHz offset, and a tuning range of 25MHz with 1Hz frequency resolution.

An alternate approach [16], uses a Frequency Synthesizer to modulate a VCO and generate the RF signal. The 2 main problems with this approach are *1*) the data rate is constrained to be low compared to the loop bandwidth, and *2*) the turn-on transients of the Power Amplifier (PA) may disturb the VCO, shifting it to a different frequency. A high degree of isolation is necessary between the VCO and PA. The method eliminates the need for a power-hungry mixer, hence it's popularity. In [16] the data rate is boosted by cascading a digital compensation filter C(*f*) with "inverse-PLL G(*f*) characteristics". The transmit filter low-pass characteristics are made to cancel out the ΔΣ modulator noise high-pass characteristics, thereby resulting in a flat modulation data transfer characteristic. Process variations result in imperfect matching and limit the data rate in practice. With a 2nd order pipelined MASH ΔΣ modulator, the synthesizer fabricated in 0.6µm CMOS achieves phase noise of -132dBc/Hz at 5MHz, satisfying the DECT specification.

The approach of [17] takes the method of [16] a step further by including a calibration circuit on chip. The calibration circuit ensures a close match between the compensation filter and the PLL response. It uses the data sequence to calculate the ideal output phase waveform. The actual output phase waveform is monitored and variations are used to tune the PLL response. Details of the procedure are beyond the scope of this paper, but the design, implemented in a 0.6µm process, is able to achieve a data rate of 2.5 Mb/s using GFSK with phase noise performance of -92dBc/Hz at 100KHz offset from a 1.82 GHz carrier. Table 2 compares performance of the 3 designs.

IV. CONCLUSION

This paper presented a tutorial overview of the subject of ΔΣ modulation in general, and of it's applications towards the wireless market. ΔΣ ADCs are the ADCs of choice for digitizing narrow-band low-power signals to high precision, since they offer superior performance over other architectures. For digital to analog conversion, lower order ΔΣ modulators may be used to meet system specifications.

As VLSI processes shrink the dimensions of transistors, there is a corresponding reduction in output resistance and it becomes increasingly difficult to meet analog performance requirements. Considerable scope exists for innovative circuit design and will continue to exist in the near future.

SiGe technology shows promise to becoming the analog workhorse of the future. The challenge in building ΔΣ modulators is to build them in a digital process, and still meet the design specifications.

Reference	Technology	Architecture	Performance	Power Consumption
T.P. Kenney, et al, Design and Realization of a Digital ΔΣ Modulator for fractional-n Frequency Synthesis", IEEE *Trans.* on Vehicular Technology, vol. 48, no. 2, March 1999[15].	PLD discrete components	MASH3 ΔΣ, with dual modulus divider (DMD) & modulus extension circuit(MEC).	Phase Noise -90dBc/Hz at 30KHz offset from 800MHz carrier, 25MHz tuning range, 1Hz frequency resolution.	-
M.H.Perrot et al, A 27mW CMOS Fractional-N Synthesizer Using Digital Compensation for 2.5-Mb/s GFSK Modulation, IEEE JSSC, vol. 32, no.12, Dec. 1997[16].	0.6μm CMOS	VCO modulation with compensation filter and pipelined 2^{nd}-order MASH ΔΣ.	Ph. Noise -132dBc/Hz at 5MHz offset from 1.8GHz carrier (DECT), 2.5 Mb/s data transmission rate.	27mW
D.R.McMahill et al, A 2.5 MB/s GFSK 5.0-Mb/s 4-FSK Automatically Calibrated Σ-Δ Frequency Synthesizer, IEEE JSSC, vol. 37, no. 1, Jan 2002[17].	0.6μm BiCMOS	VCO modulation with on-chip calibration circuit.	Ph. Noise -92dBc/Hz at 100 KHz from 1.82GHz carrier, data rate 2.5Mb/s using 2-level GFSK, 5Mb/s using 4-level GFSK	78mW

Table 2: Comparison of Frequency Synthesizer Performance.

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