

New type ADC using PWM intermediary conversion

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Abstract – The paper presents a new ADC type that uses an intermediary conversion in PWM signal. The signal is compared with a triangular wave. The pulse width at comparator's output results proportional with the input voltage. Using a simple counter or a frequency-meter like circuit, it is converted into digital words. This is not a very fast converter (up to 10kS/s) but it is easy to build and it asks reduced costs to expand to multiple simultaneous sampling. This design is aimed for FPGAs, having outside it just a comparator per channel. Hardware signal processing is available immediately in the FPGA. Resolution and accuracy can go as far as 12, 14 or 16 bits. The converter presented in the following is 12 bits resolution and measure voltages from -2 V to 2 V. Static errors are also presented.

I. Introduction

Applications as electrical energy or electrical power measurement ask for 2 or 6 simultaneous sampling ADC and signal processing. Usually such circuits (Atmel, Analog Devices, Sames) are either expensive or hard to obtain in small quantities. Most dedicated circuits do not give all the necessary quantities. Also for new developments, dedicated circuits can not be used. In this case, for each channel, the developer must use one ADC and more all must be synchronized.

The present design is dedicated for replacing such circuits in power and energy measurements in mono or triphase circuits and to offer further development possibilities. Using the same triangular wave and two or more comparators synchronous PWM signals will be obtained [1]. Measuring the high states for the PWM signals gives simultaneous results as samples values. The result is not really the value in the sampling moment, but an integral along a small period around the sampling moment.

II. Theoretical background

As mentioned above, the main idea for this A/D converter is to convert first the input signal into a PWM signal. This can be achieved with a simple comparator and a triangular signal generator as shown in Figure 1.

The clock signal coming from the oscillator *O* is divided with 2^n , where *n* is the number of bits of the

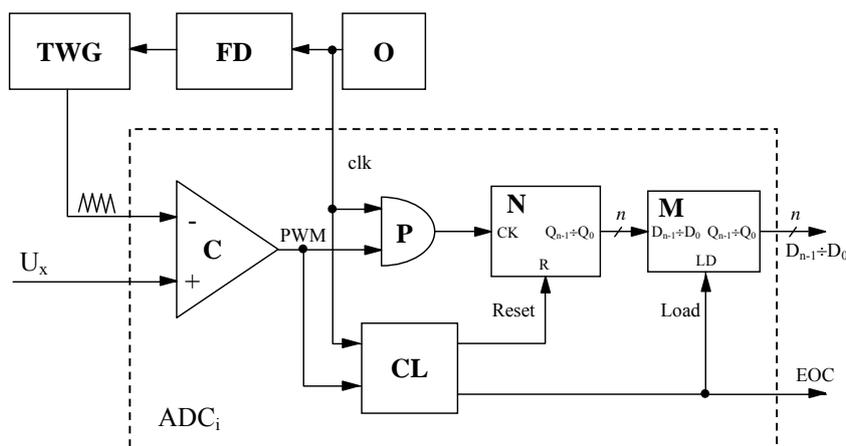


Figure 1. The ADC block diagram

converter, with a frequency divider (*FD*). The divided signal is used to generate the triangular signal (*TWG*). This is used to be compared with the input signal in order to obtain the PWM signal. As long the input signal is under the triangular one, the output of the comparator is in low state, and it stays in high state if it is above. The PWM signal is the gate signal for, while the clock is on the other input of

the AND gate (P). As long as the comparator output is in high state, the clock signal will pass the gate and the counter (N) will count them. At the end of the high state of the PWM signal the total number of clock periods counted by the counter N represents the conversion result. On the basis of clock and PWM signals, the control logic block (CL) generates two signals: *Load* signal for storing data in the memory latch (M) and *Reset* signal for clearing the counter for the next measurement. The "sampling rate" is given by the frequency of the triangle wave signal.

Knowing the period and the amplitude of the triangular signal and clock period, the high state period of the PWM signal can be determined.

The duty cycle of the PWM signal can be computed as

$$\frac{A + U_x}{2 \cdot A} = \frac{T_x / 2}{T_{TW} / 2} \Rightarrow T_x = \frac{T_{TW}}{2} \cdot \left(1 + \frac{U_x}{A}\right) \quad (1)$$

where: A is triangle signal amplitude, U_x is the unknown input voltage, T_{TW} is the period of triangular signal, T_x is period of the high state of the PWM signal. If we replace in the above equation $T_{TW} = 2^n \cdot T_0$ with T_0 the period of the clock signal and n the number of bits, we obtain:

$$T_x = \frac{2^n \cdot T_0}{2} \cdot \left(1 + \frac{U_x}{A}\right) \quad (2)$$

The total number of counts stored after T_x is N_x :

$$N_x = \frac{T_x}{T_0} \quad (3)$$

From (2) and (3) we get:

$$N_x = 2^{n-1} \cdot \left(1 + \frac{U_x}{A}\right) \quad (4)$$

Equation (4) shows that the result is in displaced binary code. This means for an input voltage equal to $-A$ we get 0, for 0 we get 2^{n-1} and for A we get 2^n . Conversions in other codes can be performed inside FPGA.

The waveforms associated to the proposed converter are presented in Figure 2. While the input voltage is 0V, the duty factor of the PWM is 0.5, and it is going higher or lower if the input voltage is greater or respectively lower than 0.

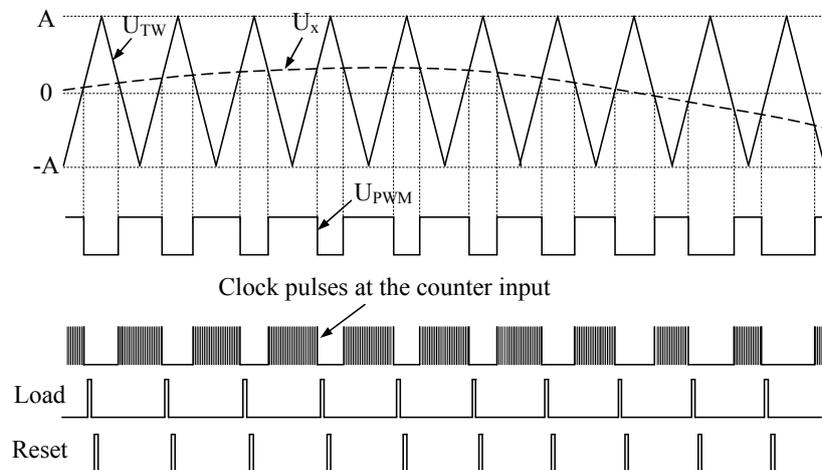


Figure 2 The waveforms associated to the ADC

Usually, for counter like circuits, the counting error occurs. This means a difference of 1 count between successive measurements and it is generated by the fact that the high frequency clock coming from the oscillator is not synchronous with the gate signal. In this case this error does not influence the result while the triangle wave is synchronized with the high frequency clock.

The extension of this converter for multiple channels measurements is simple, because we need only one more comparator per channel. Of course the digital part has to be multiplied with the number of channels too, but the area taken is of about 42 logic cells while FPGAs goes from 1k logic cells up. Keeping outside the FPGA just the comparators and the triangle waveform generator as analogic blocks, the multiple channels ADC looks like in Figure 3.

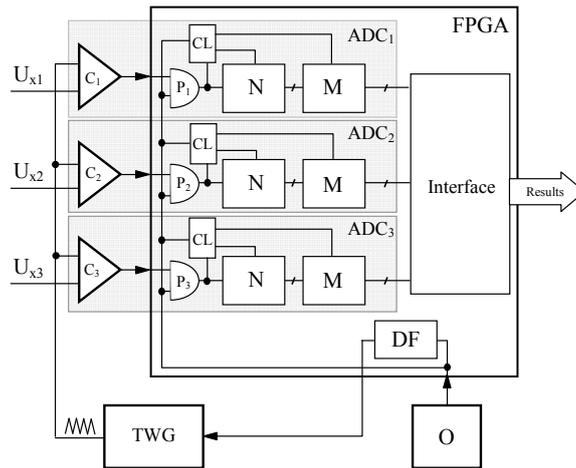


Fig. 3 The multiple channels ADC block diagram

III. Experimental realization of the ADC

Following the block diagram in Figure 1, an experimental ADC has been realized. Far from theory, few problems have to be solved, problems that will be discussed in the following.

The most important thing that contributes to the global accuracy is the quality of the triangular wave signal. Amplitude and linearity are essentials for the full scale error and for the DNL error. Starting from a rectangular waveform it is easy to obtain a triangular wave using an integrator. For high linearity the operational amplifier must have small input currents and the capacitor must have small leakage currents. If no feedback resistor is present, the DC bias point will not be fixed and the output will go into saturation or will have an offset. A DC negative feedback must be introduced [2], but in order to keep the triangle quality this must be added on the non-inverting input, as shown in Figure 4.

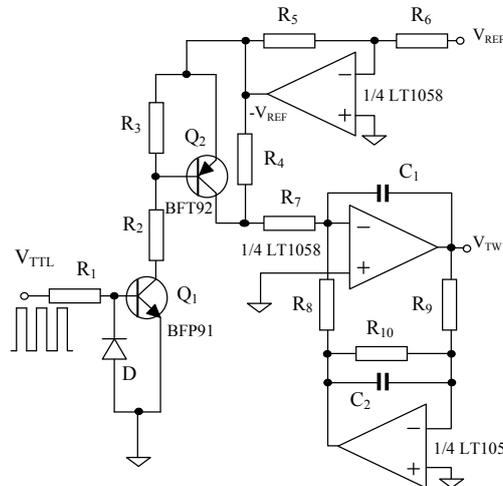


Figure 4. The triangle wave generator

Another problem is related to the triangle amplitude. It decides the scale error, and it acts as reference voltage for this type of ADC. The operational amplifier saturation voltages will vary with the temperature and with the supply voltage. On the other hand the square wave coming from the frequency divider is unipolar. Thus a level shifter has been added before the integrator as shown in Figure 4. Because the fall and the rise times must be shorter than a clock period, fast transistors were used (BFP91 and BFT92). For operational amplifier LTC1058 has been chosen [3]. It has 4 stages per package, very small offset ($180\mu\text{V}$), low input currents (50pA), and high bandwidth (5MHz). The comparator is a fast one (MXL1016) from Maxim [4]. The propagation delay is about 10ns , below the clock period, it has TTL outputs and $\pm 5\text{V}$ power supplies. For offset compensation a trim circuit has been added.

The digital part of the ADC (figure 5) has been implemented in Altera Flex10k20 with a clock oscillator of 25MHz . For 12 bits resolution, the maximum "sampling" frequency will be around 6KHz . For 50Hz power analyzer, the ADC will supply about 120 samples per period. The main counter is

count12b, a 12 bit binary counter. The *clk* input is the 25MHz clock signal and *PWM* is the PWM signal input. The control logic block (*ControlLogic*) generates, on the basis of *PWM* and *clk* the two command signals (Reset and Load). The counter content is transferred into the output buffer on the rising edge of the *load* signal. Data are available on parallel format, either on the falling edge of *load* or on the logic 1 state of *reset*. The waveform associated to this circuit can be observed in Figure 2.

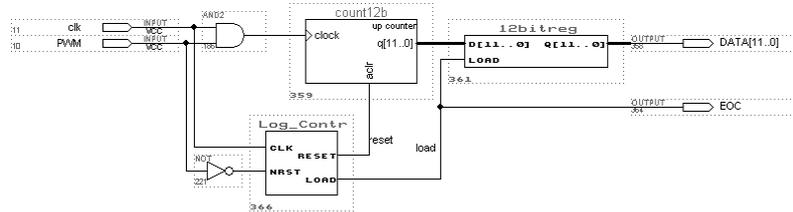


Fig. 5. The digital part of the ADC

IV. Experimental static testing

For static testing, the setup in Figure 6 has been realized. The ADC has been completed with a parallel interface for communication via LPT. The input signal was generated with a Sony-Tektronix AFG310 arbitrary function generator [5] and as reference a Keithley 2000 multimeter [6] have been used. The setup was controlled via GPIB bus with a LabView program.

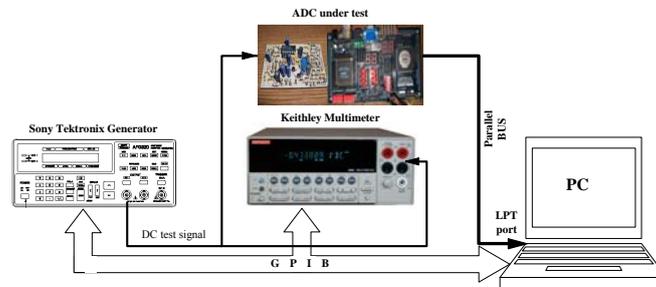


Figure 6. The electronic setup

The input DC voltage has been varied from -2V to +2V and the ADC and Keithley multimeter were recorded. From these data absolute error, INL and DNL were extracted [7]. They are presented in Fig. 7. a, b, c.

As it can be seen, the total absolute error is located between -3 LSB and +3 LSB. The most important contribution to this is the INL, error that is bounded between 1LSB and -2 LSB. The DNL error is good enough (maximum 1LSB) being sized in -0.5LSB to +0.5 LSB interval.

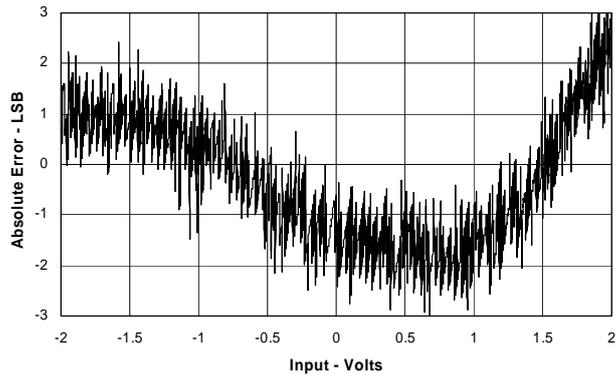
The ADC has been realized with available components. Better performances can be obtained using better components and a unitary construction of the ADC. The intention of this paper was just to prove the method and to show its advantages.

V. Conclusions

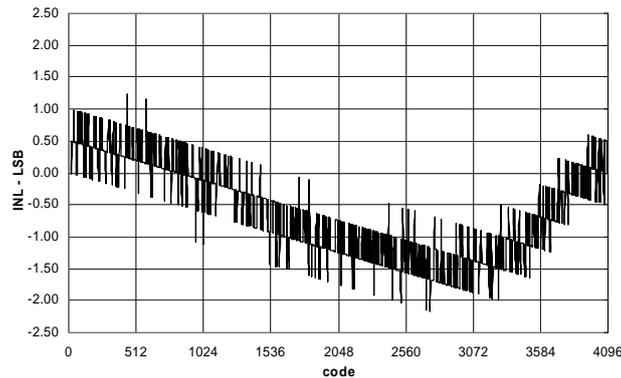
The paper was intended to show a new approach for building a cost effective ADC for low frequencies. The A/D conversion uses an intermediary conversion into PWM signal, which can be considered as conversion in quantity time. Each of the PWM states (high or low) carries information about the input signal. Choosing high or low state, the output will be in displaced binary code or respectively in inverted displaced binary code.

The construction looks complicated at first look, because it contains an analog comparator, a triangle wave generator, a digital frequency-meter, a voltage reference and an oscillator. The main advantage of such ADC is the extension to multiple simultaneous sampling. This can be achieved by adding a comparator and a frequency-meter per channel. If the ADC is based on FPGA, the extension means just an extra comparator for every channel.

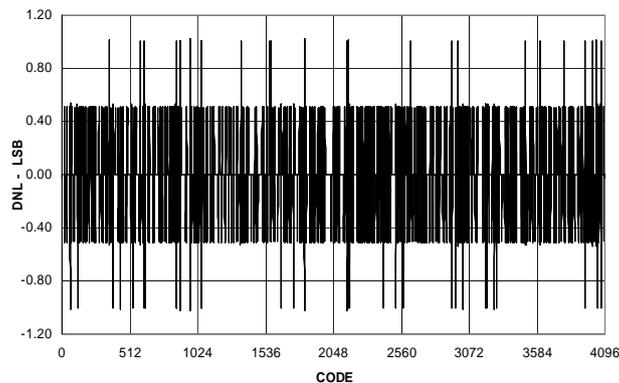
Experimental ADC using this method was realized and tested. Total errors distribution is located in ± 3 LSB domain for 12 bits resolution and ± 2 V full scale.



a)



b)



c)

Fig. 7. The experimental static errors of the ADC

Another possible application is for building a cheap ADC in a microcontroller based system, where just an analog comparator is available. Triangle wave can be generated with a PWM output, and the frequency-meter can be implemented with one timer-counter available on chip.

References

- [1] D. Grahame Holmes, Thomas A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*, Wiley-IEEE Press, October 2003, p. 95.
- [2] C. Kitchin, L. Counts, *A Designer's Guide to Instrumentation Amplifiers 2nd Edition*, Analog Devices, 2004, p. 7.1.
- [3] ****, *LT1057/LT1058 Dual and Quad, JFET Input Precision High Speed Op Amps Datasheet*, Linear Technology Corporation, LT 1205 Rev B, 1989.
- [4] ****, *Ultra-Fast Precision TTL Comparator MXL1016*, Rev 3, Maxim Integrated Products, 2003, <http://pdfserv.maxim-ic.com/en/ds/MXL1016.pdf>.
- [5] ****, *Model 2000 Multimeter User Manual*, Keithley Instruments Inc, March 1997, p. 5.3.

- [6] ***, *AFG310 and AFG320 Arbitrary Function Generator User Manual*, SONY/Tektronix Corp., 1999, p. 4.1.
- [7] Walt Kester, *Analog-digital conversion*, Analog Devices, March 2004, p.5-27.