

# Pseudorandom Noise Generator for ADC Testing

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This paper demonstrates two methods of noise signal generation for ADC testing. Digital pseudo-random number generator based on LFSR and combinations of LFRS are used. The objective of this exploration is to develop device for generation noise signal with uniformly distributed amplitudes. The signal should be used to measure parameters of AD converters using histogram test method.

## 1. Basic of digital white noise generator

Now days there is a large group of pseudo random number generators [1], [2]. We can choose pseudo random number generator with special properties like a correlation, sequence structure or length of generated sequences. Strongly emphasized are binary maximal-length sequences, also known as m-sequences. The research is focused to periodic binary sequences since they can be easily implemented in small hardware compared to aperiodic binary sequences. We choose simple linear feedback shift register (LFSR) as pseudorandom number generator.

Its properties are well known. They are generating m-sequences with length of  $2^n - 1$ , where  $n$  is bit width of used shift register. Distribution of amplitudes is strictly uniform and one of the most important parameter of generated numbers (noise) is PACF (Periodic Auto Correlation Function) defined by formula

$$R_{x,x}(s) = \frac{1}{N} \sum_{i=1}^N x_i x_{i+s} \quad (1)$$

Where  $N$  is period of generator,  $s$  is shift index and  $x$  is output vector of one period of generated noise.

In this exploration, is used LFSR and its bit width is 32 bits and so its period length is maximally  $2^{32} - 1$  with zero suppression logic and with no additional logic  $2^{32} - 1$ .

## 2. Generating uniformly distributed noise signal

One of the methods used to generate uniformly distributed noise signal from normally distributed (Gaussian) noise signal is Step-Gauss method [3]. The problem is that you have to wait whole period of generation and setting the mean value till you can say that output signal is uniformly distributed.

Our new method is to sweep (control) the mean value by other PRNG source with uniformly distributed pseudo random numbers, see Figure 1.

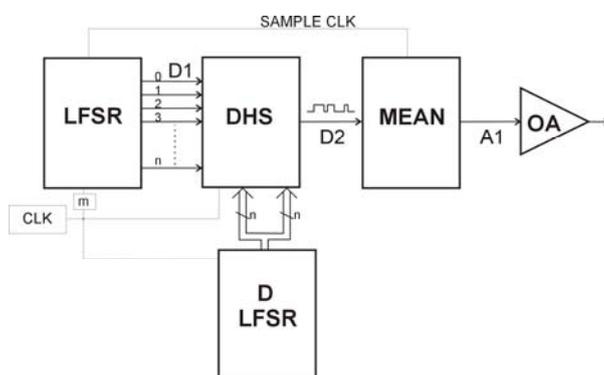


Figure 1. Structure of the digital uniformly distributed white noise generator

DHS is digital hysteresis switch. In this exploration the hysteresis limits are equal so it works only like comparator. It compares output from LFSR against output from DLFSR and produces binary coded signal. LFSR must work  $m$ -times faster than DLFSR, where DLFSR is controlled linear feedback shift register, and  $m$  is integer multiple of  $n$ . The mean block produces exact mean value of input PWM signal, during one period cycle of LFSR. Output signal is sampled by SAMPLE CLK from LFSR. These requirements are necessary for proper function of this generator and from them arises some parameters limits for this device.

The most important parameter is maximal frequency of generated band limited white noise ( $f_{BWNH}$ ) and it can be calculated by this formula

$$f_{BWNH} = \frac{f_{CLK}}{2^n} \quad (2)$$

Where CLK is system clock speed and  $n$  is bit width of LFSR.  $2^n$  is period of LFSR implemented in FPGA with additional logic for zero state suppression. Maximal frequency of generated band limited white noise ( $f_{BWNH}$ ) is limited by the bit-width of LFSR and thus it is better to use LFSR with short period e.g. 6 bits.

Next problem is the whiteness of generated noise, if short period is used. To solve this problem DLFSR from simple PRNG with uniform distribution to bank of PRNGs of bit width  $n$  have to be improved. From that bank, set of uniformly distributed pseudo-random signals are produced. If each of them is used as control signal for DHS block, unique pattern of noise signal is generated. Maximal length of the pattern period is factorial of  $n$  multiplied by  $2^n$ . So minimal frequency of band limited white noise can be calculated by formula

$$f_{BWNL} = \frac{f_{CLK}}{2^n n!} \quad (3)$$

In developed device system clock 20 MHz is used and band width limits for maximal pseudo random pattern are calculated as follows, Table I.

Table I. White noise bandwidth as function of LFSRs

$N$	5	6	11	12
$f_{BWNH}$ [kHz]	625	312.5	9.77	4.88
$f_{BWNL}$ [kHz]	5.21	0.43	0.36	0.015

### 3. Signal simulation

Spectrum of generated signal was calculated, Figure 2.

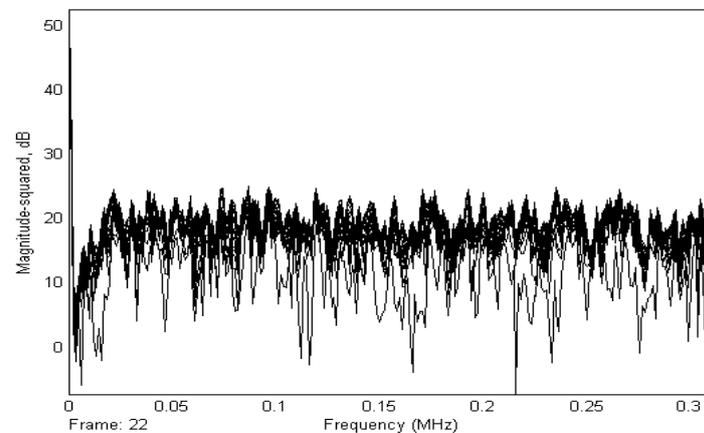


Figure 2. Spectrum of the output uniformly distributed white noise signal.

On the beginning of the spectrum is low drop corresponding to formula (3). For simulation DLFSR with 32 PRNGS of bit width 5 were used. Calculated PACF for generated noise is at Figure 3.

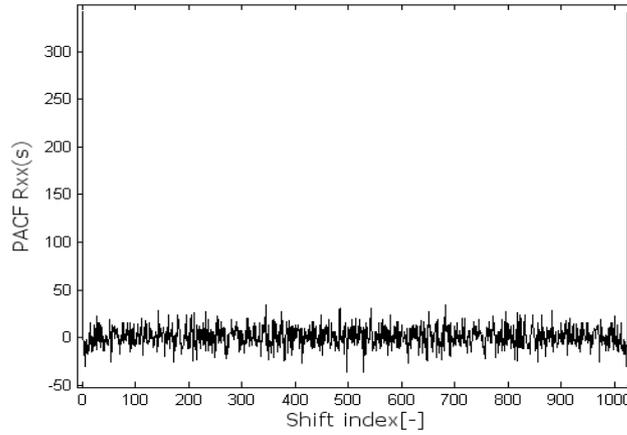


Figure 3. PACF of generated pseudo random numbers with long period

PACF is symmetric around the centered because of the periodicity of generated sequence.

The problem of this arrangement is the DLFSR block. For a proper function showed afore we have to realize full set of different pseudo random sequences by some PRN generator. It means realize  $n!$  LFSRs in this case. This can be realized by memory area where are pseudo random numbers stored.

In this case this design isn't much better than DDS noise generation. It takes too much memory for higher bit resolution and extended generated period.

Better solution is to find different LFSR structure with same bit width and different generated numbers. The condition of each LFSR is to generate maximal pseudorandom sequence. Unfortunately for specified bit width of LFSR there exist only finite and small set of different LFSR generators with maximal sequence (period) as shown in Table II. The  $N$  is length (period) of maximal sequence.

Table II. Number of maximal sequences in dependency of bit width

$n$	$N$	Number of maximal sequences
3	7	2
4	15	2
5	31	6
6	63	6
7	127	18
8	255	16
9	511	48
10	1023	60
11	2047	176
12	4095	144

It is obvious that this solution is better for higher bit width of LFSR because of higher number of possible maximal sequences. We have to redesign formula (3) for respecting, Tab.II. We obtain formula

$$f_{BWNL} = \frac{f_{CLK}}{2^n S} \quad (5)$$

Where parameter  $S$  is the number of maximal sequences. In the Table III are recalculated new values. From table is obvious that minimal generated frequency is higher than generated by first method. In Figure 4 is PCAF of generated noise sequence with the second method for 5 bits LFSR with 6 unique LFSRs in DLFSR bank.

Table III. White noise bandwidth as function of LFSRs bit width

$n$	6	7	11	12
$f_{\text{BWNL}}$ [kHz]	52.08	8.68	0.06	0.03

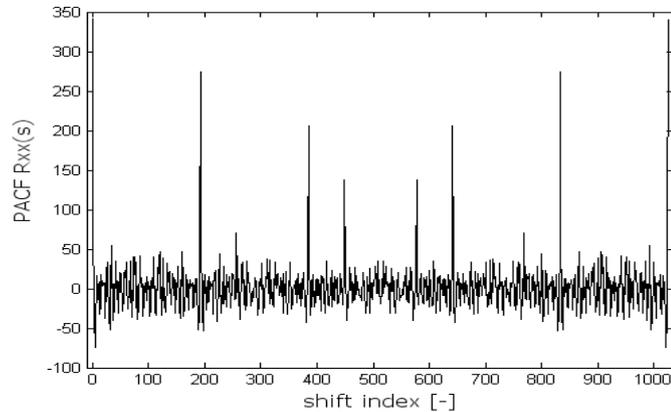


Figure 4. PACF of generated pseudo random numbers with short period

#### 4. Hardware design

For simplicity and possibility of upgrades a Field Programmable Gate Array (FPGA) Acex 1K was used for the design. The LFSR and hysteresis switch are implemented in software. The AHDL programming language was used. The device has possibility to be controlled by PC over the USB interface, so a user can set hysteresis limits and start point of LFSR (i.e. SEED). The USB can also be used as power supply for the device or we can use an external power supply.

#### 5. Conclusion

Simulation and basic experimental measurement has shown, that this is a new simple method of generating noise signal with given statistical distribution and parameters. From simulation result is obvious that for short period can be used first method of generation and for longer periods it's better to use the second one.

#### Acknowledgement

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