Over Sampling Method for the Static Characterization of High Resolution DAC: a Proposal for the IEEE Standard P1658

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Abstract- The paper presents an improved implementation of a method pointed out for the static characterization of the new generation of high resolution Digital to Analogue Converters (DACs). Interesting aspect of this method is that the problem of the signal acquisition with high resolution is shifted to the simpler problem of the signal acquisition with high speed. In particular, the method is based on the comparison of the DAC output voltage with the analogue reference sinusoidal voltage and the detection of the Zero Crossing Sequence (ZCS) of the resulting signal by high speed ADC. The variation of the ZCS respect to that occurring in the sinusoidal reference signal is used to evaluate the DAC transfer characteristic. The improved implementation concerns the proper design characteristics that can be used as selecting criteria of the test equipment. In particular, the substitution of the ADC for the detection of the ZCS by the comparator device is investigated without affecting the accurate detection of the zero crossing. Moreover, the effects of the noise parameters affecting the generator feeding the reference analogue signal, as amplitude and phase noise, on the evaluation of the DAC static characteristic is analysed by considering test equipment using the comparator device and the high speed ADC, alternatively.

I. Introduction

The advancement in both resolution and speed of the new generation of Digital-to-Analogue Converters (DACs) led to an increasing interest to test their static and dynamic performances [1]-[5]. In the paper the aspects concerning the static characterization are deal with the intent to furnish a contribute to the scope of the IEEE working group on the DAC standard [6].
The static characterization of high resolution DAC puts stringent requirements on both the testing procedure and the testing equipments. It is well known that (i) the execution time is exponential function of the DAC bit number [7], and (ii) both the linearity and the resolution of the Analogue-to-Digital Converter (ADC) should be better than that of the DAC under test [8].
In order to overcome any of these inconvenient, there are many well developed and widely adopted test methods [9]-[14]. These can be clustered in two different typologies. One typology includes test methods operating by the analogue comparison of the output signal with the reference voltage [9], [10]. Another typology includes the test methods inferring the non-linearity from the counter of pulses generated in well defined experimental conditions [11]-[13], or generated by high frequency clock [14].
In order to take advantages of both the two typologies, in [15] a new test method was presented and pointed out. It is based on the comparison of analogue signals, and the over sampling the analogue signal at low resolution ADC. In particular, the analogue voltage signal of the DAC is added to the reference voltage signal with sinusoidal shape. The Zero Crossing Sequence (ZCS) in the time domain of the resulting signal is evaluated by over-sampling into the neighbour where the signal changes its sign. The variation vector of the ZCS respect to that occurring in the sinusoidal reference signal is build. This vector is used to evaluate the analogue output voltage of the DAC. By repeating the evaluation for each output voltage level, the transfer characteristic of the DAC can be determined.
In the research given in the paper two fundamental aspects concerning the design characteristics of the testing equipments and involving the method accuracy are investigated. The first concerns the reduction of the ADC resolution without loosing the performance and the accuracy of the method. The reduction of the ADC resolution is important task that makes useful the method for test the new generation higher resolution DACs. The second concerns the effect of the noise parameters affecting the generator feeding the reference analogue signal, as amplitude and phase noise, on the evaluation of the DAC static characteristic. The information about the noise parameters can be used as selecting criteria of the testing equipment to be used.
The paper is organised has follows. The parameters addressing the ADC resolution in the test method are detected by theoretical investigation. The new operating conditions in which the ADC resolution can be reduced to 1 bit resolution are evaluated. The effect of the phase and amplitude fluctuations in the reference signal on the accuracy of the static DAC characterization are determined. The results of numerical tests performed to validate the method in the new operating conditions are discussed.

II. DAC characterization based on the Zero Crossing detection

In [15] the testing method is proposed to evaluate the output voltage V_k of high resolution DAC. The logic and control unit feed the DAC by means of the Digital Input Code DIC_k, k=0,…,2^n-1. For each DIC_k, the output voltage V_k of the DAC under test is added to the sinusoidal reference voltage $v_r(t)$.

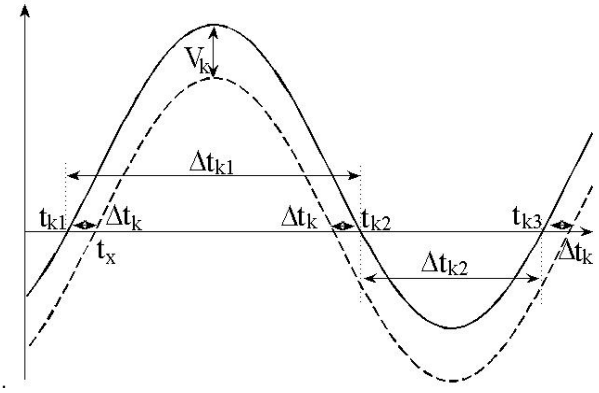


Fig.1. Zero crossing time interval in the case of the offset V_k added to the reference sinusoidal signal.

The resulting signal $v_k(t)$ is:

$$v_k(t) = V \sin(\omega t + \varphi) + V_k \,, \qquad (1)$$

where V and φ are the amplitude and the phase of $v_r(t)$, respectively, and $\omega = 2\pi f$, with f frequency of the reference signal. The resulting analogue signal is sampled by high speed ADC and stored in the PC.

Important innovation of the proposed method is that the amplitude changes of the DAC output voltage are detected not by means of the amplitude changes of the acquired signal, as performed by method present in literature, but by means of the ZCS in the time domain of the resulting signal (1).

Indeed, in the case of reference sinusoidal signal, the sequence in time between two successive zero crossings is characterised by only one constant time interval equal to T/2, with T period of the reference signal. If the constant voltage V_k is added to the reference signal, the sequence in time between two successive zero crossing changes if compared with the sequence obtained from the reference signal, and two different time intervals were defined.

As shown in Fig.1, for the positive offset added to the reference sinusoidal signal, the time interval Δt_{k1} between two successive zero crossings in which the signal has positive values is longer than Δt_{k2}, defined between two successive zero crossings in which the signal has negative values. The sum of these two time intervals is constant and equal to T. Therefore, the time interval Δt_k between the zero crossing of $v_r(t)$ and $v_k(t)$ is:

$$\Delta t_k = \frac{\Delta t_{k1} - \Delta t_{k2}}{4} \,. \qquad (2)$$

The dependence of V_k from Δt_k is [15]:

$$V_k = V \sin(\omega \Delta t_k) \,. \qquad (3)$$

V_k is used to estimate the static parameters that characterizes the DAC as the Least Significant Bit (LSB), the Integral Non Linearity (INL) and the Differential Non Linearity (DNL).

A. Sampling frequency evaluation

From (3) the sampling frequency f_s of the ADC can be determined, once established the expected amplitude resolution (ΔV_x). In fact, the (3) can be re-written as:

$$V_k = V \sin\left(\frac{\omega N_c}{f_s}\right), \qquad (4)$$

where N_c is the number of the acquired samples included into the time interval Δt_k. From (4) the sampling frequency can be extracted once established the expected amplitude resolution ΔV_x. It is:

$$f_s = \frac{2\pi f N_c}{\arcsin\left(\frac{\Delta V_x}{V}\right)} \,. \qquad (5)$$

As expected, the method resolution is linked to the sampling frequency and as ΔV_x decreases f_s increases.

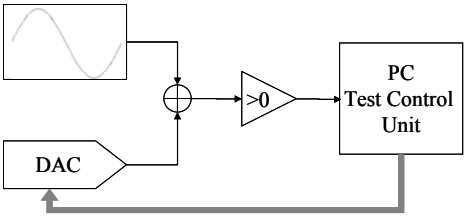


Fig.2. Testing equipment for the static characterization of high resolution DAC employing the comparator device.

B. Evaluation of the bit number of the ADC

Into the neighbour Δt_c of the zero crossing the resulting signal (1) change its sign. Denoted by N_{fs} the number of samples acquired at the frequency f_s into Δt_c, it is $\Delta t_c = N_{fs}/f_s$. Moreover, into Δt_c the minimum change of the ADC output is equal to 2 LSB. By assuming that the slope of $v_k(t)$ is constant into Δt_c, the following relation holds:

$$\frac{2\,\mathrm{LSB}}{\Delta t_c} = \omega\, V \cos(\omega\, t_k + \varphi)\,, \tag{6}$$

where t_k denotes one of the zero crossing instants t_{k1}, t_{k2}, t_{k3}.
From (6) the following expression of N_{fs} can be obtained:

$$N_{fs} = \frac{\mathrm{LSB}}{2\pi\, V\, \cos(\omega\, t_k + \varphi)}\mathrm{OSR}\,, \tag{7}$$

where OSR=f_s/f, LSB= $V_{fs}/2^N$, V_{fs} full scale voltage of the ADC, and N the bit resolution of the ADC. OSR has the value determined from (5).The (7) can be used to set up the parameter LSB in order to reduce N_{fs}, once established the remaining parameters. Reduced value of N_{fs} denotes high accuracy in the evaluation of the ZCS. From (7) can be inferred that the same reduction of N_{fs} achievable by high resolution ADC can be obtained by means of comparator device. Indeed, in this case the factor LSB must be substituted by the threshold value of the comparator. In practice the characteristic value of the threshold voltage is equal to a few μV. Therefore, the proposed test method can be executed by employing the comparator device in the place of high resolution ADC without affecting the expected amplitude resolution ΔV_x. Fig.2 shows the block scheme of the testing equipment employing the comparator device to detect the ZCS and the time interval between two successive zero crossings.
Fig.3 shows the ZCS detection by means of the ADC and the comparator assuming: sinusoidal reference signal V=1.0V and f=1Hz, 12 bit DAC resolution with V_{fs}=0.9V and V_k=0.85V corresponding to the code k=3867, ADC with 6 bit resolution, V_{fs}=±2V and f_s=5kHz. The threshold voltage of the comparator was established equal to 0.06V. The ZCS detected by the comparator, Fig. 3b), and the ZCS detected by the 6 bit ADC, Fig.3c), are practically coincident. As a consequence, the error trend of the evaluation of the DAC static characteristic by using the comparator, Fig.4a), and the 6 bit resolution ADC, Fig.4b), are similar. Differently, by using the 4 bit resolution ADC (Fig.4c) with V_{fs}=±2V the shape of the error trend changes and the error range increases. Indeed, the LSB of the 4 bit resolution ADC is greater than both the LSB of the 6 bit resolution ADC and the threshold voltage of the comparator.

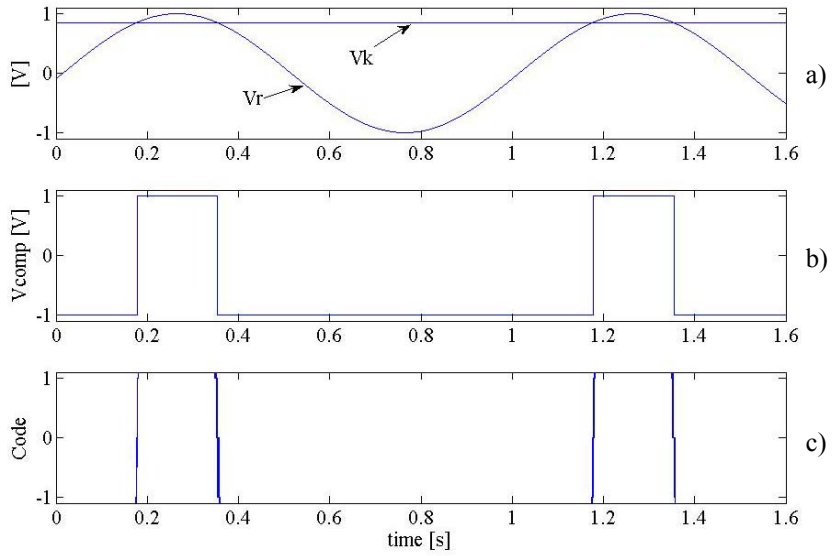
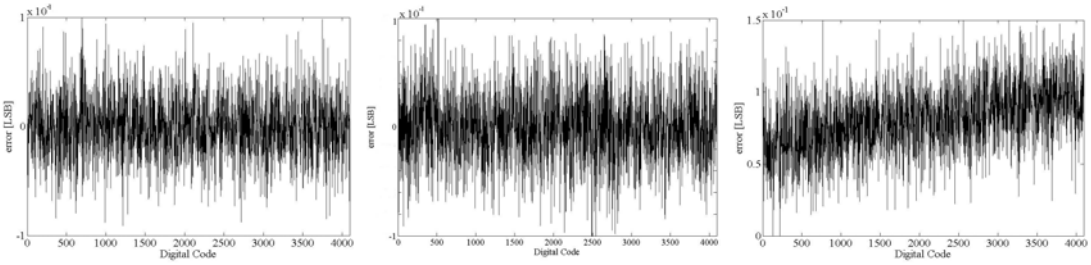


Fig.3 a) reference signal and output voltage of the DAC (with code k = 3867), b) ZCS detected by the comparator, c) ZCS detected by the 6 bit ADC.



a) b) c)

Fig.4 Error trend of the evaluation of the DAC static characteristic
by using a) the comparator, b) the 6 bit resolution ADC, and c) the 4 bit resolution ADC.

III. Effects of the amplitude and phase noise affecting the reference signal

By referring to the test equipment of Fig.2, it can be considered that in real application the signal generator is affected by unwanted amplitude and phase noise. The fluctuation of the reference signal caused by this noise can affects the ZCS in the time domain with different modalities. In particular, the amplitude noise has influence directly on the working operation of the comparator, the phase noise has influence on the spectral purity of the sine wave, and consequently, on the zero crossing instant. These zero crossing changes are taken into account by the method as error introduced by the DAC. Therefore, these alterations have influence on the accuracy of the test. Because the accuracy of the method is function of the quantity of noise that affect the reference signal, it is fundamental to determine the relation between the noise and the error in the DAC output level estimation. This relation is useful to chose the generator characteristics with the required accuracy. In order to investigate about the influence of the generator characteristics, the (1) is rewritten as:

$$v_k(t) = [V + \varepsilon(t)]\sin(\omega t + \phi(t) + \varphi) + V_k \tag{8}$$

where $\varepsilon(t)$ is the instantaneous amplitude fluctuations, and $\phi(t)$ is the instantaneous phase fluctuations. In this condition the zero crossing instants t_{ki}, i=1, 2, 3 corresponding to the V_k values are:

$$t_{ki} = \frac{\arcsin\left(\frac{-V_k}{V + \varepsilon(t_{ki})}\right) - \varphi - \phi(t_{ki})}{\omega}, \; i=1, 2, 3 \tag{9}$$

By assuming as time reference the first zero crossing t_x of the signal $v_k(t)$ with positive slope, is $\varphi=0$.
By referring to the Fig.1, the zero crossing t_{ki}, i=1, 2, 3 evaluated into one period of the reference signal are:

$$t_{ki} = \begin{cases} t_{k1} = t_x - \Delta t_k + \dfrac{\phi(t_{k1})}{\omega} \\ t_{k2} = t_x + \dfrac{\pi}{\omega} + \Delta t_k + \dfrac{\phi(t_{k2})}{\omega} \\ t_{k3} = t_x + \dfrac{2\pi}{\omega} - \Delta t_k + \dfrac{\phi(t_{k3})}{\omega} \end{cases} \tag{10}$$

The substitution in the first of (10) of (2) and (9), with i=1, permits to obtain the following relation, once imposed $t_x=0$:

$$\omega\Delta t_k = \frac{\omega}{4}(\Delta t_{k1} - \Delta t_{k2}) = 2\phi(t_{k1}) - \arcsin\left(\frac{-V_k}{[V + \varepsilon(t)]}\right) \tag{11}$$

The dependence of V_k from Δt_k can be obtained from (11). It is:

$$V_k = [V + \varepsilon(t_{k1})]\sin\left[\omega\left(\frac{\Delta t_{k1} - \Delta t_{k2}}{4}\right) - 2\phi(t_{k1})\right]. \tag{12}$$

This expression highlights the influence on V_k of both the amplitude and phase noise of the reference signal.

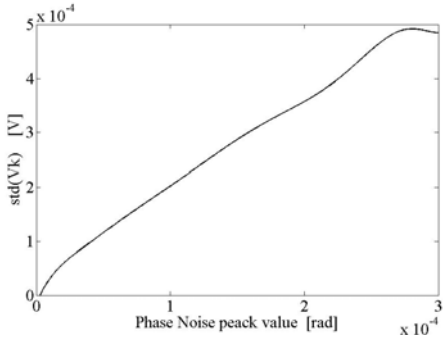


Fig.4 Trend of the standard deviation of the error in the DAC output estimation versus phase noise.

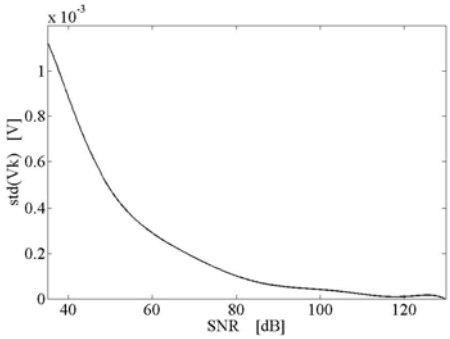
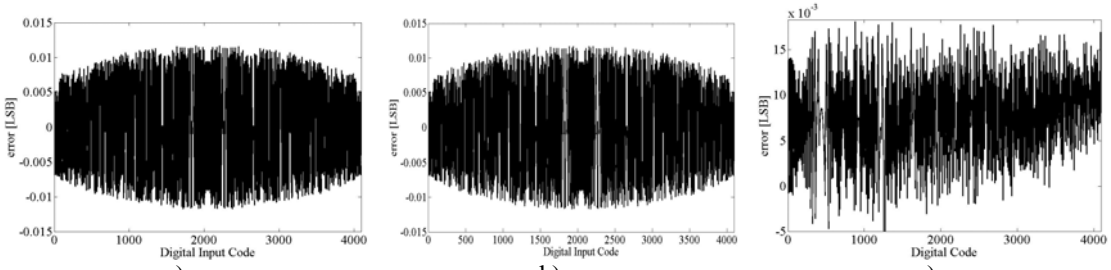


Fig.5 Trend of the standard deviation of the error in the DAC output estimation versus the SNR.

Numerical tests are devoted to investigate about the DAC output evaluation versus the amplitude and phase noise. It is considered the reference signal with V=2.5V, f=200Hz. The tests are executed in Matlab environment, and the error is evaluated as the difference between the imposed value of the DAC output and the estimated level of the DAC output by detecting the ZCS with the comparator.
Fig.4 shows the trend of the standard deviation of the error versus the maximum value of the phase noise. Fig.5 shows the trend of the standard deviation of the error in the DAC output estimation versus the SNR. These two figures furnishes useful information to evaluate the influence of the noise parameters of the generator on the static characterization of the DAC on the basis of the proposed method.

V. Numerical tests

The proposed method with the use of the comparator to detect the ZCS is validated by numerical tests developed in the Matlab environment. The tests are devoted to establish the performances of the method with a reference signal affected simultaneously by amplitude and phase noise typically present on a functional waveform generator.
Fig.6 shows the error trend versus the digital input code in the case of a 12 bit DAC with a full scale value equal to 2V and DNL included into the range [-2, +2] LSB. In the test is considered the reference signal with frequency equal to 200Hz, and amplitude equal to 2.5V. The signal is affected simultaneously by the phase noise equal to -115dBc/Hz and amplitude noise with SNR equal to 130dB. Both these values have been considered by referring to a high performances functional waveform generator. The acquisition system is constituted, alternatively, by a) the comparator, b) the 6 bit resolution ADC, and c) the 4 bit resolution ADC. Each ADC is characterised by sampling frequency equal to 125MHz.
For sake of synthesis, the error trend in the evaluation of the transfer characteristic of the DAC is taken into account, only. In particular, Fig.6a) shows the error trend versus the digital input code in the case of the comparator device, Fig.6b) in the case of the ADC with 6 bit resolution. In both the cases the error trend is similar and it is included into the range [-0.01, 0.01] LSB. The effect of both the amplitude and phase noise of the reference signal is highlighted by the curve shape of the peak envelope. Differently, the peak envelope were constant in absence of fluctuation of the reference signal, as shown in [15]. Fig.6c) shows the error trend versus the digital input code in the case of the ADC with 4 bit resolution. In this case the error trend is included into the range [-0.005, 0.02] LSB and the shape of the peak envelope is different from that of Fig.6 a) and b).



a) b) c)

Fig.6 Error trend of the evaluation of the DAC static characteristic with reference signal affected by phase noise equal to -115dBc/Hz and SNR equal to 130dB, in the case of acquisition by a) comparator, b) 6 bit ADC, and c) 4 bit ADC.

Conclusions

The improvement implementation of a previous presented test method for the static characterization of high resolution Digital to Analogue Converters (DACs) is proposed.
The testing method is based on the comparison of the analogue signal furnished by the DAC output and the reference sinusoidal signal. The successive acquisition of the signal by high speed low resolution ADC is used to detect the Zero Crossing Sequence (ZCS) and the time interval between two successive zero crossings. The variation of the ZCS respect to that occurring in the sinusoidal reference signal is used to evaluate the DAC transfer characteristic.
The improvement of the implementation presented in the paper concerns the proper design characteristics that can be used as selecting criteria of the test equipment. On the basis of the theoretical investigation has been demonstrated that the ADC can be replaced by a comparator device to detect the ZCS without affecting the method accuracy. Results of numerical tests are assessing that the proposed replacement of the device does not affect the accurate detection of the ZCS and the evaluation of the transfer characteristic of the DAC.
On the basis of theoretical consideration and numerical experimentation the effects of the amplitude and phase noise characterizing the signal generator included into the testing equipment are investigated.
Because the proposed test method doesn't require high resolution ADC, and it is robust versus the fluctuation of the reference signal caused by the simultaneously presence of the amplitude and phase noise, it provides a potential practical solution to the static test problem of the new generation of high resolution DACs.

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