Advanced Modeling and Design Evaluation Procedure applied to Pipelined A/D Converter

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Abstract – This paper deals with a prospective approach of modeling and design evaluation applied to pipelined A/D converter architecture. In contrast with conventional ADC modeling algorithms targeted to extract the maximum ADC non-linearity error, the innovative approach presented allows to decompose magnitudes of individual error sources from a measured or simulated response of an ADC device. This qualitative decomposition can significantly contribute to the ADC calibration procedure performed in term of integral and differential non-linearity. This is backgrounded by the fact that the knowledge of ADC performance contributors provided by the proposed method helps to adjust the values of on-chip converter components so as to equalize (and possibly minimize) the total non-linearity error. In this paper, the design evaluation procedure is demonstrated on a system design example of pipelined A/D converter. Significant simulation results of each stage of the design evaluation process are given, starting from the INL performance extraction proceeded in a powerful Virtual Testing Environment implemented in Maple™ software and finishing by an error source simulation and modeling of pipelined ADC structure, suitable for a generic process flow.

Keywords – pipelined A/D converter, ADC modeling, design evaluation, integral and differential non-linearity.

I. Introduction

A. Novel design evaluation approach

Verification of design performance and subsequent device calibration of an A/D converter is a challenging task. This is backgrounded by the fact that the ADC performance depends on many parameters of the analog design part. This becomes apparent especially in complex design structures, such as pipelined A/D converters where the number of circuit components is high due to partitioning into several stages. Therefore, it is very uneasy to develop an explicit expression of the ADC performance contributors, represented in this case by the error sources of underlying circuit instances. Prior works were focused predominantly on a classical ADC modeling and design approach [1], [2] providing only the information about the maximum INL and DNL values, with no subsequent search for the root-cause error contributors. Interesting approach of pipeline ADC calibration was described in [3], [4]. Unfortunately, its application in our work is difficult as the method is dedicated for the post-fabrication measurement rather than design evaluation focused in this paper.

In contrast to this, the innovative approach of design evaluation presented in this article is capable to extract the magnitudes of individual error sources contributing to the ADC performance. Assigning an error mechanism to a specific circuit component or a group of instances, efficient ADC device calibration is possible. At this point, it should be emphasized that the design evaluation approach developed throughout our article represents an efficient tool for design optimization as an inherent part of the integrated circuit design flow.

B. Modeling and parameter extraction of pipelined ADCs

The basic building blocks of pipelined ADCs [6] are organized into consecutive stages, each containing a sample&hold (S&H), a low-resolution ADC and DAC, and a summing circuit that includes an inter-stage amplifier. In our work, a combination of the pipelined architecture with a flash converter type is implemented into converter stages. The combined pipelined-flash ADC provides an optimum balance of speed and resolution, with respect to the power dissipation and the chip size. Therefore, this ADC type becomes increasingly attractive in data conversion. To optimize the pipelined ADC design, performance extraction is necessary as the first step of the evaluation procedure. For this purpose, we developed a powerful Virtual Testing Environment (VTE). The VTE proposed is implemented in Maple™ and consists of program procedures to extract ADC errors expressed in term of integral and differential non-linearity (INL and DNL). To extract the ADC errors, an innovative variant of Servo-Loop method was developed – refer to Section II. In Section III, we follow the concept of an *a priori* ADC modeling with an emphasis to the error source identification and simulation. Subsequently, the design decomposition procedure with respect to the extracted error sources is applied in Section IV. Finally, the work conclusions are drawn in Section V.

II. Advanced Servo-Loop algorithm for parameter extraction

The method concerned is the Servo-Loop, being the core of the proposed virtual testing engine. In our work we apply an innovative approach developed on assumptions discussed in [7]. Consequently, the loop convergence is significantly accelerated, together with the reduced number of iterations. The implementation is shown in Figure 1.
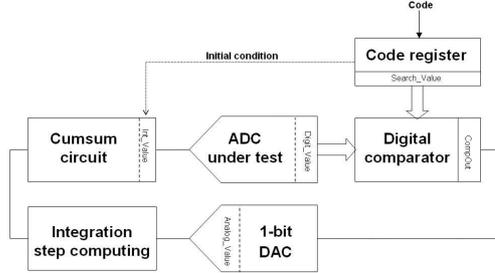

Figure 1. Servo-Loop block diagram

Compared to the standard solution [8], the asset of our Servo-Loop implementation is the following: Cumsum circuit applies a priori known values to the input signal. Convergence process is assisted by an initial condition and by adaptive step refinement of the cumsum block. At this point, adjustment of the step size helps to accelerate the search for the loop equilibrium point as there is less iteration needed to maintain the same INL accuracy. The search complexity is changed from linear to logarithmic. Further details about the novel Servo-Loop algorithm are given in [7].

III. Pipelined ADC modeling

A. Pipelined ADC model description

The ADC model under verification is a pipelined-flash structure proceeding stage-by-stage conversion algorithm corresponding to the scheme shown in Figure 2. The behavioral pipelined flash ADC model consists of n stages, where each stage consists of a N_X-bit A/D sub-converter, D/A sub-converter, summing block and an inter-stage gain block. An N-bit conversion is accomplished by using at least two or more steps of sub-ranging (in this sense called pipelining), starting with the most significant bit (MSB). First, the analog input signal is converted in stage 1 providing N_1-bit resolution. Then, using a DAC with at least N_1-bit accuracy, the result is converted back to analog voltage and subtracted from the input voltage. Next, the difference is multiplied by 2^{N1} and subsequently, the algorithm continues in the same way down to least significant bit (LSB). The flash A/D sub-converter used in our implementation is depicted in Figure 3. Here, an ADC stage with N-bit resolution contains 2^N-1 comparators connected in parallel, with reference voltages set by a resistor network.
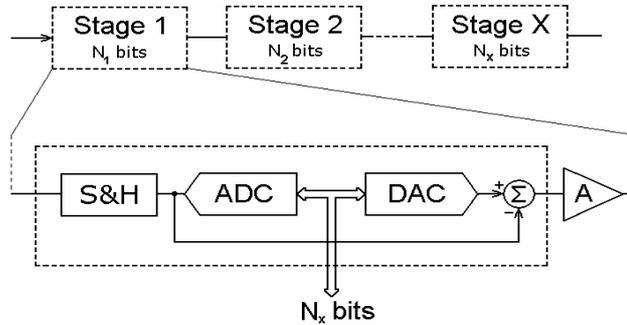

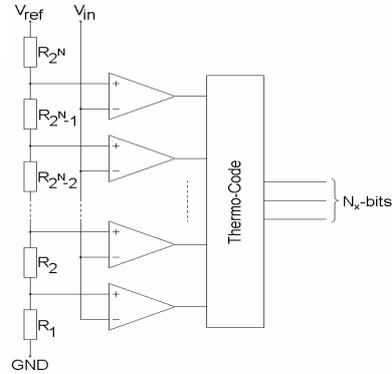Figure 2. Block diagram of pipelined A/D converter

Figure 3. Flash ADC stage

B. Identification of architectural error sources

In the pipelined flash ADCs, errors can be classified into two main groups; systematic ADC error and code-specific ADC error [11]. In our work, we are concerned in code-specific errors from which the dominant ones are: *resistance error*, *comparator offset*, *inter-stage gain error* and finally, the *settling time*. The mechanism of resistance error (labeled as *res_error*) originates in the voltage divider and can be described by the formula (1a). The offset error labeled as *off_error* acts at each separate comparison level and occurs under condition given in (1b). Finally, the inter-stage gain error, in (1c) denoted as *ig_error* acts between two converter stages and its occurrence is specific to the signal direction.

$$R_x' = R_x \cdot \left(1 - \frac{res\_error[ppm]}{10^6}\right), \qquad u_{in} - u_{ref} \cdot \frac{\sum_{i=0}^{k} R_i}{\sum_{j=0}^{2^N-1} R_j} \cdot (1 + off\_error) > 0, \qquad K' = 2^N \cdot \left(1 - \frac{ig\_error[ppm]}{10^6}\right) \qquad (1a,b,c)$$

The error sources described by (1a,b,c) exhibit a linear deviation or scaling with respect to its typical values usually expressed in ppm or absolute units. Beside these sources, a *signal distortion* can occur, caused by non-linear device characteristic of the ADC components. A typical example is the *"tanh-shaped" distortion* of the inter-stage gain block (see amplifier A in Figure 2) caused by the internal stages of the transistor-level OpAmp. The distorted characteristic of the inter-stage gain block (K'=1 is assumed) can be described as:

$$y = C_1 \tanh\left(\frac{x}{C_2}\right) \qquad (2)$$

where x, y are the transfer function co-ordinates and C_1, C_2 are constants. Here, the C_2 constant is chosen upon the desired relative error level and the C_1 constant is calculated so that the transfer function endpoints are [0, 0] and [1, 1]. In Table 1, the distorted transfer characteristic is described by the *error_level* parameter varying from 1 to 3, determining the scale of relative and absolute errors. The resulting waveforms are illustrated in Figure 4a,b.

	Error_level=1 defined as $y = 4{,}082988 \cdot \tanh(\frac{x}{4})$	Error_level=2 defined as $y = 8{,}041623 \cdot \tanh(\frac{x}{8})$	Error_level=3 defined as $y = 18{,}27384687 \cdot \tanh(\frac{x}{18{,}25559128})$
Absolute error	< 0,008	< 0,002	< 0,0005
Relative error	< 0,025	< 0,006	< 0,0015

Table 1. Error levels for tanh-shaped distortion

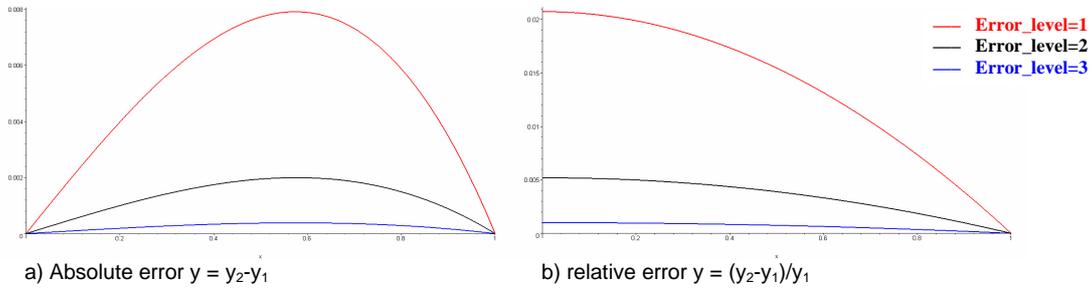a) Absolute error y = y$_2$-y$_1$ b) relative error y = (y$_2$-y$_1$)/y$_1$
Figure 4. Tanh-shaped distortion of the transfer characteristic (K'=1)
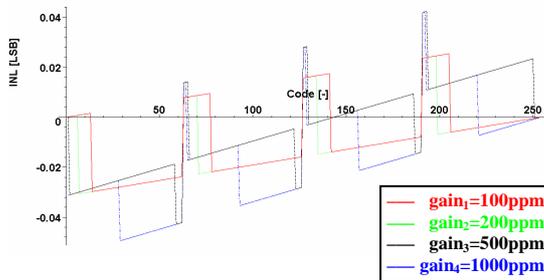

Figure 5. Inter-stage gain error – after 1st section
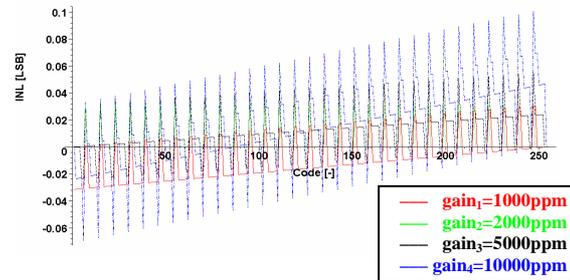(100ppm, 200ppm, 500ppm, 1000ppm)

Figure 6. Inter-stage gain error – after 2nd section
(1000ppm, 2000ppm, 5000ppm, 10000ppm)

C. Error mechanism simulation

In the previous Section, most important error sources occurring in the pipelined ADC architecture were identified. The subsequent step in systematic design decomposition is to recognize the influence of the error sources to the INL characteristic. This can be done by simulating individual error mechanisms so as to sort-out the shape of the corresponding INL waveform and measure its peak-to-peak magnitude.

The VTE was running on the 8-bit ADC with pipelined-flash architecture (2+3+3 bits) from Figure 2 and Figure 3, focusing on the INL contributions of the inter-stage gain and offset error. The first investigated error is the inter-stage gain error, documented in Figure 5 and 6. In Figure 5, the inter-stage gain error between the first and the second section is depicted. On the shape of the error waveforms, a specific dependency of the pulse length on the ADC error magnitude can be observed.

From the simulated patterns in Figure 5 to 7 it is obvious that the ADC system response to the error mechanisms can be classified into two basic groups. In the first error group, the principle of linear scaling and superposition is valid, i.e. the magnitude of the INL and DNL characteristic is directly proportional to the error level [5]. Particularly, this is documented in
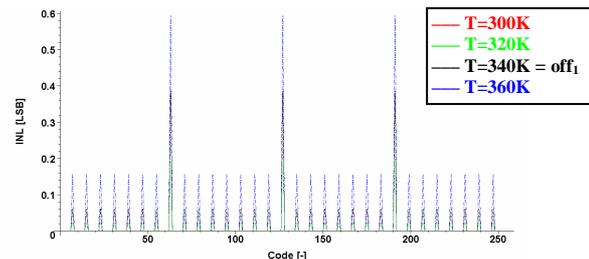

Figure 7. Temperature depencence of the offset error
(T=300,320,340,360K, Tempcoef=40μV/K)

Figure 7 where the comparator offset is shown. In the second group of error sources represented by the inter-stage gain error, the linear superposition principle is violated. This is backgrounded by the quantization of INL contributions from the ADC stages, induced by a set of specific threshold values of error sources. Particularly, if the error source magnitude exceeds a specific value, a significant change of the corresponding INL contribution is invoked. Note that the inter-stage gain error exhibits a periodical influence to the INL characteristic, as it is documented in Figure 5, 6. Such an influence is caused by "forwarding" the ADC error from one stage to the next.
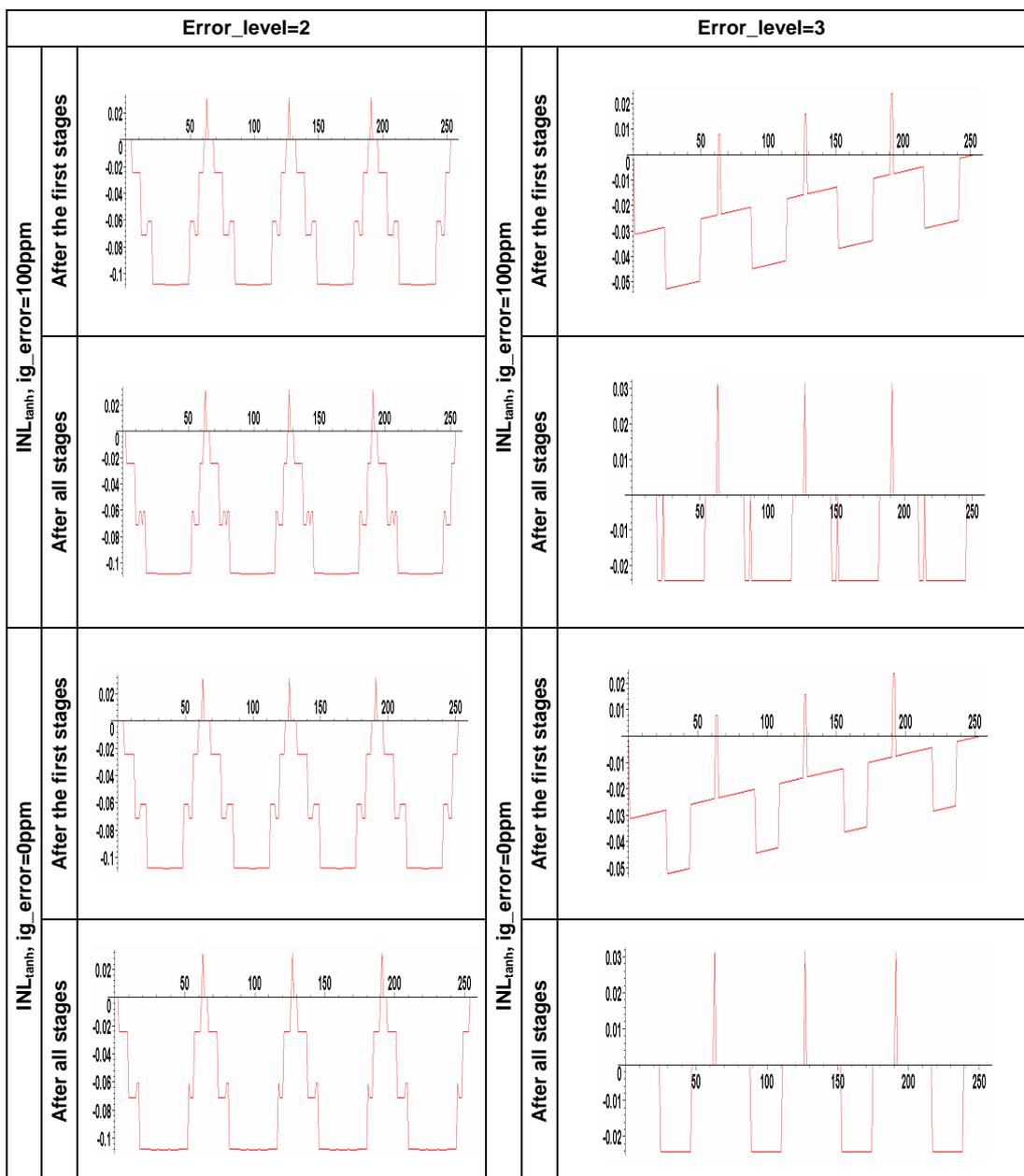

Figure 8. INL response to tanh-shaped distortion for various ig_error level

The INL response of the tanh-shaped distortion of the inter-stage gain block belongs to a special category in the error mechanism simulation. Since this error mechanism describes a non-linear process, the particular influence of other error sources has also to be taken into account; in our case, we consider two values of the inter-stage gain error ig_error = 0ppm and ig_error = 100ppm, respectively. Simulated waveforms for error_level=2 and error_level=3 are shown in Figure 8. Notice that the original (undistorted) waveform for ig_error=100ppm is displayed as the $gain_1$ curve in Figure 5. Apparently, the non-linear distortion creates a masking effect, breaking down the dependency of INL response on the ig_error level. However, for the tanh-shaped error level being sufficiently low (such as in the error_level=3 case), the ig_error influence is still well observable. Because of the masking effect, the tanh-shaped distortion has to be kept at a sufficiently low level in practical design considerations. In such a case, the non-linear effects can be separated in a systematical way so as to allow further decomposition process.

IV. Design decomposition and performance fitting

A. Decomposition Algorithm Background

This section introduces the innovative design decomposition flow carried out to the end of this article. Based on the simulated INL contribution of particular error sources present in the ADC model, we will demonstrate how the error sources and their combination will affect the total INL error. Specifically, the design decomposition will be understood in the sense of identification of the major components and their magnitudes in a simulated ADC device characteristic. As the "real" measured or simulated INL characteristic of a transistor-level ADC device was not available at the time of writing this article, a set of "pseudo-real" characteristics generated by the ADC model was used instead. Despite this fact, the decomposition procedure described below provides a valuable feedback to the modeling procedure.

Applying the linear superposition principle (proven for an ADC response e.g. in [9], [10]), the resulting INL characteristic can be decomposed into a weighted sum of INL characteristics associated with individual error mechanisms. It is important to note that in our work, we demonstrate a suitable extent of the superposition principle to the set of linearly independent INL contributors which are generated by magnitude variation of a single error source. Particularly, it is the case of the ig_error source which clearly violates the linearity assumption, but nevertheless can be attached into the decomposition flow. Fulfilling the conditions defined in Section IIIC, we first assume to separate the non-linear effects (such as the tanh-shaped distortion) from the ADC INL response. Subsequently, we arrange the remaining individual error contributors into the *model matrix* B_{mod}:

$$B_{mod} = \begin{bmatrix} INL1_{gain1}(1) & \cdots & INL1_{gain4}(1) & INL1_{off1}(1) \\ \vdots & \cdots & \vdots & \vdots \\ \vdots & \cdots & \vdots & \vdots \\ INL1_{gain1}(2^N-1) & \cdots & INL1_{gain4}(1) & INL1_{off1}(2^N-1) \end{bmatrix} \tag{3}$$

Apparently from (3), the model matrix contains one column per each error source contributor. Here, N denotes the number of ADC bits used for the purpose of a general notation (N=8 in our case). Note that $INL1_{gain1}$ to $INL1_{gain4}$ correspond to the INL contribution generated by various magnitudes of the inter-stage gain error in the first stage, as it is defined by (1c) and plotted in Figure 5; refer to $gain_1$ to $gain_4$ error sources. Analogously, INL_{off1} denotes the offset error contribution as it is defined by (1b) and depicted in Figure 7; refer to the off_1 error source. The decomposition of the device characteristic INL_{mod} is given by:

$$INL_{mod} = B_{mod}x + \Delta_{LACK} \tag{4}$$

where $INL_{mod} \in R^{2^N}$ is the total characteristic of the pipelined ADC model, x is the vector of weights of individual error sources, $\Delta_{LACK} \in R^{2^N}$ denotes the lack-of-fit underlying error mechanisms not captured by the model matrix B_{mod}. As the first design decomposition step, we estimate the vector of weights as:

$$\tilde{x} = LeastSquares(B_{mod}, INL_{mod}) \tag{5}$$

Subsequently, the lack-of-fit is calculated as follows:

$$\Delta_{LACK} = INL_{mod} - B_{mod}\tilde{x} \tag{6}$$

B. Practical Algorithm Implementation

For practical use with pipelined ADC, the design decomposition procedure established by (3)-(5) needs to be enhanced by determination of error source magnitudes from the components of the vector $\tilde{x}$. With respect to the simulation result given in Figure 6, the offset error fulfills the linear superposition principle with respect to the INL response. The maximum value of the offset error (expressed in volts) can be then expressed as follows:

$$offset\_error = x[5] \cdot off_1 \tag{7}$$

where $x[5]$ is the ratio between the INL curve of measured ADC and INL curve given by the offset error off_1.

For the gain error source, the situation is a bit more complicated, as we need an iteration search procedure to find the error source magnitude. This can be done by the following algorithm:

$$i_{iter} := arg\,max(x[i])^2$$

$$gain_{high} := \frac{gain_{i_{iter}} + gain_{i_{iter}+1}}{2}, gain_{low} := \frac{gain_{i_{iter}} + gain_{i_{iter}-1}}{2} \quad \rightarrow \quad simulate(INL_{gain_{high}}, INL_{gain_{low}}) \tag{8}$$

$$B_{mod}^{red} := \begin{bmatrix} INL_{gain_{low}} & INL_{gain_{high}} \end{bmatrix}$$

$$x := LeastSquares(B_{mod}^{red})\}$$

The algorithm body (8) described above is repeated in a loop until $x([i_{iter}]-1)^2<\varepsilon$. Here, $argmax(x[i])^2$ denotes matrix position of the error component providing the highest magnitude, $gain_{high}$ and $gain_{low}$ specify the interval of error components where the decomposition solution is expected, B_{mod}^{red} is the reduced model matrix with selected INL components $INL_{gainlow}$, $INL_{gainhigh}$, ε is the error tolerance limit by which the iteration algorithm stops.

The concrete asset of the practical algorithm implementation is apparent from Figure 9. Here, the x[1] to x[4] are the error weighs plotted versus the ig_error parameter. Obviously, the global maxima of the x[1] to x[4] curves indicate the concrete values of the ig_error level present in the ADC INL response. In such a way, the inter-stage gain error level can be determined by "filtering-out" the response of the tested device-under-test.
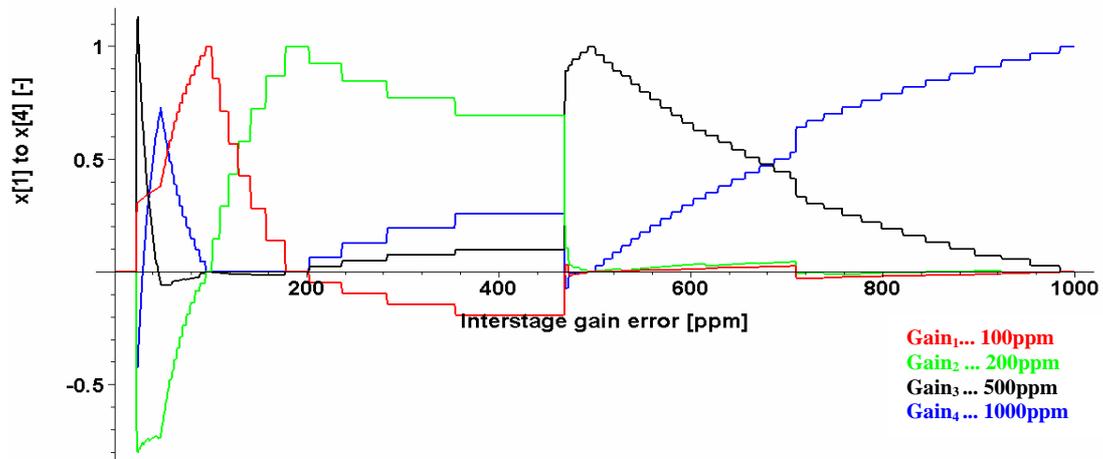
Figure 9. Decomposed model vector coefficients for ig_error parameter

V. Conclusions

The main contribution of this work is the development of a systematical design evaluation methodology suitable for Nyquist-rate A/D converters. Particularly, the decomposition flow was solved and demonstrated for pipelined ADC devices frequently used in IC design solutions. Compared to prior approaches [5], [9], [10], the proposed decomposition algorithm can also proceed the ADC error sources which violate linearity assumption. Practical asset of the decomposition algorithm is expected namely in the custom ADC design with an emphasis on the optimization proceed on behavioral or full transistor-level.

VI. Acknowledgement

References

[1]   M. Parenti, G. Vecchi, A. Boni, G. Chiorboli, "Systematic Design and modeling of high-resolution, high-speed pipeline ADCs", *Measurement*, vol. 37, pp. 334-351, 2005.
[2]   Hung-Chih Liu, Zwei-Mei Lee, Jieh-Tsorng Wu, "A 15b 20MS/s CMOS Pipelined ADC with Digital Background Calibration", *Digest Proc. ISSCC*, article No. 25.2, on-line version, 2004.
[3]   R.Yun, Y.Qin, S.Signell,"LMS-based Calibration of Pipelined ADCs Including Linear and Nonlinear Errors", *Proc. IEEE Conf. ECCTD,* Seville, Spain, pp. 348-351, 2007
[4]   G.Chiorboli, Morandi, "Functional simulation of a technique for background calibration of capacitor mismatch errors in pipelined A/D converters", *Measurement*, vol. 39, pp. 204-212, 2006
[5]   A. Wrixon, M. P. Kennedy: "A rigorous exposition of the LEMMA method for analog and mixed-signal testing", *IEEE Trans. Instrum. Meas.*, vol. 48, No. 5, October 1999, pp. 978-985.
[6]   F. Maloberti, *Data Converters*, pp. 184-199, Springer, ISBN 978-0-387-32485-2, 2007
[7]   O.Šubrt, P. Martinek, C. Wegener, "A Contribution to Advanced Extraction Methods for Static ADC Non-linearity", *Proc. IEEE Conf. IMTC*, CD-rom, 2007.
[8]   The Institute of Electrical and Electronics Engineers, Inc.: *IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters*, IEEE Std. 1241-2000, New York, December 2000.
[9]   O. Šubrt, *Application of SI Technique in A/D Conversion and Its LEMMA-aided Design Evaluation*, Ph.D. thesis at CTU Prague, Faculty of Electrical Engineering, December 2005
[10]   C.Wegener, M.P.Kennedy, "Linear model-based error identification and calibration for data converters", *Proc. DATE, Conf. on Design Automation and Test in Europe*, pp. 630-635, Munich, Germany, March 2003
[11]   L. Michaeli, *Modeling of the analog-digital interfaces*, (in Slovak), Monography TU Košice, ISBN 80-968550-1-8