Measuring deterministic jitter using time interval measurement system

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*Abstract-*This paper describes the method of analysis of the measuring data obtained from low resolution and non-linear Time Interval Measurements System (TIMS) implemented in to FPGA device. Information about quantization and nonlinearity errors of TIMS warrants more precise analytical results during deterministic jitter investigation. The probability density function of the time-interval fluctuation can be very helpful during diagnosing of the jitter sources. As source of signal with deterministic jitter was used digital Delay Locked Loop (DLL) block, embedded in Virtex-E device. The TIMS with the suitable processing of the data allows observe and measure peak-to-peak value of deterministic jitter on the level of resolution of TIMS.

I. Introduction

Jitter is defined as time-interval fluctuation of clock's signal from its ideal positions. Theoretically jitter distribution is characterized by Gaussian Probability Density Function (PDF) but in some real cases jitter distributions contains also meaningful deterministic peaks. In the dedicated blocks of frequency synthesis as Delay Locked Loop (DLL) or Phase Locked Loop (PLL) total jitter contains determined and random components. To estimate both: random and deterministic components of jitter the PDF of the output signal should be analysed. The peaks of deterministic component come from many sources, including duty-cycle distortion, power supply noise or internal circuit structure. The example of PDF is shown in Fig. 1. Precise analysis of the PDF allows separating jitter component [1, 2]. Measurement and analysis of deterministic jitter distribution can significantly improve the diagnostic procedure and find the reason of determined jitter component. Known and applied technique of the measurement of jitter PDF use the high speed digital oscilloscope. The precision time position of the clock edges is calculated from samples obtained as a result of analog-to-digital conversion. The different method of measurement of the jitter PDF based on latching time stamps for each event (rising/falling edge) of the analysed clock signal by high resolution TIMS. In this paper the method of deterministic jitter distribution measurement using low resolution (in relation to the value of the fluctuation) TIMS is presented. Improvement of the histogram resolution is possible by using information about each time stamp accuracy.
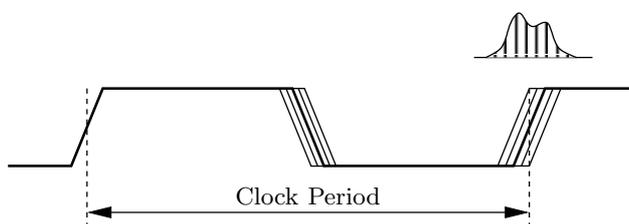

Figure 1. Probability Density Function of the jitter clock signal

II. Experimental setup

As a source of signal disturbed by deterministic jitter the DLL has been used. The DLL unit embedded in Xilinx FPGA devices (Virtex-E family) is used to multiplication the input frequency by two. The fluctuations of the output clock signal contains deterministic jitter components. Jitter distribution of this signal is non-Gaussian and has meaningful deterministic peaks, which strongly depends on the digital DLL architecture, shows Fig. 2 [3]. The distance between peaks equal near τ, when DLL are used as multiplier of the frequency.
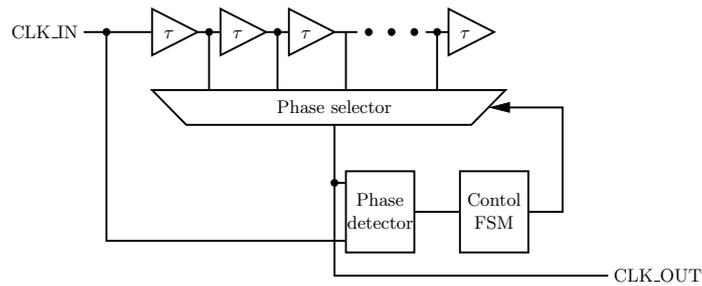
Figure 2. Internal structure of digital Delay Locked Loop [3]

Jitter distribution measurements have been performed by TIMS implemented also in the FPGA XCV300E device [4]. The complete deterministic jitter measurement system also contains the digital oscilloscope LT374 for the verification of measurements. The TIMS have average time resolution equal to 70 ps and double-pulse resolution equal to 8 ns. Block diagram of the TIMS is presented in Fig. 3. The main part of the presented module implemented in the single FPGA (XCV300E) device, consists of tapped delay line built using of the carry chain, a data register, two clock counters, memory blocks and computer interface. Each rising edge on Start/Stop input produce time-stamp. Delay segments τ have spread of the delay from mean value (see on figure 6d) caused by unideal FPGA structure. The total value of the delay line is equal to the half value of the standard clock period. The period of the standard clock equals 10ns. The latched vector of bits is in the not optimal thermometric code and is compressed through the hardware decoder on 6 bits. Correct value of clock counter is chosen by multiplexer. Measured time-stamps data are sent after each measurement cycle to computer by Ethernet interface. The high stable quartz generator about frequency 32 MHz was connected to Start/Stop input.
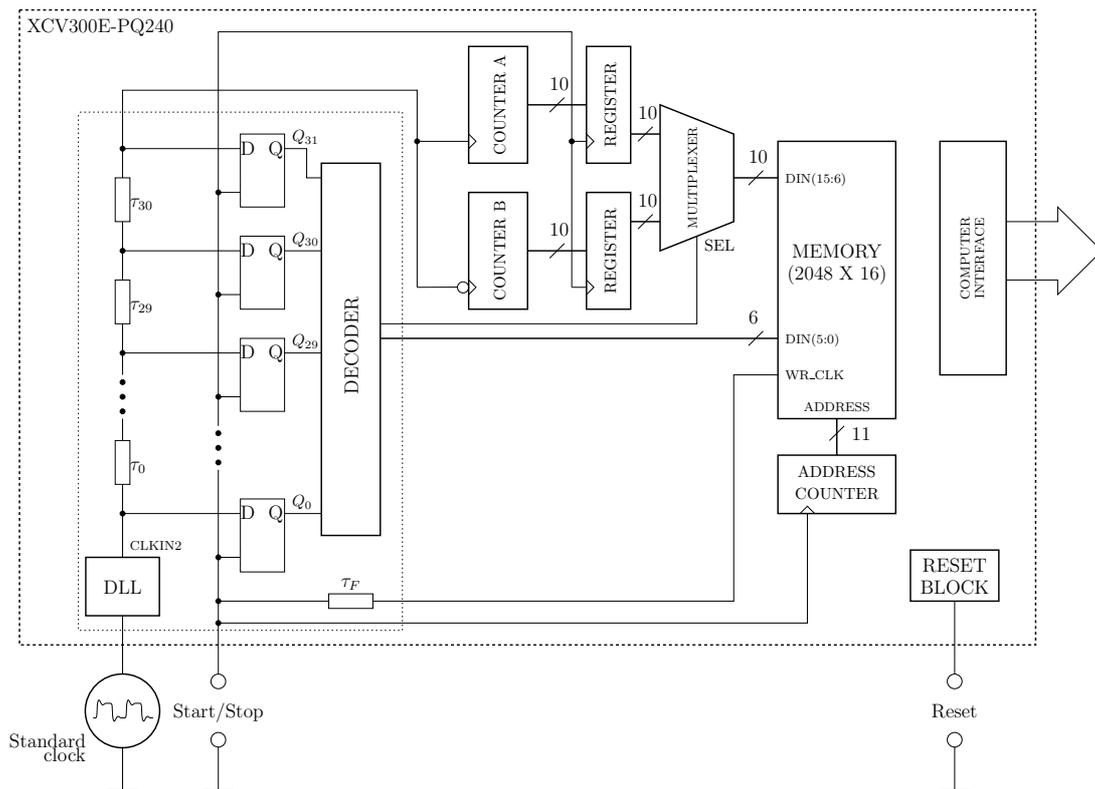

Figure 3. Block diagram of the Time Interval Measurement System

III. The method of building the histogram

Density code test allows precision measurement of all time bin widths of the TIMS. The time bin widths depend on delays τ_0-τ_{30} and standard clock period. Fig. 6d shows characteristic of the module. This characteristic can be used to increase resolution during example bimodal distribution measurement. Distribution of the each time-

interval error is convolution of the normalized rectangular distributions from START and rectangular distribution from STOP (Fig. 4). The time-interval error distribution with quantization and non-linear errors has generally trapezium distribution (when START bin width is equal to STOP bin width it is triangle distribution).
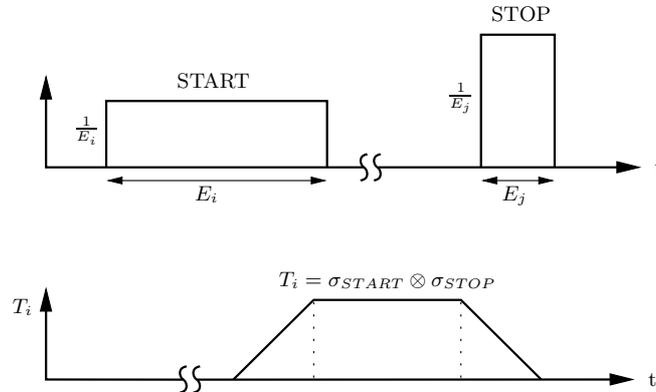

Figure 4. Distribution of the time-interval error

It is possible to build histogram adding to bins value proportional to area of adequate partition of the trapezium distribution built for each time-intervals [5]. The method of the histogram construction for n periods was shown in the Fig. 5. In this way it is possible to obtain higher resolution and eliminate influence of nonlinearity error on the histogram.
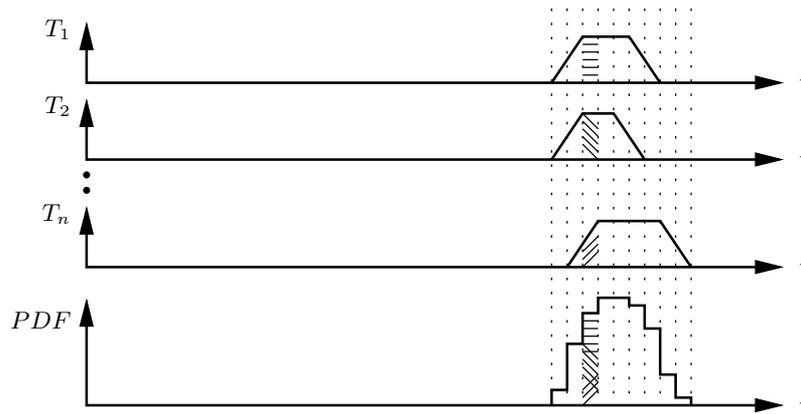

Figure 5. The method of the histogram construction

IV. The results of measurements

The results of jitter measurement using the TIMS are presented in Fig. 6. These histograms have been made by different methods from 500 measurement cycles. Histogram with small resolution shown in Fig. 6a and 6b doesn't allow observing bimodal distribution. The histogram which is shown in Fig. 6a was built assuming ideal linearity of TIMS. The improved histogram obtained using the information about nonlinearity of TIMS is shown in Fig. 6b. Fig. 6c shows the histogram applied with resolution of 3 ps, obtained from 500 periods (time-interval) measured from DLL output. Improvement of the histogram resolution was possible by using the method described above. The improved histogram of higher resolution enable to estimate the deterministic components of analysed jitter.
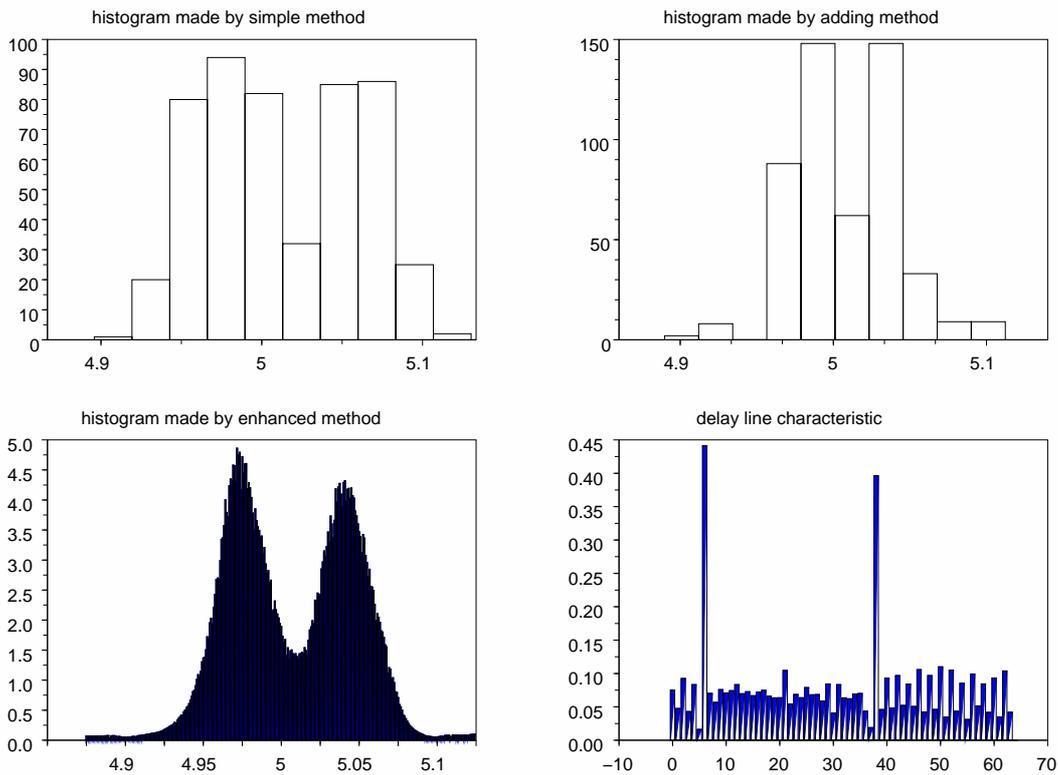
Figure 6. Histograms of time-interval fluctuations obtain by a) simple method with module resolution, c) improve resolution, d) module characteristic

Figure 7 presents histogram of period DLL signal received from the digital oscilloscope. Measurements executed by the oscilloscope confirm the shape jitter PDF.
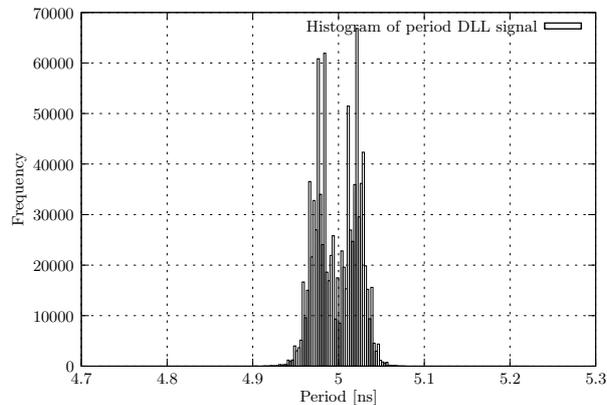

Figure 7. Histogram of period obtain by digital oscilloscope LT374

V. Conclusions

High resolution TIMS with small dead-time provide promising technical solution for jitter distribution measurements. Additionally, the method of analysis presented in this paper allows to increase of histogram resolution to observe deterministic jitter components. It also allows recovering information of time-interval average values. This method can be used also to measurement of deterministic jitter components in case of more complicated signals obtained during digital frequency synthesis or modulation processes. Knowledge of deterministic jitter can be used by diagnostic system to determine the components of signal fluctuations. Other type of jitter e.g. accumulated jitter can be also measured by TIMS..

VI. Acknowledgment

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