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Drift-like errors compensation in intelligent cyclic A/D converters

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Abstract **-** The paper presents the results of investigations on elimination of drift-like errors in intelligent cyclic A/D converters, in particular errors caused by drifts (droops) of voltage at the output of sample-and-hold blocks. The proposed solution is based on application of the extended multi-dimensional algorithm, which estimates simultaneously values of the input sample and the drift rate using the drift rate estimates for correction of the input sample codes. Implementation of the extended algorithm in the intelligent cyclic A/D converters requires only insignificant changes in the digital part of the converter and does not increase their production costs. The motivations to these investigations were results of practical realizations of the intelligent cyclic A/D converter in CMOS technology and difficulties in design of a precise sample-and-hold circuit. The results of selected simulation experiments related to analysis of influence of a droop rate on the final performance of the intelligent cyclic A/D converters employing the standard (one-dimensional) and extended algorithms are discussed and compared in the paper.

I. Introduction

Cyclic analog-to-digital converters are characterized by a relatively long conversion time of one sample which consists of several cycles of processing. Therefore, the errors caused by drifts may be of crucial importance for the worsening of conversion quality. In this aspect, an especially sensitive component of the converter is a sample-and-hold block (S/H) whose output voltage may change over a conversion time (in a hold mode) due to imperfections in the hold capacitor, switch or S/H output amplifier. The changes of the output voltage are caused by a leakage current flowing into or out of the hold capacitor. This effect is known as a droop [1,2] at the S/H output and is specified by a droop rate usually expressed in V/μs or V/ns. Certainly, a droop can be reduced by increasing the value of the hold capacitor, but this increases also acquisition time and reduces the bandwidth of the converter. There are many sophisticated differential circuit techniques often used to reduce the effect of a droop in sample-and-hold circuits [1,2].

In this paper a new approach to solution of such problems is presented. The approach is based on application of the two-dimensional algorithm of estimation of both the sample value and droop rate coefficient. The usage of the proposed algorithm is possible in the new class of cyclic A/D converters, so called intelligent cyclic analog-to-digital converters (IC ADCs) which particularities of design and operation were discussed in [3,4]. The first prototype of IC ADC was realized in CMOS technology [5]. The experience from the process of design and assessment of the prototype and its components inclined to start the investigation on usage of multi-dimensional algorithms enabling simultaneous measurement of parameters of appearing errors and their compensation.

IC ADCs employ a new conversion method based on application of the analytical approach to optimisation of adaptive estimation algorithms [6] and, in conventional form [3,4], use its simplest one-dimensional version. This paper focuses on application of multi-dimensional versions of the algorithms [6] in IC ADCs, which enables drift-like errors parameters estimation and compensation. General principles of application of these algorithms to elimination of errors and interferences are presented in [7].

II. IC ADC operation principles

An essential feature distinguishing intelligent cyclic A/D converters from other known cyclic A/D converters is computing of input samples codes in the form of long binary words of the fixed length N_{comp} (e.g. N_{comp} = 16, 24 or 32-bit) using adaptive algorithms based on the approach [6]. A simplified block diagram of IC ADC, which illustrates the principles of its functioning, is presented in Fig.1.

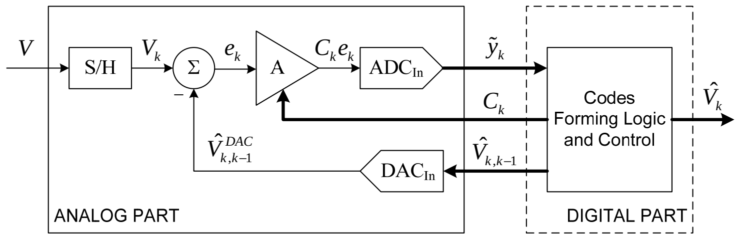

Figure 1. General block diagram of IC ADC.

The input signal $V(t)$ is sampled in the sample-and-hold (S/H) block and a voltage $V(mT) = V$ (for notational convenience, the time index is further omitted) is held during the sampling interval T permitting to complete K cycles of conversion. In each k-th cycle ($k = 1,2,\ldots,K$) of conversion the voltage value at the input of an analog subtractor Σ should be constant, that is $V_k = V$. The second (negative) input of the subtractor Σ is connected to the output of an internal D/A converter (DAC_{In}). DAC_{In} forms the analog voltage $\hat{V}^{DAC}_{k,k-1}$ from the binary N_{DAC} -bit code ($N_{DAC} < N_{comp}$) of the estimate $\hat{V}_{k,k-1}$ calculated in the previous stage. The subtractor Σ forms a residual signal $e_k = V - \hat{V}^{DAC}_{k,k-1}$, which is routed to the input of the controlled gain amplifier A with the gain C_k. The amplified signal $C_k e_k$ is routed to the input of the internal coarse fast (N_{ADC} = 1÷6 bits) A/D converter (ADC_{In}). The adequate model of N_{ADC} -bit code $\tilde{y}_k$ formed by ADC_{In}, which takes explicitly into consideration the possible saturation of the converter caused by the limited input range $[-D, D]$ of ADC_{In}, is as follows:

$$\tilde{y}_k = \begin{Bmatrix} C_k e_k & \text{for} & C_k |e_k| \le 1 \\ D \,\text{sign}(e_k) & \text{for} & C_k |e_k| > 1 \end{Bmatrix} + \xi_k , \tag{1}$$

where ξ_k is a noise related primarily to quantisation in ADC_{In}. N_{ADC} -bit code $\tilde{y}_k$ formed by ADC_{In} is routed to the digital part of the converter which computes the estimate (code) $\hat{V}_k$ of the input sample on the basis of its value calculated in the previous stage and the output code of ADC_{In} according to the following relationship:

$$\hat{V}_k = \hat{V}_{k-1} + L_k \tilde{y}_k . \tag{2}$$

Sub-optimal values of gains C_k (maximal under given acceptable probability of overloading μ) as well as corresponding values of coefficients L_k can be found using the analytical approach proposed in [6]. In one-dimensional case we have:

$$C_k = \frac{D}{\alpha\sqrt{\sigma_\nu^2 + P_{k-1}}}, \qquad L_k = \frac{C_k P_k}{\sigma_\xi^2 + C_k^2 \sigma_\nu^2} . \tag{3}$$

These values minimize, for each $k = 1,2,\ldots, K$, the mean square error (MSE) of conversion:

$$P_k = E[(\hat{V}_k - V)^2] = \frac{(\sigma_\xi^2 + C_k^2 \sigma_\nu^2) P_{k-1}}{\sigma_\xi^2 + C_k^2 (\sigma_\nu^2 + P_{k-1})} \tag{4}$$

under probability of overloading not greater than a given acceptable value μ. Saturation factor α in (3) is determined by the permissible probability μ of overloading and in Gaussian case satisfies the equation $\Phi(\alpha) = (1-\mu)/2$, where $\Phi(\alpha)$ is the tabulated Gaussian error function. Variables σ_ν^2 and σ_ξ^2 in expressions above represent the variances of noises ν_k at the output of the subtractor Σ (caused, among others, by the finite resolution of DAC_{In}) and ξ_k at the output of ADC_{In} (caused, first of all, by quantisation), respectively.

The usage of the algorithm (2-4) and its modifications [8,9] enables achievement of the IC ADC resolution greater than in conventional cyclic A/D converters with similar analog parts and comparable probability of saturation [3,4]. Application of long-bit operations in IC ADC permits to remove inevitable in conventional cyclic A/D converters constraints on the gain coefficients which should have only the values equal to integer powers of two. Impossibility to set the gains to each theoretically required value restricts possibilities to utilize entirely the resources of the analog components of IC ADC for reduction of influence of technological errors and noises. To avoid overloading in each cycle, designers must artificially decrease the gains of amplifiers and use so-called redundant bits. This results in incomplete utilization of the resources of converter components and decreases its final resolution. In IC ADC, potential overloading is excluded by setting the components parameters in each cycle to the close to optimal values determined analytically.

III. Extended algorithm in case of drift-like errors

In the case of drift-like errors occurrence, the following model of the voltage $\tilde{V}_k$ (in order to distinguish the drift case we use the upper wave over V_k) at the output of S/H block can be assumed:

$$\tilde{V}_k = V + \beta d_k \,, \tag{5}$$

where V is the measured value of the input sample and β is the unknown rate (amplitude) of a drift-like (e.g. droop) component, which has the known form d_k, e.g. $d_k = k - 1$ (linear) or $d_k = 1 - e^{-\gamma(k-1)}$ (exponential), where k is the cycle number (k = 1,2,…, K). Typical runs of the voltage at the S/H output are shown in Fig. 2: a) linear drift $d_k = k - 1$, $\beta = -10^{-4}$, b) exponential drift $d_k = 1 - e^{-\gamma(k-1)}$, $\beta = -2\cdot 10^{-3}$, $\gamma = 10^{-1}$.

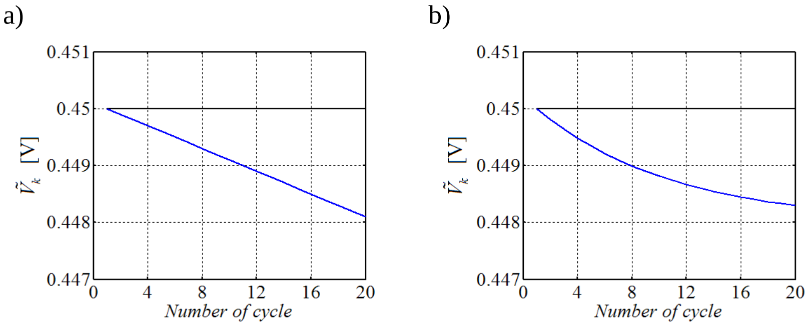

Figure 2. Trajectory of input voltage in case of linear (a) and exponential (b) drift.

The considered voltage (5) can be presented in the form of the regression type model:

$$\tilde{V}_k = \boldsymbol{\theta}^T \boldsymbol{X}_k \,, \tag{6}$$

where $\boldsymbol{\theta} = [V, \beta]^T$ is a vector of unknown parameters to be estimated and $\boldsymbol{X}_k = [1, d_k]$ consists of two known deterministic components. Our goal is to find the optimal method of estimation of both sample value V and the drift coefficient β. In this case, the residual signal has the form $e_k = \tilde{V}_k - \hat{\tilde{V}}^{DAC}_{k,k-1}$, where $\hat{\tilde{V}}^{DAC}_{k,k-1}$ is the prediction of the value of the voltage $\tilde{V}_k$ at the output of S/H block in the k-th cycle calculated on the basis of estimates $\hat{\boldsymbol{\theta}}_{k-1} = [\hat{V}_{k-1}, \hat{\beta}_{k-1}]^T$ obtained in previous (k – 1)-th cycle:

$$\hat{\tilde{V}}_{k,k-1} = \hat{\boldsymbol{\theta}}^T_{k-1} \boldsymbol{X}_k = \hat{V}_{k-1} + \hat{\beta}_{k-1} d_k \,. \tag{7}$$

The recursive equation for the optimal estimates is as follows

$$\hat{\boldsymbol{\theta}}_k = \hat{\boldsymbol{\theta}}_{k-1} + \boldsymbol{L}_k \tilde{y}_k \tag{8}$$

and the sub-optimal values of the gains C_k (maximal under given acceptable probability of overloading μ) as well as corresponding values of coefficients $\boldsymbol{L}_k = [L^{(1)}_k, L^{(2)}_k]^T$ can be found using the multi-dimensional version of the algorithm of optimal signal parameter estimation [6]:

$$C_k = \frac{D}{\alpha\sqrt{\sigma_\nu^2 + \boldsymbol{X}_k^T \boldsymbol{P}_{k-1} \boldsymbol{X}_k}} \,, \qquad \boldsymbol{L}_k = \frac{C_k \boldsymbol{P}_{k-1} \boldsymbol{X}_k}{\sigma_\xi^2 + C_k^2(\sigma_\nu^2 + \boldsymbol{X}_k^T \boldsymbol{P}_{k-1} \boldsymbol{X}_k)} \,, \tag{9}$$

$$\boldsymbol{P}_k = E[(\hat{\boldsymbol{\theta}}_k - \boldsymbol{\theta})(\hat{\boldsymbol{\theta}}_k - \boldsymbol{\theta})^T] = \boldsymbol{P}_{k-1} - \frac{C_k^2 \boldsymbol{P}_{k-1} \boldsymbol{X}_k \boldsymbol{X}_k^T \boldsymbol{P}_{k-1}}{\sigma_\xi^2 + C_k^2(\sigma_\nu^2 + \boldsymbol{X}_k^T \boldsymbol{P}_{k-1} \boldsymbol{X}_k)} \,. \tag{10}$$

Initial conditions for the algorithm (8-10) are usually as follows $\boldsymbol{\theta}_0 = [0,0]^T$, $\boldsymbol{P}_0 = diag(\sigma_V^2, \sigma_\beta^2)$, where σ_V^2, σ_β^2 are the variances (a priori) of the converted voltage (usually $\sigma_V^2 = FSR^2/12$) and the drift coefficient, respectively. From the practical point of view, implementation of the extended algorithm (8-10) in IC ADC resolves itself into additional implementation of the relationship (7) and two following operations:

$$\hat{V}_k = \hat{V}_{k-1} + L^{(1)}_k \tilde{y}^{corr}_k \,, \qquad \hat{\beta}_k = \hat{\beta}_{k-1} + L^{(2)}_k \tilde{y}^{corr}_k \tag{11}$$

instead of one operation (2) as in the case of the standard IC ADC. It is worth noticing that calculations of gains and coefficients (9-10) are performed off-line before their implementation in the converter.

IV. Results of computer experiments

In order to verify the proposed method, the appropriate models of IC ADC employing both standard (2-4) and extended (8-10) algorithms as well as simulation tools were developed in MATLAB environment. In simulation, the correction related to the finite resolution of DAC_{In} was taken into consideration, that is instead of $\tilde{y}_k$ the corrected value $\tilde{y}_k^{corr} = \tilde{y}_k - C_k \Delta\hat{\tilde{V}}_{k,k-1}^{DAC}$ was used, where $\Delta\hat{\tilde{V}}_{k,k-1}^{DAC} = \hat{\tilde{V}}_{k,k-1} - \hat{\tilde{V}}_{k,k-1}^{DAC}$ is the difference between the calculated in the digital part N_{comp} -bit long estimate and its N_{DAC} -bit long version cut at the input of DAC_{In} [9]. The values of parameters in simulations were as follows: $N_{ADC} = 4$, $N_{DAC} = 12$, $D = 1$ [V], $\alpha = 3$, $\sigma_V^2 = FSR^2/12$, $V_0 = 0$, $\sigma_\beta^2 = 10^{-8}$, $\beta_0 = 0$. The values of basic IC ADC parameters assumed in simulations are the same as the values of the parameters which were implemented in the first prototype of IC ADC realized in CMOS technology [5].
In the first series of experiments the single runs of estimates are analysed. The plots presented in Fig. 3 illustrate the results of conversion of the input sample for $V = 0.45$ [V] in a presence of linear drift at the S/H output with the drift rate $\beta = 10^{-4}$ [V].

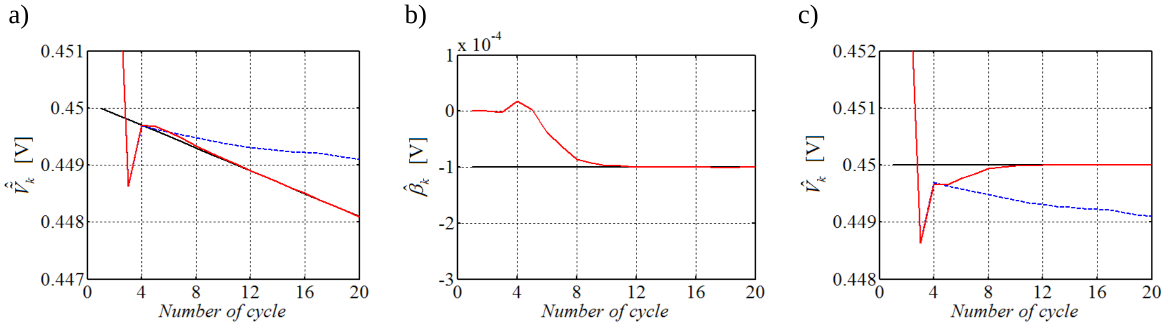

Figure 3. Typical runs of estimates formed by IC ADC with standard (blue dashed lines) and extended (red continuous lines) algorithms, estimates of: (a) voltage at S/H output, (b) drift rate, (c) input sample value.

Fig. 3a shows typical runs of estimates $\hat{\tilde{V}}_k$ of the voltage $\tilde{V}_k$ at the output of S/H block in subsequent cycles of conversion for both the standard (one-dimensional) and extended (two-dimensional) algorithms, blue dashed and red continuous lines, respectively. The trajectory of estimates of the drift rate obtained by the extended algorithm is presented in Fig. 3b, whereas Fig. 3c shows typical runs of estimates $\hat{V}_k$ of the input sample V for the standard and extended algorithms. The plots from Fig. 3a indicate a significant advantage of the extended algorithm over the standard one in ability of tracking of changing input voltage.
In the next series of simulations, the properties of application of the standard and extended algorithms in IC ADC were investigated on the basis of the behaviour of empirical values of Effective Number of Bits (ENOB) [10]. Test input signals were generated as sequences of random uniformly distributed (in the input range of IC ADC) signal samples $V^{(m)}$ $(m = 1,\dots,M)$, where M is the number of samples converted in the given experiment (M = 10 000). For every input sample $V^{(m)}$ concerned in simulation experiments, the value of the drift parameter was generated randomly with the Gaussian distribution $N(0,\sigma_\beta^2)$ for the standard deviation $\sigma_\beta = 10^{-4}$ [V]. The empirical values of ENOB were calculated using the following formula [3,4]:

$$\hat{N}_k = \frac{1}{2}\log_2\left(\frac{P_0}{\hat{P}_k}\right), \qquad \hat{P}_k = \frac{1}{M}\sum_{m=1}^{M}[V^{(m)} - \hat{V}_k^{(m)}]^2 , \tag{12}$$

where $P_0 = FSR^2/12$. Fig. 4 shows plots of ENOB versus the number of cycle obtained for both standard (blue dashed line) and extended (red continuous line) algorithms used in IC ADC. The blue dashed plot confirms that IC ADC with the standard algorithm is not able to work properly in the case of drift occurrence, but ENOB obtained for IC ADC employing the extended algorithm (red continuous line) continues further increase after a short break in 5-th cycle.

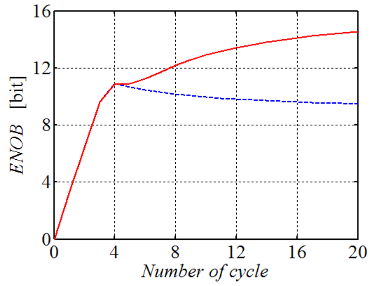

Figure 4. ENOB versus number of cycle for the standard (blue dashed line) and extended (red continuous line) algorithms used in IC ADC and for $\sigma_\beta = 10^{-4}$ [V].

In the last series of simulation experiments the empirical values of ENOB for the standard and extended algorithms applied in IC ADC were compared for different values of the standard deviation σ_β of drift coefficient. Fig. 5a relates to the standard algorithm and Fig. 5b to its extended version.

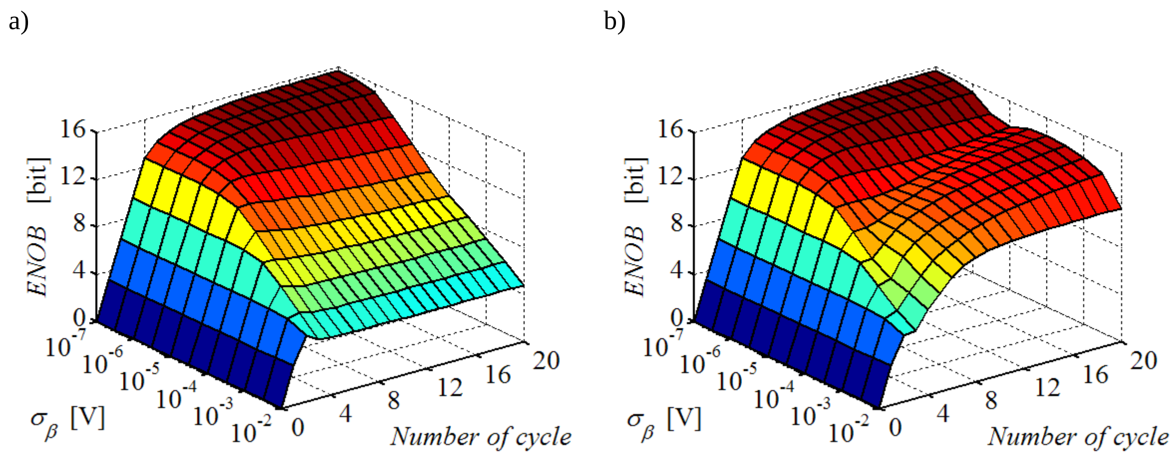

Figure 5. ENOB for different σ_β obtained for the standard (a) and extended (b) algorithms used in IC ADC.

Figures 5a and 5b explicitly demonstrate that drift occurrence degrades performance of the standard IC ADC expressed in ENOB proportionally to the drift (droop) rate, while IC ADC with the extended version of algorithm can work satisfactorily in the wide range of the drift coefficient values.

V. Conclusions

The proposed application of the extended algorithm with drift parameter estimation enables preservation of IC ADC capability to accurate conversion of input samples in the presence of drift (droop) which is impossible in the case of conventional cyclic A/D converters. Of great importance for practice is the fact that the application of the extended algorithm requires no change in the architecture of the conventional IC ADCs but only insignificantly extends the digital part of the converter which practically does not change the production costs of the converters. Certainly, simultaneous estimation of the sample amplitude and drift rate causes an increase of cycles number needed to obtain assumed resolution and, in consequence, diminishes a sampling rate in comparison with the situation when there is no drift.

The proposed approach can be also used in the case of occurrence of errors of other types, e.g. harmonic interferences. Then, suitable extension of the vector of known deterministic components and appropriate modification of the vector of unknown parameters to be estimated must be done, without changes of general form of the conversion algorithm.

The developed simulation tools allow the assessment of predicted influence of a drift rate on the final performance of IC ADC with both the standard and extended algorithms. They also enable the estimation of the number of cycles needed to obtain the given resolution of the converter which would be able to work properly in the presence of drift.

References

[1] Ed. W. Kester, *Analog-Digital Conversion*, Analog Devices Inc., 2004.

[2] M.E. Waltari, K.A.I Halonen, *Circuit Techniques for Low-Voltage and High-Speed A/D Converters*, Kluwer Academic Publishers, 2002.

[3] A.A. Platonov, K. Jędrzejewski, J. Jasnos, "Design and Analysis of Algorithmic Multi-pass A/D Converters with Theoretically Highest Resolution and Rate of Conversion", *Measurement*, vol. 35, No. 3, pp. 277-287, 2004.

[4] A.A. Platonov, K. Jędrzejewski, Ł.M. Małkiewicz, J. Jasnos, "Principles of Optimisation, Modelling and Testing of Intelligent Cyclic A/D Converters," *Measurement*, vol. 39, No. 3, pp. 213-231, 2006.

[5] A.A. Platonov, J. Jasnos, K. Jędrzejewski, Ł. Małkiewicz, Z. Jaworski, E. Piwowarska, P. Studziński, "Particularities of Cyclic Intelligent ADC Design, Implementation and Adjusting", *Proceedings of International Conference on Signals and Electronic Systems ICSES 2008,* Cracow, Poland, pp. 43-46, 2008.

[6] A.A. Platonov, "Optimal Identification of Regression-type Processes under Adaptively Controlled Observations," *IEEE Transactions on Signal Processing*, vol. 42, No. 9, pp. 2280-2291, 1994.

[7] A.A. Platonov, J. Szabatin, K. Jędrzejewski, "Optimal Synthesis of Smart Measurement Systems with Adaptive Correction of Drifts and Setting Errors of The Sensor's Working Point", *IEEE Transactions on Instrumentation and Measurement*, vol. 47, No. 3, pp. 659-665, 1998.

[8] J. Jasnos, "Analysis and Application of Modified Sub-Optimal Algorithms to ICADC Design," *14th IMEKO Proceedings of International Symposium on New Technologies in Measurement and Instrumentation and 10th Workshop on ADC Modeling and Testing*, Gdynia-Jurata, Poland, pp. 564-567, 2005.

[9] Ł.M. Małkiewicz, A.A. Platonov, "Methods of Additional Improvement of Intelligent CADC Performance," *Proceedings of IEEE Instrumentation and Measurement Technology Conference, IMTC'2007,* Warsaw, Poland, CD-ROM, 2007.

[10] *IEEE Std 1241-2000*, "IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters," IEEE Inc., 2001.