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Methods with a new approach for measure static characterization of High Resolution DAC converters

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Abstract- This paper presents two new methods for measuring the static characteristic of high resolution Digital to Analog Converters (DACs). Both proposed methods are based on the conversion of the DAC output voltage to time by using a fast comparator and a reference calibrator. The main advantage of this approach is that time can be measured in the electronic domain much more accurately than amplitude. Both methods are based on direct time measurement by a high frequency counter and on the registration of the input DAC code. From the obtained information a Personal Computer (PC) evaluates the Integral Non Linearity (INL) and the Differential Non Linearity (DNL). Another advantage of the proposed methods is the relatively low requirements on all laboratory equipment involved.

I. Introduction

DAC converters are core elements of precise signal synthesizers. Today electronic devices based on digital signal processing integrates more and more features each demanding higher requirements for further increases of the volume of processed data, speed but also accuracy and quality. Such a significant increase in performance and accuracy of today's electronic devices also require the use of highly accurate, fast and linear DAC converters. The implementation of high quality DAC converters can be achieved by using suitable DAC architectures with their associated properties and technology used in production.

An important question arises for testing and measuring static and dynamic characteristics of such high quality converters when it is necessary, because their accuracy and speed has been higher than ADC converters. In literature, many suggestions have been proposed for measuring DACs characteristics ([1], [2] [3], - [9]), but most of them have been analyzed only from a theoretical point of view in simulations and their experimental implementation is often difficult. This paper proposes a method based on the conversion of the output voltage DAC tested level into a time interval. The time interval is measurable with higher precision than dynamic output voltage. Further the proposed method will be assessed with methods published in the papers [9], [10], - [13]) and ways how to improve their properties.

A. The proposed method to measure the precision of DAC converters

The principle of the proposed methods is based on the digital generation of a sawtooth signal, which serves as the input reference to the DAC converter. The time instant when the DAC output signal achieves the chosen quantization level on its output carries information about DAC nonlinearity. The time interval between successive generations of the same DAC output level is measured by a traditional method with known and adjustable accuracy. In this case DAC testing is performed under dynamic conditions, close to real using of the device. Time interval will be estimated with high precision by using fast voltage comparators, precision DC voltage sources and further auxiliary circuits.

The time interval must be measured with very high accuracy. For DACs with the resolution of 14-bit or 16-bit the time measurements allowing the discrimination of a voltage step of 1 LSB require the use of very fast electronic components and appropriate signal processing. Extending the measured time interval will significantly increase the proportion of the total number of pulses to the pulse representing the actual error, which for longer measurement cycles allow the detection of such small errors. Both proposed methods have been simulated in LabView environment and have not been yet fully implemented experimentally.

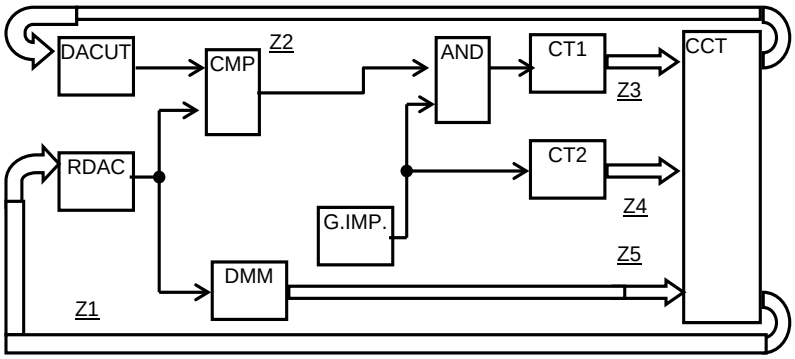

Figure 1. Block scheme of proposed method highlighting small difference in time

B. Method of precise time difference measurement

The proposed test method (Fig 1) includes the digital converter under test (DACUT) whose output is connected to a voltage comparator (CMP). The other comparator input voltage is connected to the reference digital analog converter (RDAC) output whose value is measured with high accuracy by a digital multimeter. The output value of the reference DAC is controlled by the control computer and its accurate measurement is registered by the same computer. During the measurement cycle the control computer tester (CCT) generates periodically a digital sawtooth with chosen slope S applied to the DACUT. The time interval generated at the comparator (COM) output is proportional to the integral non-linearity of the DACUT. The width of this time interval is measured by counting the number of pulses in counter M1 (CT1) which the gate (AND) released from the pulse generator (G,IMP,). Counter (CT2) is used to measure the total number of pulses M in one measurement cycle, which suppresses the effects of frequency instability of the pulse generator. The sawtooth waveforms generated at the output of the DAC under test represents a measurement cycle. Let's consider the tested output level U_1, which in the ideal case will be achieved with the digital input code k. The number of sawtooth periods during one measurement cycle is $M_{B.}$ The number of pulses generated during one sawtooth period from G.IMP is M_A . The ratio of tested voltage U_1 to the maximal value U_{MAX} is proportional to the ratio of the corresponding code bins k and $k_{MAX.}$ For the the ideal DAC the ratio is

$$\frac{U_1}{U_{MAX}} = \frac{k*Q}{k_{MAX}*Q} = \frac{k*M_A}{k_{MAX}*M_A} \tag{1}$$

The integral nonlinearity of DACUT at the output voltage $U_1$is given by

$$INL(k) = \frac{U_{REAL}(k) - U_1(k)}{U_{MAX}} = \frac{M_1}{M} - \frac{k*M_B*M_A}{M_A*M_B} \tag{2}$$

Taking into account that $M_A.M_B=M$ the final expression for $INL(k,S)$ is

$$INL(k) = \frac{M_1 - k*M}{M} \tag{3}$$

Here the slope S of the sawtooth signal is

$$S = \frac{k_{MAX}*Q}{M_A*T_{G.IMP}} \tag{4}$$

At the end of each cycle, the measurement control computer tester (CCT) register the measured DC voltage U_1 from digital voltmeter (DMM), the output M_1 from counter (CT1) and output M from the counter (CT2). The main advantage of testing the dynamic errors of digital analog converters is the fact that the uncertainty of the measurement time interval is suppressed by compensation of data M_1, M. The resulting accuracy is determined only the accuracy of the DC digital voltmeter (DMM). Precision digital DC multimeters

with bus compatible with any interface (CCT) are one of the most affordable devices with the required accuracy at most electronic workplaces. Moreover, variation of the slope S offers possibility to test integral nonlinearity in the dynamic mode.

The quantization error in the time interval measurement can be enhanced by enlarging the number of counts *M* for longer measurement cycle. The measurement cycle has to be repeated for any code bin. This is the main drawback of the proposed method. The long testing time can be shortening by using DAC models and estimation of the INL values in the crucial points of the DAC FSR.

C. Simulation of proposed method

Before experimental implementation the method was verified through software simulations. The input signal is being represented by a digital sawtooth generator, which represents the ideal output of the DAC converter which can be artificially added to a known failure. Fig 2 shows simulation of this method for a DAC with a resolution of 9-bit and with forced errors in its transfer characteristic. Finally, their evaluation as *DNL* and *INL* parameters from the simulated data has been performed. Simulation results of a DAC with known *DNL* show, that testing error are larger when the modelled DAC is corrupted by noise. Inherent *DNL* of the simulated DAC is hidden in the noise.

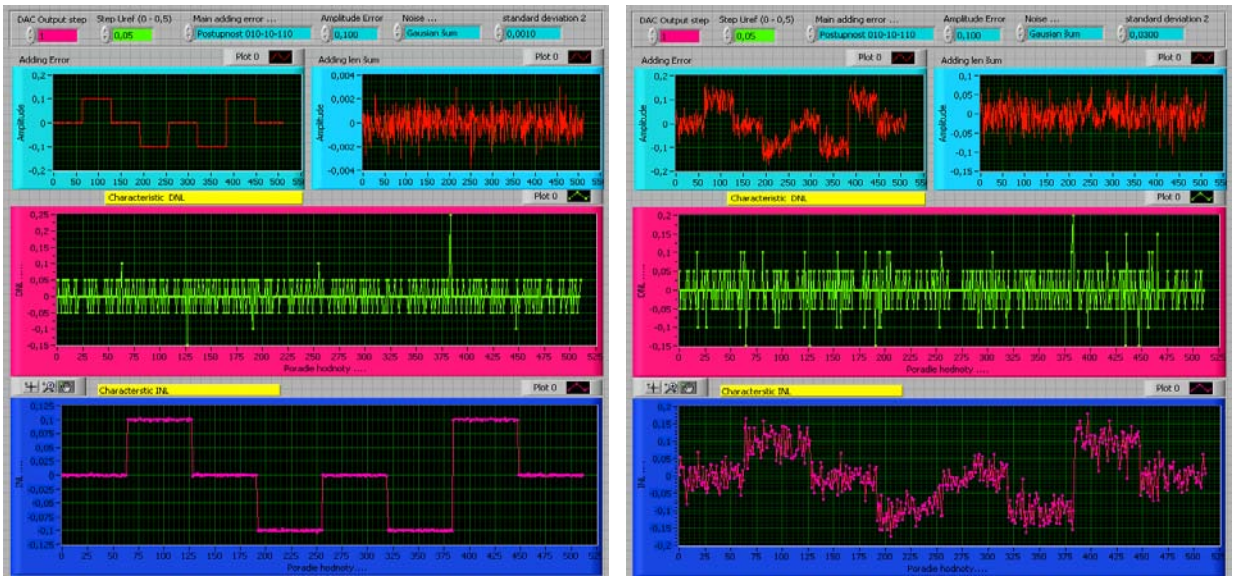

Figure 2. Simulation of precise time difference measurement for a 9-bit resolution DAC without noise (on left-hand side) and with noise (on right-hand side) in development environment

The proposed method under ideal condition works properly. The weakness of the proposed method is that the voltage steps of the reference input voltage have to be lower than quantization level of DACUT. The voltage reference step size, relative to 1LSB determines the accuracy of the measurement required characteristics for INL and DNL. Enlarge the number of counts M for longer measurement cycle highlights quantization error in the time interval measurement. Another very important fact in implementing the measurement procedure is also the very short time (t_X << 1ns), which will require a very fast electronic components and equipment and suppression of various interference. Another drawback is the insensitivity of measuring stand on the reference voltage changes inside of quantisation level of the DAC UT.

D. Method of generation and measurement of pulses

As mentioned above in part A. the principle of this method is based on conversion amplitude to time using fast comparator and adding dithering voltage, which increase accuracy of the measurement errors below 1 LSB. The output of the comparator is not directly represented as a time which will be subsequently measured, but the output of the comparator will be used for setting the conditions for entry code value of the input buffer memory. Since in this way are processed very short times related to small voltage of quantization level fast DAC converters with a resolution of 12, 14 and 16-bit it is necessary to synchronize the entire measurement system and also to remove possible error sources in the testing stand and look for ways how to improve precision.
This method has the advantage by using the speed memory, whose contents is loaded into a PC where it will run

processing of data and in that case we do not need any fast counters or quick scopes.

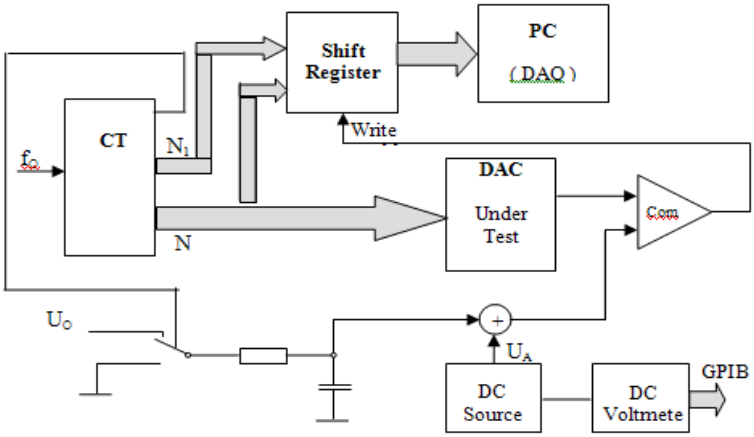

Figure 3. Block diagram of the method of generation and measurement pulse

The comparator's response time is greater than the measured time difference. The acquired time is being corrected by subtraction of a constant delay. The same delay error for all input values is assumed here. In average the number of pulses from G.IMP is $N_1=M_A/2^N$.

The output of the counter is connected to input of the test converter and the buffering memory FIFO. Dithering voltage allows to measure INL inside quantization level of DAC UT. Dithering signal avoids repetition of quantization error in the digital interval measurement caused by the possible synchronism of starting instant of measurement with sawtooth generation too. Triangular dithering voltage with peak value U_0 has been added to the DC voltage U_A. Average voltage at the DC multimeter is being measured with the same accuracy. Added DC voltage shall be adjusted as the decision-making level for the test quantization level. Set voltage U_A is also measured by precision digital multimeter and its value transmit to computer. The output of the comparator will be used to set the conditions for entry code value of the input buffer memory. Buffering memory will be used for storing values of code words related condition is met, that the test voltage output DAC converter is greater than the sum of the DC voltage and dithering voltage. Block diagram of the proposed method, which was described above can be seen in Figure 3.

Dithering voltage is added to enhance the resolving power of the method to distinguish an error less than LSB, the amplitude should be equal $U_{DITH\ MAX}$ = 1LSB and the period will be binary times period saw.

Comparison of the input voltage of comparator we control writing the codes word into buffer memory to get sequence for a certain quantization level. On Fig 4. can see waveforms for particular signal and sequence obtained from describe method.

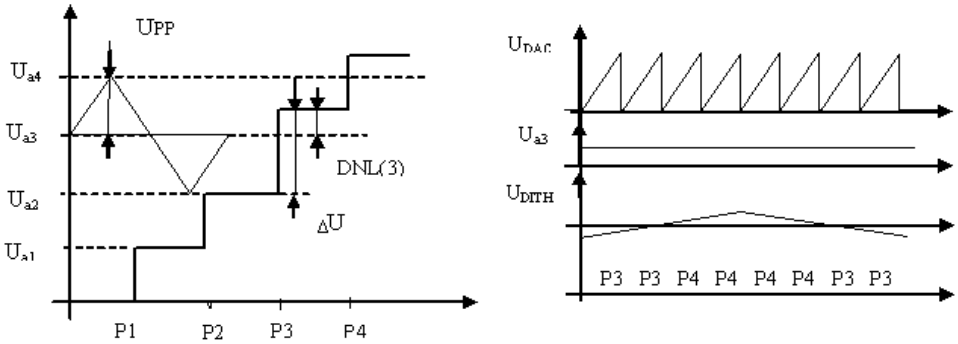

Figure 4. Output from tested DAC converter with no ideal voltage level Ua3 on left-hand side and particular signal with obtained sequence

Record for individual quantization level is loading of buffer memory into the PC where is post processing. To increase the accuracy of measurement will be achieved by the repeatedly measurements for one value and successive averaging. The principle of proposed method has been verified by the simulation. The simulation shows applicability of proposed method for testing of INL, DNL of high resolution DAC below LSB under dynamic conditions. The dynamics of the testing signal is determined by the best implementable parameter in all dynamic models which is slope of the input signal.

II.Conclusion

This paper describes two methods of measuring non-linearity DAC converters, based on conversion of voltage to time and then measures it, which is precisely thereby avoiding measurement of amplitude. Measurement allows achieve the sufficient accuracy for precision DAC with high resolution, often higher than 12, 14 or 16 bit. Both methods have a weak point in the comparator's own delay, that it's higher than the error that we try to detect, but there we assume that the comparator steal the same error in all measurements, and it can be corrected.
The first mentioned method is relatively simple and output voltage from DAC under test is appropriate way transferred to the number of pulses using simple and readily available component. Measurement of very short time require use very fast component, but on the other side with average linearity. Quantization error in the time interval measurement is being enhanced by the enlarging the number of counts M for longer measurement cycle. The only issue to be solved is its inability to determine INL for voltages U1 in one quantization interval. The dithering voltage proposed in the second version avoids this drawback.

The second method is more complex and by addition of dithering voltage allows more accurate measurement of small errors. Dithering voltage added to DC voltage suppress the systematic error in the digital interval measurement caused by the synchronism of stating instant. The main drawback of the proposed method is fact, that the measurement cycle has to be repeated for any code bin. The long testing time can be shortening using DAC model and estimation of the INL values in the crucial points of the DAC FSR.

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