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A sine generation and coherent sampling system with high time accuracy

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***Abstract*-**In this paper, a system is presented, which accurately synthesizes and coherently samples sinusoidal signals. The system, based on an atomic clock which disciplines both a signal generator and a data acquisition board, has been used to analyze the code excitation statistics of a coherently sampled sinewave, as a function of the selected sinewave parameters, including overdrive and initial phase. Experimental verifications have been carried out, aimed at investigating the problem of designing efficient stimuli for ADC testing purposes.

I. Introduction

ADC and DAC testing is a very important topic, due to the wide diffusion of digital signal processing. To this aim, various testing techniques have been developed and standardized [1]-[3]. A related problem is the selection of the proper stimulus, which, in order to guarantee a proper characterization of the converter under test, should ensure the excitation of each of the converter codes [4][5]. To this aim, some sufficient conditions have been derived in the literature for uniform converters, which guarantee the excitation of each converter code when the stimulus is coherently sampled. Such conditions may be used to select the minimum sample length of a stimulus, as a function of the converter resolution [4]. Further conditions have be derived to compensate any unwanted stimulus frequency deviation, by properly increasing the minimum sample length of the selected stimulus [4]-[7].

In previous activities, the authors have proposed a procedure for selecting the stimulus frequency and minimum record length, also analyzing the effects of Additive White Gaussian Noise (AWGN) on the converter code excitation [7]. In particular, a design algorithm has been developed using Farey Series theory [8][9], and implemented as an Open Source C++ program [10]. While the design algorithm relies on number theory to select the test parameters, its performance may be improved by comparing its results against experimental evidence, which would allow the identification of any phenomena affecting the test design effectiveness. To this aim, accurate control of the experimental environment is needed. In particular, the ratio between stimulus frequency and sampling frequency is a critical parameter, and a high stability of both stimulus and sampling frequencies is required [4]-[7]. In this paper, an accurate experimental system is described, which can generate and coherently sample sinusoidal signals, with very high frequency resolution and accuracy. The results may be used to refine the pre-existing test design algorithms [1]-[7]. Moreover, the selection of the stimulus initial phase and offset is considered, showing that unwanted drifts of this parameter may significantly affect the code excitation statistics. Such results seemingly imply that the various test design procedures, including the ones described in the standards, may be improved by keeping into account the stimulus initial phase and offset.

II. The developed system

The proposed system, whose architecture is shown in Fig. 1, consists of a HP3325 B programmable waveform generator, and a National Instruments NI-5105-PCI Data Acquisition System (DAS), installed on a Windows XP Personal Computer (PC). The DAS features a 12 bit ADC, capable of operating at a maximum sampling rate of 60 Msample/s, with programmable trigger slope/level, input range, and 16 MByte of internal RAM. A Stanford Research PRS-10 Rubidium atomic clock is also present, with a stability of $5 \cdot 10^{-12}$ (Allan Variance, 1 hour), providing a very stable 10 MHz reference signal. By using the atomic clock signal as a reference for both the function generator and the NI DAS, sampling coherency is guaranteed with very high accuracy. The overall system is entirely controlled by the PC, through a C++ program developed by the authors. In particular, the atomic clock is initially configured via an RS232 interface, the stimulus parameters are properly set by programming the function generator through GPIB bus, and the DAS is directly controlled by interacting with the NI dynamically linked library (DLL). In particular, the record length, the sampling frequency, the DAS input

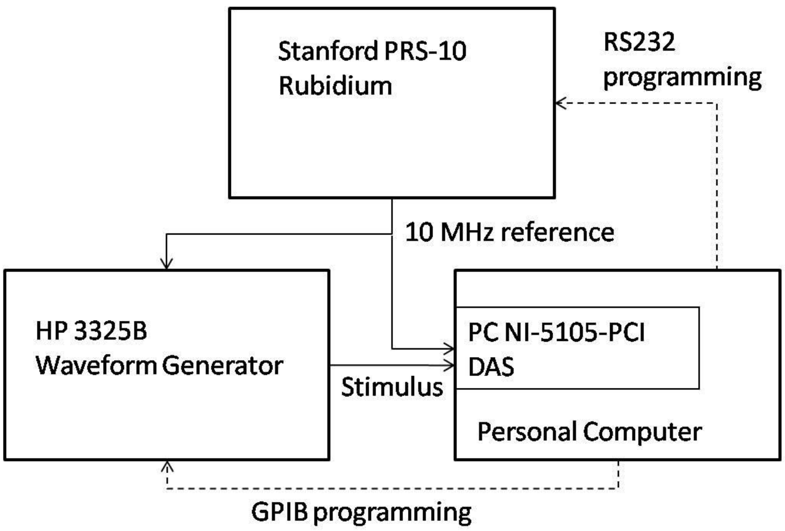

Figure 1: Experimental setup.

range, and trigger level/slope can be automatically set. Notice that the trigger setting may be used to control the initial phase of the acquired record.

III. Simulation and experimental results

Testing procedure

The experimental setup has been tested under various conditions. It is worthy of notice that, according to manufacturer's choice, the DAS selectable ranges do not completely excite the ADC dynamic range, leaving some external unused codes. To keep into account this feature, two approaches have been followed. As a first step, the sinewave generator amplitude has been gradually increased, checking out the acquired signal dynamic, (i.e. the maximum and minimum values of the ADC output codes), and identifying the ADC true Full Scale Range, gain, and offset. In particular, for a nominal range of 0.5 V, the conversion range [-0.5659 V, 0.5581V] was obtained, corresponding to an actual Full Scale Range of 0.5612 V coupled to an offset of approximately -0.0037 V. After applying a sinewave with amplitude 0.57 V, compensating the offset, and using a 3 parameter sinefit, a gain *G* of 0.985 was estimated. Furthermore, in order to operate in a simplified scenario, a reduction of the ADC resolution has been introduced, by normalizing the 12 bit ADC collected integer codes to 2^4. In this way, the 12 bit ADC reduces to a 8 bit converter, whose larger decision intervals consent to excite the largest 8 bit codes even if the applied sinewave amplitude is slightly lower than the ADC Full Scale.

Following the identification of the ADC range and offset, code excitation can be investigated as a function of the stimulus initial phase, controlled by changing the trigger level/slope conditions. Such an approach does not consent to completely control the acquired sinewave initial phase, due to the unknown delay between the trigger event and the following sampling instant. Consequently, after the amplitude tuning procedure, three parameter sinefit can be applied, attempting to accurately estimate the actual sinewave initial phase. Notice that the sinefit results can be used to estimate also the overall noise power at the ADC output. Once the signal has been acquired and characterized, the test design algorithm can be used, and both Montecarlo simulations and measurements can be carried out, allowing performance comparison and validation.

Testing Results

Following the described approach, a series of measurements have been carried out, aimed at investigating the code excitation behaviour when the sinewave initial phase slightly differs from the null value. In particular, Fig. 2 shows the percentage of bad records, that is the percentage of records which fail to excite all of the equivalent 8 bit ADC levels, evaluated on a set of 100 acquired records, as a function of the sinewave initial phase ϕ, normalized to π, which has been varied in the interval $[0, 0.1\pi]$. The results have been obtained by converting a sinewave of amplitude A=0.57 V and frequency f_0=496.9 Hz, sampled at a frequency f_C=200 ksample/s, by the equivalent 8 bit ADC with nominal range equal to 0.5 V, and the aforementioned estimated *FS* of 0.5612V and offset of -0.0037 V. Two curves are shown, one obtained by selecting a record length L=805 according to [4][5]

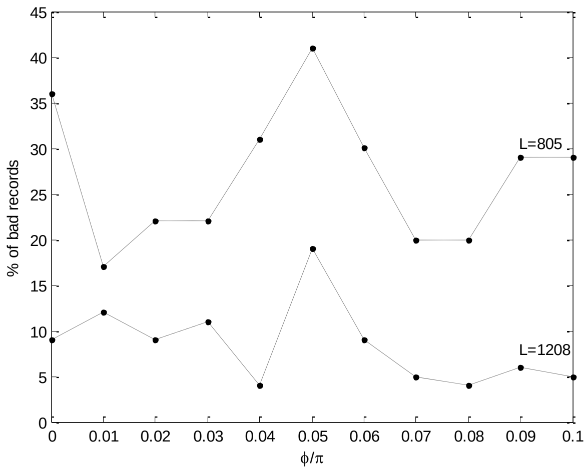

Figure 2: percentage of bad records, experimental results, ϕ∈[0, 0.1π].

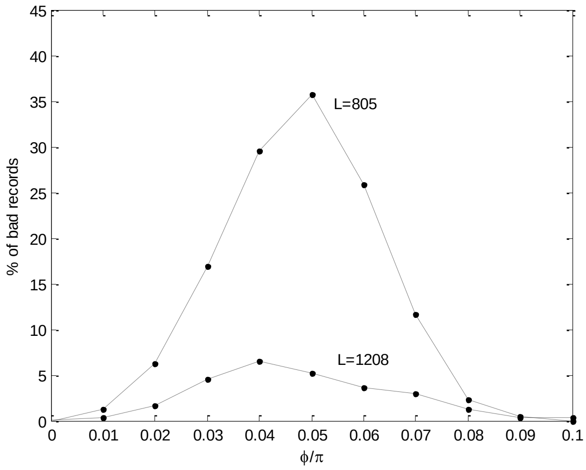

Figure 3: percentage of bad records, Montecarlo results, ϕ∈[0, 0.1π].

$$M = ceil(2\pi \cdot 2^b)\ , \quad (1)$$

where b is the converter bit resolution, one obtained by extending the record length to L=1208, selected as in [4]-[7]. Notice that the accuracy of the initial phase selection has been checked using three parameter sinefit on the acquired sinewave. The results seemingly suggest that the adopted procedure usually consents to control the acquired sinewave initial phase with a maximum deviation of about π/100. As expected, the percentage of bad records is reduced when the record length is increased, however it is not reduced to zero as suggested by [4]-[7]. Moreover, the percentage of bad records changes with the initial phase, and is maximized when ϕ=0.05π, for both values of record length L. Following such results, the amount of ADC output noise power exceeding the expected quantization noise power has been estimated using sinefit results, obtaining an additional noise standard deviation σ of $4.2\cdot10^{-4}$ V, and the various estimated parameters have been used to run Montecarlo simulations. The results, obtained by simulating the acquisition of 1000 records for each considered phase, are summarized in Fig. 3. It can be observed that the phase dependency is similar to that of Fig. 2, the percentage of bad records being maximized when ϕ=0.05π.

However, the Montecarlo analysis tends to lose accuracy when the phase is set to the extremes of the considered [0, 0.1π] interval. Furthermore, even in simulations, the bad record percentage is not reduced to zero when the record length is increased. Such differences may be due to several reasons. First of all, the test design algorithm [4]-[7] assumes that the initial phase ϕ equals 0, and that neither the ADC or the stimulus are affected by offset. Furthermore, the Montecarlo analysis assumes that the simulated ADC is not affected by INL, which may be

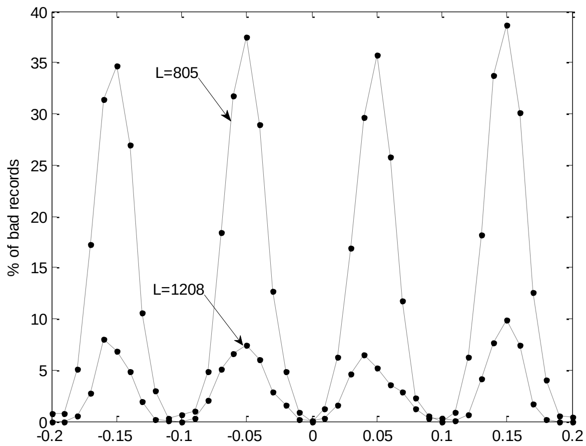

Figure 4: percentage of bad records, Montecarlo results, ϕ∈[-0.2π, 0.2π].

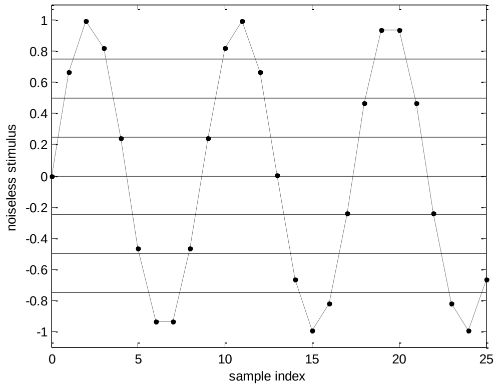

Figure 5a – Noiseless stimulus and ADC transition levels, d=0, ϕ=0.

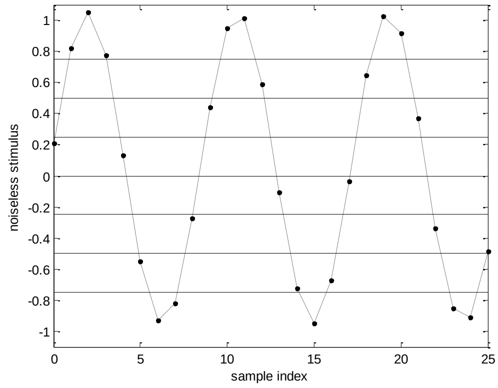

Figure 6a – Noiseless stimulus and ADC transition levels, d=0.2Δ, ϕ=0.05π

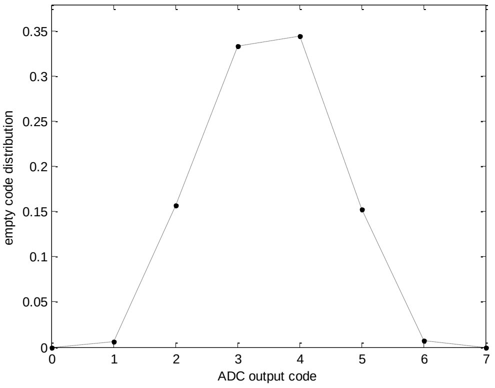

Figure 5b – Relative frequency of unexcited code occurrences, d=0, ϕ=0, σ=0.2Δ.

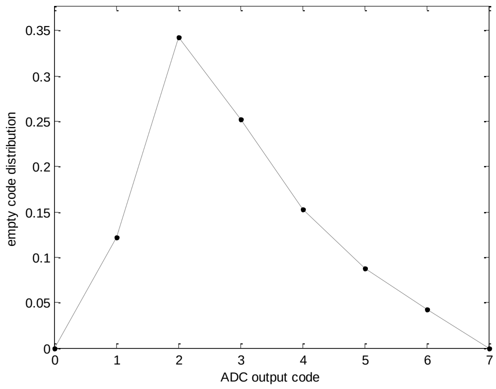

Figure 6b – Relative frequency of unexcited code occurrences, d=0.2Δ, ϕ=0.05π, σ=0.2Δ.

present in the real ADC. Finally, the sinewave initial phase of the experimental data is known with limited accuracy. In order to gain further insight, simulations have been repeated, this time considering the phase interval [-0.2π, 0.2π]. The obtained results, reported in Fig. 4, suggest that the percentage of bad records is seemingly periodic with the stimulus initial phase. Such a behaviour has been further investigated, and is discussed in the following section.

IV. Effects of initial phase and offset variations on converter code excitation

The observed behaviour has been further analysed and discussed, and may be explained by preliminarily observing that (1) determines the value of M, which is both the record length and the denominator of the ratio J/M between the sinewave frequency and the sampling frequency [4]. Eq. (1) is a sufficient condition, derived by upper bounding the width of the intervals between the phases associated to the stimulus samples [4], and by assuming that no input noise is superimposed to the acquired signal. The phase gaps are insensitive to any sinewave initial phase ϕ, as changing it simply rotates any phase by the same amount ϕ. However, as the phase associated to each sample changes with ϕ, the distances of the corresponding samples from the converter transition levels depend not only on the sinewave offset d, but also on ϕ. In particular, in presence of additional noise at the converter input, samples close to an ADC transition level are likely to be shifted by input noise, falling into a bin different from the one to which the noiseless samples would actually belong. Consequently, changes in the initial phase may actually affect the probability that a record fails to excite each of the converter codes. To further investigate the problem, a simplified scenario has been considered, in which a 3 bit uniform midriser converter is excited by a sinewave with amplitude A, equal to the ADC Full Scale Range FS. Equation (1) provides M=26, and the ratio between the sinewave frequency and the sampling frequency has been chosen equal to the irreducible fraction J/M=3/26. The dotted curve of Figure 5a shows the collected stimulus when d=0 and ϕ=0, together with the ADC transition levels, plotted as solid horizontal lines. It can be observed that, under such condition, several samples are very close to the transition levels of the converter bin they fall into. It is worthy of notice that the aforementioned conditions are ideal, and that, provided that J/M remains an irreducible

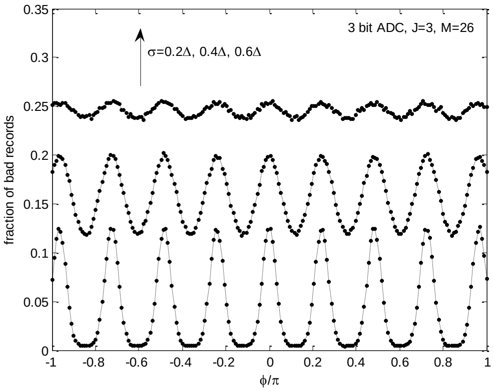

Fig. 7 – fraction of records failing to excite all of the ADC codes, for *d*=0 and various AWGN levels.

fraction, changing *J* would produce the same *M* samples, only collected in a different order. Under such condition, the effect of noise has been considered, by adding to the noiseless stimulus an AWGN with standard deviation σ=0.2Δ, where is the ADC quantizer step. The selected value of guarantees that a noisy sample may be shifted at most into an adjacent bin, with respect to the bin the ideal stimulus would excite, and corresponds to high SNR conditions at the ADC input. By running Montecarlo simulations, a fraction of about 13% (which reduces to 0.45% by choosing a record of 2*M* samples) of the collected records failed to excite all of the converter bins, and, as shown in Fig 5b, the most frequently unexcited ADC bins are the one that a noiseless samples would have filled with samples closer to the ADC transition levels. Following that, simulations have been repeated, changing both *d* and ϕ. For instance, Figs. 6a and 6b have been obtained this time by setting *d*=0.2Δ and ϕ=0.05π. By inspecting Fig. 6a, it can be inferred that the new noiseless stimulus is potentially more robust than the previous one, as the various samples are farther from the corresponding ADC transition levels. By repeating Montecarlo simulations with the same noise level, this time only 0.7% (which reduces to 0.006% by choosing a record of 2*M* samples) of the generated record failed to excite all of the converter codes. As expected, most of the non-excited bins are again the ones corresponding to samples in Fig. 6a closer to the ADC transition levels. The obtained results show that test design procedures may be improved, by using also sinewave offset and initial phase as an additional degree of freedom. Notice that the considered phenomenon may have significant effects only for high SNR. In fact, when SNR is lowered, the input noise may dominate quantization noise, acting as a dither [7]. Such a behaviour is confirmed by Fig. 7, which reports the fraction of bad records for *J*/*M*=3/26, and *d*=0, obtained as a function of ϕ for various levels of AWGN. It can be observed that also in this case the fraction of records failing to excite all of the ADC codes shows a seemingly periodic dependence on ϕ, even if the oscillation period differs from the one of Fig. 4, possibly due to different values assumed by *M* and Δ. As expected, the oscillations amplitude is reduced when σ is increased.

IV. Conclusions

An experimental setup for analysing the effects of coherent sampling has been developed and tested, which allows to control both sampling and stimulus frequencies with very high accuracy. The setup has been characterized and is currently being used to validate an ADC test parameter design algorithm, and to refine the related simulation model. In particular, the system has been used to test the effects of sinewave initial phase on the excitation of ADC's codes. Further research is in progress, aimed at characterizing with deeper accuracy the ADC characteristics, the effects of trigger jitter, and the application of sinewave overdrive. Both the Montecarlo analysis and the experimental results seemingly show that the currently known test design procedures may become inaccurate if the stimulus phase is not properly controlled, and that such parameter, together with sinewave offset, may be conveniently selected to improve the converter test efficiency.

Acknowledgement

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