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ADC Design in Organic Thin-Film Electronics Technology on Plastic Foil

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Abstract- In this work an architectural investigation is presented concerning the full integration of ADCs in thin-film organic electronics technology on a plastic foil. From a technological point of view and dealing with a limited number of building blocks available, i.e. often only p-type transistors are available and resistors are not, several ADC architectures are discussed and compared for their specifications and limits. From this discussion a few topologies are left over that are considered applicable up to a certain level. Finally a ΔΣ ADC design is presented in this work and the measurement results of this organic ΔΣ ADC integrated on foil are presented.

I. Introduction

While the industry is preparing the market entry of flexible and rollable full-color display devices the interest for more plastic applications such as RFID tags [1], flexible lighting, printed memory and large area sensor arrays[2] keeps growing. Next to these mostly digital circuits also analog sensor applications for smart sensor systems are of interest since organic semiconductors can be influenced by several environmental parameters, i.e. pressure, chemicals[3] and light. The smart sensor systems require analog circuits such as front-end amplifiers but also high precision analog-to-digital converters (ADC) as well as digital-to-analog converters (DAC) as an interface with their sensors and actuators. This need for high precision conflicts with the limited performance of organic electronics technologies nowadays, especially when compared to silicon technologies and therefore demand for an efficient implementation in the technology. Organic technologies suffer from low mobility (typically ~0.1-1cm^2/Vs), behavioral parameter variations (i.e.variation of the threshold voltage V_T) and from sensitivity to the ambient environment (light, O_2 and H_2O). Moreover the applied technology is unipolar and only provides p-type pentacene transistors. In this work after a brief presentation of the applied technology in section II we give a broad overview of several ADC topologies and their applicability in organic electronics technologies in section III. Section IV elaborates a ΔΣ ADC designed for implementation on foil. Finally also the measurement results of the fully integrated ΔΣ ADC in organic technology on a plastic foil are shown in section V.

II. Organic Electronics Technology

One of the promising organic materials that show a semiconductor behavior is an oligomer called pentacene that is being used now for more than a decade and is applied in all the most developed organic electronics technologies. Nevertheless these organic technologies suffer from an intrinsically low carrier mobility, caused by the grain boundaries in the semiconductor layer. However researchers are finding and implementing n-type organic transistors and combining them in complementary technology, the applied technology in this work is unipolar and only the p-type transistors are supplied. Moreover organic transistors are very sensitive to variations of transistor parameters such as the threshold voltage V_T. These variations come to the surface at process time or at run time, where they are caused by bias stress and interference with H_2O and O_2 in the ambient environment. The technology in this work is a bottom-gate thin-film transistor technology with 3 metal layers[4], as depicted in fig. 1. This enables the application of backgates that are considered as a second gate physically located on top of the bottom-gate transistor. These backgates have a linear influence[5] on the transistor's V_T and therefore result in improved transistor behavior. Furthermore the backgate serves as a passivation layer and reduces the sensitivity of the technology to the ambient environment. P-type transistors and metal-metal capacitors can easily be produced in the applied technology. A specific material for resistive components is not available, but transistors biased in the linear region can under certain conditions be applied as resistors.

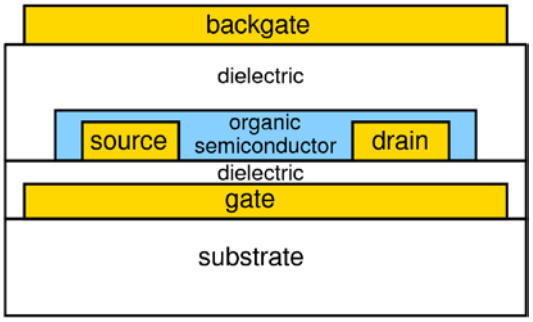

Figure 1: The layer structure of a transistor in the applied organic thin-film electronics technology.

III. ADC Architectures

The family of ADC architectures is subdivided in several subfamilies such as flash ADC, SAR ADC, integrating ADC. Flash ADCs are known to be the fastest whereas with the integrating ADC the highest accuracies are obtained. SAR and oversampling ADC both are a trade-off between speed and accuracy. This section focuses on their applicability in organic thin-film electronics technologies, more specifically in the unipolar technology described in section II.

A. Flash ADC

A common flash ADC, as depicted in fig. 2a consists of a resistive ladder that creates digital levels and a comparator to compare the input signal to these digital levels. The thermometer-code digital word is then in an encoder converted to a binary output . The applicability of this topology is low since it relies hardly on mismatch between a large set of identical resistors that are not provided in the technology. Replacing them with transistors also suffers from the mismatch that is present. Moreover a large set of high-gain comparators is required. These comparators suffer from offset due to mismatch and can therefore also not be reliably implemented in the technology. Several improved flash architectures exist that reduce the number of building blocks, i.e. subranging, pipelined, folding and interpolating ADCs. However they reduce the number of required building blocks and resistors, they do not fully solve the matching issue and all still suffer from the same issues.

B. Integrating ADC

The working principle of a dual-slope integrating ADC, presented in fig. 2b, is that first a fixed capacitor is charged with an input voltage. In the second phase the capacitor discharges at a fixed speed while a digital counter starts running. A comparator detects when the capacitor is discharged and directly stops the counter. The value of the counter is then the digital output of the ADC. Integrating ADCs have the advantage that they do not rely on matching between identical components. They reuse one capacitor and one comparator, and thus this ADC can easily be calibrated for an improved performance. Moreover the offset present in the comparator can even be eliminated in a slightly modified quad-slope architecture. The disadvantage of the dual-slope and quad-slope topologies is that it is known to be very slow compared to other architectures. Therefore in a technology with limited headroom in terms of speed (~1-10kHz) this architecture might not be the most preferred.

C. SAR ADC

An n-bit successive approximation ADC is presented in fig. 2c. It applies an n-bit DAC, a comparator and a digital unit. In the first clock cycle the input signal is compared to half of the input voltage window of the ADC, i.e. the value corresponding to the digital n-word “100…0”, and the most significant bit (MSB) is determined and stocked. In each of the following clock cycles the most significant bit that was not yet set is determined by comparing the input signal with half of the remaining voltage window. After n clock cycles the digital output is determined and the circuit is reset to its initial state. The DAC in SAR ADCs can be implemented with a bank of matched resistors, matched current sources or matched capacitors. The resistors and current sources in the applied technology score poorly for matching, but the metal-metal capacitors in the applied technology are known to be more reliable. Therefore a capacitive C-2C capacitor bank in a SAR ADC forms an interesting architecture for application in the described technology. Moreover, as the implementation is on a plastic foil, the

parasitic capacitance towards the substrate is practically non-existing hence no capacitive losses towards the substrate are experienced. However since the applied technology is unipolar the '0' and '1' values in an inverter never exactly equal the ground or the power supply voltage. Therefore the voltage swing that each capacitor undergoes is not clearly determined and suffers from variations which forms an upper limit to the accuracy of this topology. A 6b C-2C topology partially integrated in a complementary organic technology on glass is discussed in [6].

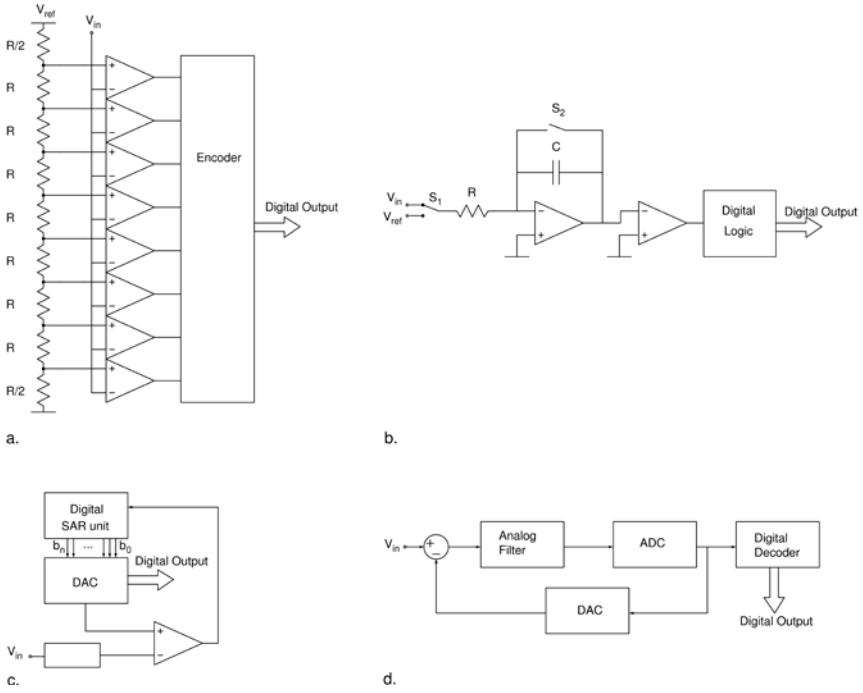

Figure 2: Schematic system level view of (a) a resistive flash ADC, (b) a dual-slope integrating ADC, (c) a successive approximation ADC, (d) an oversampling ΔΣ ADC

D. Oversampling ADC

A promising architecture that is even more insensitive to parameter mismatch in a bank of components is a ΔΣ ADC [7] since this topology does not apply a ladder of components that rely on matching. Instead it applies a feedback circuit that generates an error signal by subtracting the high frequent quantized output from the low frequent analog input. It is visualized in fig. 2d. An analog low-pass filter shapes the quantization noise at the output towards higher frequencies forcing a higher SNR within the signal band width. The filtered error signal is then digitized with a comparator that needs a certain minimal gain in order not to diminish the accuracy of the converter. Therefore the accuracy of a ΔΣ ADC topology is primarily determined by the filter order and the gain of the comparator of this ADC circuit. Moreover nowhere in the circuit information is thrown away and every error between input ant output is sent back in the loop. Therefore this architecture also repairs its own mistakes as long as the loop gain is high enough. ΔΣ ADCs tend to reach higher speeds than integrating ADCs but typically they remain slower than SAR architectures. Several techniques exist to improve the precision for the same oversampling ratio (OSR) such as using higher order filters and more-bit ΔΣ ADC where an n-bit ADC and DAC are applied internally instead of just a comparator. Moreover cascaded topologies exist that further improve the precision without increasing the OSR or becoming unstable.

IV. Design

The ΔΣ presented in this work is the first fully integrated organic ADC implemented on foil. The presented ADC, shown in fig. 3a, consists of an integrator, a comparator and a level shifter. The differential double-input integrator in fig. 3b is built around a 3-stage opamp with Miller capacitors for pole splitting and applies transistors biased in the linear region as resistors. Its function is to push the quantization noise towards high

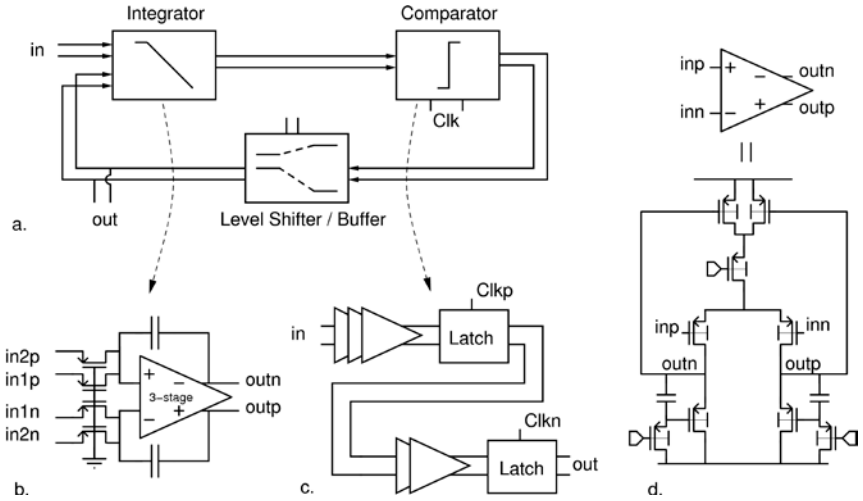

Figure 3: Schematic view of the implementation of (a) the first order ΔΣ ADC, (b) implementation of the integrator, (c) implementation of the comparator and (d) Implementation of the single-stage differential amplifier with CMFB, BGE, backgate steering and a cascade.

frequencies. The comparator in fig. 3c digitizes the signal. Both the opamp and the comparator are built using a single-stage differential amplifier, presented in fig. 3d, as a building block in which several analog techniques are applied for improving the performance such as bootstrapped gain enhancement (BGE), common-mode feedback and backgate steering. Successive amplifier stages are connected through high-pass filters in order to compensate for the offset in each stage.

V. Measurement Results

Fig. 4a shows the measured output spectrum of the ADC. The first order ΔΣ ADC achieves a measured SNR of 26.5dB for an OSR of 16 at a clock speed of 500Hz and a 10Hz input sine wave. This results in an input signal band width of 16Hz. The circuit consumes 100μA from a 15V power supply voltage. The noise floor in the signal band width of the spectrum is caused by the limited gain in the integrator and it forms an upper limit to the performance of this ADC. The chip photograph of the ADC is shown in the right panel of fig. 4b.

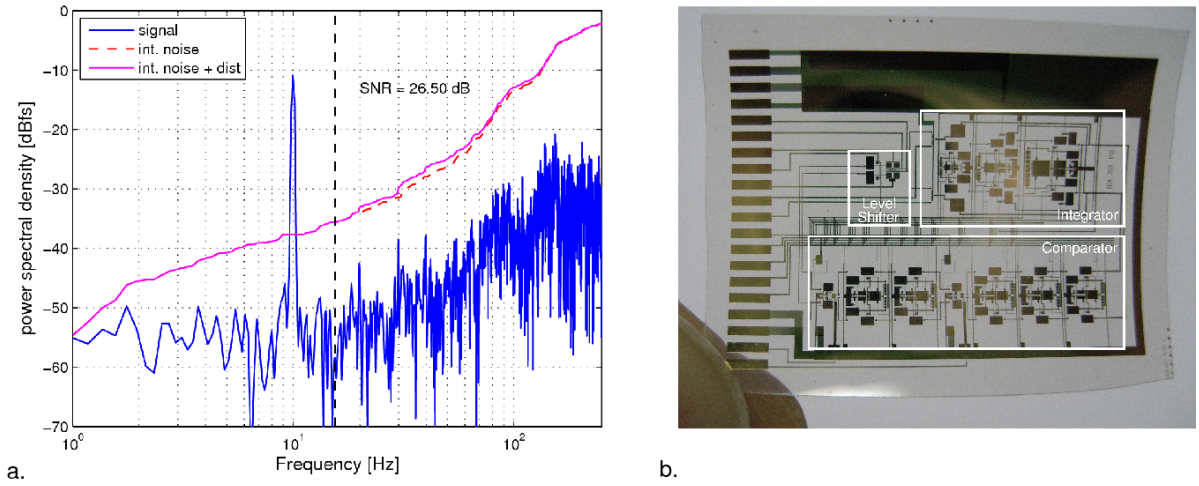

Figure 4: (a) The measured output spectrum of the presented ΔΣ ADC and (b) the plastic chip photograph of the presented ADC.

VI. Conclusion

In this work an overview is given of ADCs and a discussion about their applicability in thin-film organic technologies on foil. The typical characteristics of organic electronics technology are briefly presented in order to support the circuit considerations made in this work. Afterwards the applicability of flash, SAR, integrating and ΔΣ ADC architectures in organic electronics technologies are compared for accuracy. Finally a fully integrated ΔΣ ADC on foil performing with 26.5dB SNR is elaborated and measurement results are presented. Organic ADC circuits are applicable as an interface between sensors of any kind and the digital signal processing in smart sensor systems on foil, i.e. applied in body area networks.

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