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An Input Signal Statistics Aware Design Approach and Examples for Analog-to-Digital Converters for communication systems

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Abstract-Most of the analog-to-digital converters (ADCs) nowadays are designed for a specific application and embedded in a System-on-Chip (SoC) instead of a stand alone ADC chip for general purpose. In this case, the ADC input signal statistics is known information, while in different systems it can be far different from others. This observation gives opportunities to design ADCs smartly in a system context to achieve the required system performance at minimal complexity, area and power. In this paper, an input signal statistics aware design approach for ADCs for communication systems is discussed and two parallel ADCs architectures based on this approach are proposed for converting multi-carrier signal.

I. Introduction

The trend of achieving higher data throughput in communication systems and moving more functions from the analog domain to the digital domain for cost reduction and flexibility imposts more and more demanding specifications on ADCs in terms of bandwidth, conversion accuracy, area and power. While CMOS technology scaling helps in achieving higher bandwidth and smaller area thanks to shorter transistor channel length and component matching improvement, dynamic range and sampling linearity are got worse due to reduced supply voltages and available signal swing [1][3]. These two factors are strongly affecting the conversion accuracy which is also referred to the effective resolution of ADC. The choice of the ADC effective resolution for a certain system needs to take special care, since the complexity and power consumption of an ADC is nearly exponentially related to its conversion accuracy. Conventionally, ADCs are design in such way that the signal is “blindly” converted without any consideration of its statistical property. Since the signal statistical property is known in a specific system, there is opportunity to design ADC optimally for the needs of the system without over designing to reduce the ADC complexity and power consumption.

In section II, ADC conversion accuracy limitations, signal characterization for communication systems and a design approach based on using the priori statistical properties of the input signal to optimize the design of ADC are discussed. Then in section III, two parallel ADCs architectures are proposed based on this approach for converting multi-carrier signals, with detail discussion on their principle, advantages and analytical simulation. Finally, a conclusion is drawn in section IV.

II. Analysis

A. ADC conversion accuracy limitations

A good indication of the overall conversion accuracy of an ADC is the Signal-to-noise-and-distortion power ratio (SNDR) which can be expressed by:

$$SNDR = \frac{V_{signal.rms}^{2}}{n_{quantization} + n_{clipping} + n_{thermal} + n_{mismatch} + n_{nonlinearity} + n_{other}} \qquad (1)$$

Where the

$V_{signal.rms}^{2}$: input signal power of the ADC;

$n_{quantization}$: quantization noise caused by the rounding error between the analog input signal and the digitized output value;

$n_{clipping}$: clipping noise caused by the difference between the signal exceeding the input range of an ADC and the ADC's maximum range.

$n_{thermal}$: thermal noise which can be characterized by the total integrated noise $\gamma \cdot \frac{k_B T}{C}$, with k_B the Boltzmann constant, T temperature, C the total input sampling capacitance and γ the noise excess factor.

$n_{mismatch}$: noise caused by mismatch of components;

$n_{nonlinearity}$: nonlinearity distortion which is dominated by the input sampling stage and amplifying stages;

n_{other} : other noise due to clock jitter, supply noise and so on .

From equation (1), it is clearly shown that the SNDR of an ADC can be improved by either reducing the denominator of the equation or increasing the numerator. Reducing the denominator requires to minimize thermal noise, improve matching or linearity. This is a costly way in terms of ADC complexity, area and power consumption and has been discussed extensively in many publications [2][3][4][5]. Generally speaking, the power needed for an ADC increases exponentially with the increase of conversion accuracy through this method. For matching limited ADC (mainly low resolution ADCs), increasing the ADC conversion accuracy by one bit requires an 8 times increase in power and for thermal noise limited ADCs, it is around a 4 times increase in power. For an ADC that is already at the edge of the state-of-the-art, increasing one extra bit resolution may result in an infeasible implementation. The other way to improve the SNDR is by increasing the input signal power of the ADC. This looks straight forward but it is limited by the linearity of the sampling stage, output signal swing of amplifying stages and available signal swing decided by the technology in conventional ADC architectures.

B. ADC input signal characterization for communication systems

In digital communication systems, the information is conveyed by means of modulation, commonly used techniques are single-carrier modulation techniques and multi-carrier modulation techniques which several carriers are transmitted simultaneously. Fig. 1 shows a single-carrier signal (BPSK modulated) and a multi-carrier signal (each sub-carrier is QAM modulated) in time domain and their amplitude histograms which reflect the amplitude distribution of the signal. It is clearly shown that the statistical property of a multi-carrier signal is far different from that of a single-carrier signal. The single-carrier signal is sinusoidal alike and has a U-shaped distribution. While the multi-carrier signal is a summation of a large number of single-carrier signals with uncorrelated amplitudes and phases, the resulting signal amplitude distribution is approaching a Gaussian distribution according to the Central Limit Theorem. In time domain, the multi-carrier signal is observed to have large "peaks" when compared to its average power value. This undesirable property requires ADCs to have a higher dynamic range in order to cope with the requirement of having a small probability of clipping events required by the system. In multicarrier communication systems, too much gain in the receiving front-end will saturate the ADC and clip the signal, while insufficient gain will result in higher quantization, thermal and mismatching induced noise with respect to signal power. Conventionally, a compromise was found by backing off the input signal power by a large factor from the ADC full scale power level (e.g. 10dB power back-off for clipping probability less than 10^{-3}) in order to achieve an optimal SNR[6]. For signals with large crest factor, this approach leads to very inefficient usage of the ADC's dynamic range and power.

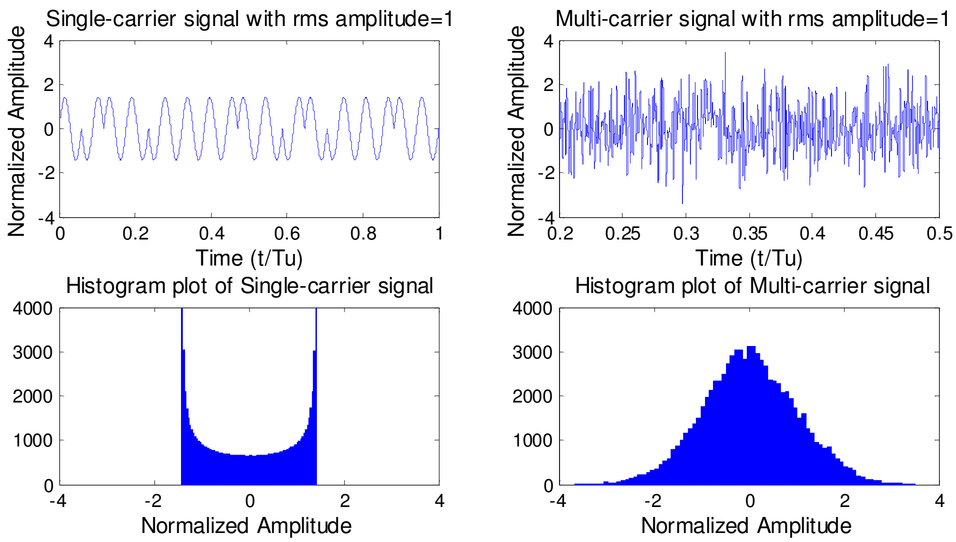

Figure 1. Multi-carrier signal versus single carrier signal in time domain and their amplitude histogram

C. An Input Signal Statistics Aware Design Approach

If the signal statistics is considered, Eq. (1) can be rewritten to

$$SNDR = \frac{V_{signal.rms}{}^{2}}{\sum_{k=1}^{2^N} \int_{x_{k-1}}^{x_k} (x-y_k)^2 f(x)dx + 2\cdot \int_{L_{clipping}}^{\infty} (x-L_{clipping})^2 f(x)dx + n_{thermal} + n_{mismatch} + n_{nonlinearity} + n_{other}} \quad (2)$$

Where $f(x)$ is probability density function of the signal, x_k the quantization levels and y_k the output levels of the ADC, N is number of bit and $L_{clipping}$ is the ADC clipping level.

Previous studies show that it is possible to design an optimal quantizer for a given signal statistics [7][8]. By spacing quantization levels closely where the signal amplitudes are more likely to occur than where they are not, the total quantization noise can be minimized. This can help to increase the SNDR by reducing the first term in the denominator of eq. (2). Another approach in literature is companding [9][10][11] which the input signal is compressed according to its probability density function $f(x)$ and passed it to an uniform ADC, and then the ADC output signal is expanded in the digital domain. This is equivalent to using a non-uniform ADC and can also achieve optimum quantization theoretically. On top of that, the compressed ADC input signal may have a higher signal power than that of an optimal quantizer that having the same input range which is a benefit for a higher signal to thermal noise ratio.

Since IC technology offers poor absolute values but good relative values or matching, an ADC with non-uniform quantization levels is difficult to implement accurately. And for high resolution ADCs, the SNDR is normally limited by thermal noise instead of quantization noise. Thus, it is preferred to use an ADC with uniform quantization step size. While for companding, implementing a compressor to compress input signal according to its probability density function ideally in analog domain can be very complicate and accurately expanding a nonlinear compressed signal can be unstable and may generate additional distortion. So a good way lies in taking into account implementation difficulties, and combines the advantages of the above mentioned approaches.

III. Parallel ADCs architectures

A. Principle and advantages of the parallel ADCs architectures

Two parallel ADCs architectures using uniform ADCs and linear compressor are proposed based on this approach for signal with Gaussian amplitude distribution. In Fig. 2a the first proposed parallel ADCs architecture is shown, in this architecture the input signal is split into a main signal and an auxiliary signal which is an attenuated version of the input signal. These two signals are sampled at the same time. Depending on the input signal level, one of them will be chosen to reconstruct the signal in the digital domain. Fig. 2b shows the other proposed parallel ADC architecture, in this architecture the input signal is split into a main signal and two auxiliary signals which are offsetted and scaled versions of the input signal. They are sampled at the same time. Depending on the input signal level, one of them will be chosen to reconstruct the signal in the digital domain. The criterion is such that the signal in the main path is maximized to exploit the dynamic range of the ADC efficiently and have more resolution over the main part of the signal range, while the auxiliary signal path provides coarsely quantized samples to replace the samples of the main signal that are clipped by the ADC, hence avoiding excessive clipping noise in the main signal.

The sampled main signal has a better signal to quantization noise ratio (SQNR) and signal to thermal noise ratio (STNR) while the sampled auxiliary signal has a better signal to clipping noise ratio (SCNR) and signal to distortion ratio (SDR). When the signal is reconstructed properly in the digital domain, the digitized signal has a better SNDR compared to the one with the conventional method. Therefore, a required system performance can by achieved by using multiple of uniform ADCs with lower effective resolution instead of a single higher effective resolution ADC which is much more power efficient, since generally power consumption of ADCs increases exponentially with conversion accuracy. Another advantage is that since ADC input signal power is boosted compared to the conventional one ADC architecture, it allows a higher amount of thermal noise for a given signal to thermal noise ratio (STNR) which reduces the kT/C noise limitation in determining the capacitor size, hence a smaller layout area can be achieved.

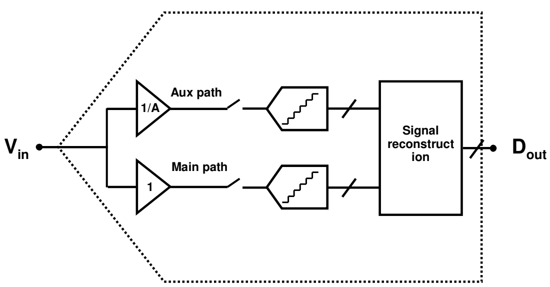

Figure 2a. Block diagram of parallel ADCs architecture I

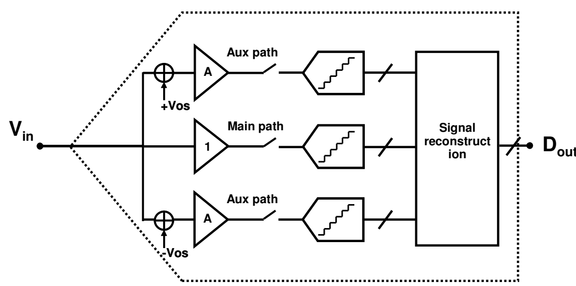

Figure 2b. Block diagram of parallel ADCs architecture II

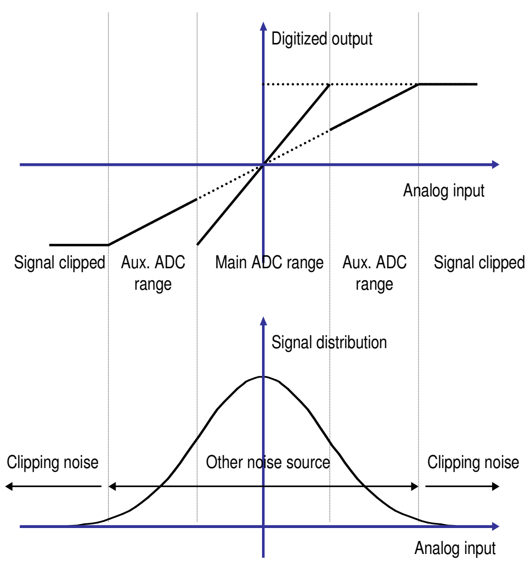

Figure 3a. Mapping ADC input range with multi-carrier signal amplitude distribution (architecture I)

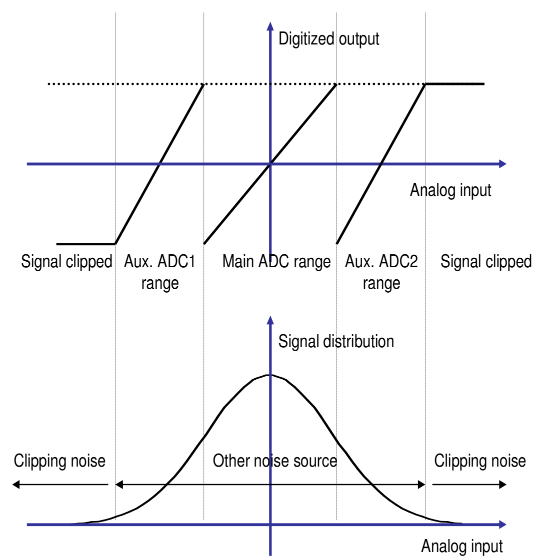

Figure 3b. Mapping ADC input range with multi-carrier signal amplitude distribution (architecture II)

B. Analytical simulations of the parallel ADCs architectures

For simplicity, in this analytical analysis the ADC non-linearity is not included, so the SNDR becomes signal-to-total-noise ratio (SNR) and can be expressed as following:

$$SNR_{conventional\_ADC} = \frac{V_{signal.conventional.rms}{}^2}{F(-L_{clipping}, L_{clipping}) \cdot (n_{quant} + n_{other}) + 2 \cdot F(-L_{clipping}) \cdot n_{clipping}} \quad (3)$$

$$SNR_{proposed\_ADC} = \frac{V_{signal.proposed.rms}{}^2}{F(-L_{clipping1}, L_{clipping1}) \cdot (n_{quant1} + n_{other1}) + 2 \cdot F(-L_{clipping2}, L_{clipping1}) \cdot (n_{quant2} + n_{other2}) + 2 \cdot F(-L_{clipping2}) \cdot n_{clipping}} \quad (4)$$

Where $V_{signal.conventional.rms}{}^2$ and $V_{signal.proposed.rms}{}^2$ are the RMS input signal power of ADC, $F(x)$ is the distribution function of the input signal, $L_{clipping}$ is the ADC clipping level , n_{quant} and $n_{clipping}$ are the quantization and clipping noise power respectively, n_{other} is used to model other input referred noise power.

For signals with known statistical properties, optimal SNR for ADCs can be found from Eq. (3) and (4). In order to make the analysis clearly, an input signal with Gaussian amplitude distribution and a thermal noise floor according to the ADC resolution are applied in these equations. In Fig. 4a, the SNR of the proposed architecture I with two 10b ADCs and the SNR of a single 10b and 11b ADCs are plotted with respect to signal loading level (defined by signal rms amplitude over ADC clipping level). The SNR of the proposed architecture II with one 10b and two 9b ADCs and the SNR of a single 10b and 11b ADC are also shown in Fig. 4b. By properly setting the scaling factor (A) of the auxiliary signal path, the peak SNR of the parallel ADC architectures can be substantially improved compared to conventional one ADC approach with the same resolution and achieve similar peak SNR compared to ADC with one bit higher resolution. This observation is also valid for ADCs with arbitrary number of bits.

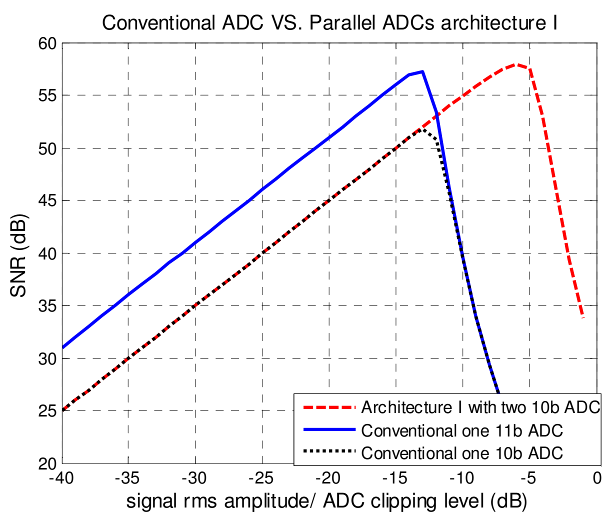

Figure 4a. Architecture I, SNR versus signal loading level (input signal with Gaussian amplitude distribution)

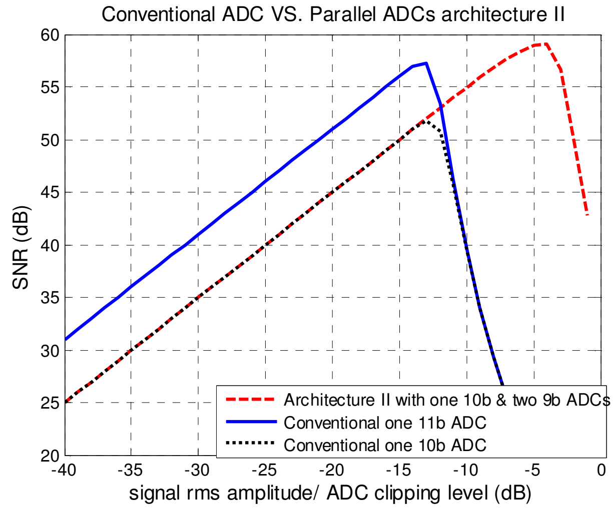

Figure 4b. Architecture II, SNR versus signal loading level (input signal with Gaussian amplitude distribution)

IV. Conclusions

In this paper, an input signal statistics aware design approach for ADCs for communication systems is discussed. It shows that ADCs can be designed wisely to reduce the power consumption and implementation complexity to achieve a required system performance by exploiting the statistical properties of the signal. Two parallel ADCs architectures are proposed for mulit-carrier signal based on this approach. Analysis and simulations show that the peak SNR of the parallel ADC architectures can be substantially improved compared to conventional one ADC approach with the same resolution and achieve similar peak SNR compared to ADC with one bit higher resolution.

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