The Design and Initial Testing of the Beam Position Measurement System in SSRF Based on Fully Digital Signal Processing

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Abstract- This fully digital beam position measurement system is designed both for beam position monitoring and machine research in Shanghai Synchrotron Radiation Facility (SSRF). The signals received from four position-sensitive detectors (PSD) are narrow pulses with a repetition rate up to 499.654 MHz and a pulse width of around 100 ps, the dynamic range of which could vary over more than 40 dB in machine research. By the employment of the under-sampling technique based on high-speed high-resolution A/D conversion, all the processing procedure is performed fully by the digital signal processing (DSP) algorithms integrated in one single FPGA. A previous incomplete prototype of this system had been designed with simple tests conducted. After debugging and modification, the second version system is designed, and a more systematic test is conducted, which will be presented in details. The initial testing results indicate that this system has achieved a position resolution (at the turn by turn rate of 694 kHz) better than 7 um over the input amplitude range of -40 dBm to 10 dBm.

Index Terms- beam position measurement, under-sampling, high-speed high-resolution A/D conversion, fully digital signal processing, SSRF

I. INTRODUCTION

Shanghai Synchrotron Radiation Facility is one of the third-generation synchrotron radiation light sources in the world, the kernel of which is an electron accelerator [1]; up to 720 electron bunches in the beam circulate in the storage ring to produce synchrotron light [2]. The amplitudes of the beam signals from the PSDs change with the beam position; therefore by calculating the amplitudes of the 4 channel signals, the beam position can be obtained according to the Δ/Σ normalization principle [3].
The output signals from the PSDs are periodic narrow pulses, the width of which is around 100 ps, as shown in Fig. 1. The repetition frequency of the pulses is 499.654 MHz, rendering its frequency spectrum as shown in Fig. 2. This repetition frequency corresponds to the machine clock frequency (e.g. Turn-By-Turn rate) of 693.964 kHz (marked as f_{mc}) multiplied by the bunch number of 720 (499.654 MHz = 693.964 kHz $\times$ 720).

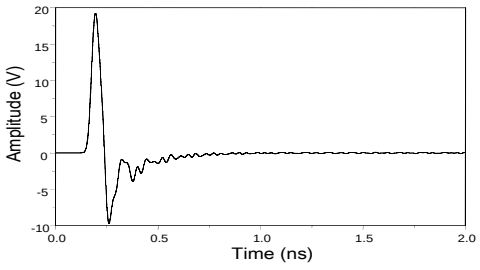


Fig. 1 Waveform of the signal from the PSD

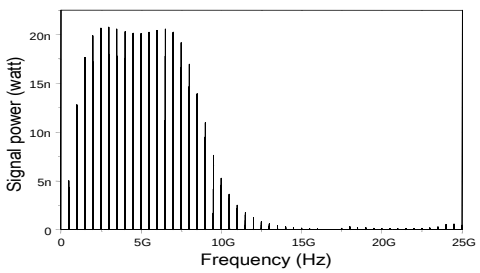


Fig.2 Frequency spectrum of the signal from the PSD

As shown in Fig. 2, the signal energy is only located on the frequency of 499.654 MHz and its integral multiples. So the amplitude of the narrow pulse can be obtained from the signal amplitude on 499.654 MHz, because they are proportional to each other.
As for the beam position measurement in SSRF, the beam position resolution is required to be better than 10 um at the Turn-By-Turn (TBT) rate [4]. We had worked on a previous incomplete prototype of the beam position measurement system, with simple tested conducted. [5] After debugging and modification based on the previous version, the second version system is designed, the kernel techniques and system architecture of which will be

presented as below in details. Meanwhile, a much more systematic test is conducted; the initial test results will also be introduced.

II. SYSTEM ARCHITECTURE

The traditional method for beam position measurement is based on analog manipulation, in which the signals are analog down-converted to Intermediate Frequency (IF) signals and then are manipulated directly to obtain the beam position information, all in analog domain [6]. Another method is to employ the IF sampling and digital data processing technique to achieve a better resolution [7]. As for the method based on analog signal manipulation technique, the beam position resolution will be inevitably deteriorated by the noise and mismatches of analog channels.

As for this system, the under-sampling technique based on high-speed high-resolution A/D conversion and digital signal processing are combined together to construct a fully digital processing system. As shown in Fig. 3, the narrow pulses from the PSDs are converted to sinusoid signals through Band Pass Filters (BPF), and then amplified to fit the dynamic range of the ADCs through the Automatic Gain Control (AGC) circuits. Then the 499.654 MHz sine wave signals are A/D converted by 4 high-speed high-resolution ADCs with the under-sampling technique; all the signal processing is implemented in one single FPGA. The calculated results are sent to the Single Board Computer (SBC) and further to the remote computer through the Ethernet Interface.

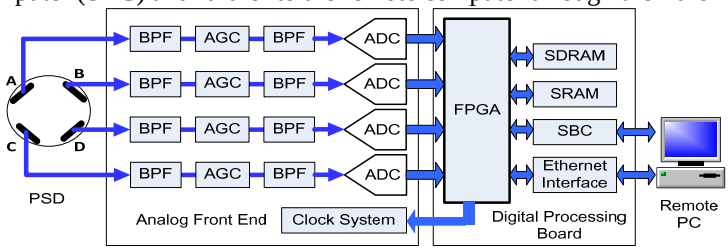


Fig. 3 Block diagram of this digital beam position measurement system

III. ANALOG FRONT END

A. Design of the AGC and BPF circuits

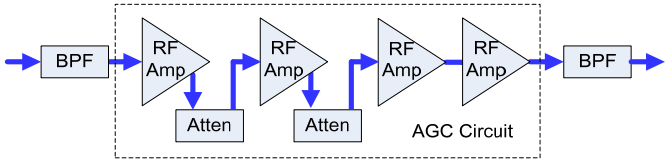


Fig. 4 Block diagram of the AGC and BPF circuits of one channel

When used in machine research, the output signals from the PSDs would change over a range of tens of dB. To obtain a high accuracy during A/D conversion, the signal should be amplified to a suitable amplitude before input to the ADC. As shown in Fig. 4, Radio Frequency (RF) amplifiers and RF attenuators are cascaded together to obtain a total gain from -3 dB to 59 dB. The RF attenuators are controlled by digital signals from the FPGA, which contains the AGC algorithm in it.

Surface Acoustic Wave (SAW) filters (TA0506A) are used for band pass filtering. The first BPF is used to filter the narrow pulses to sinusoid signals, while the second one functions mainly as an anti-aliasing filter. This two cascaded BPFs achieve a total out-of-band rejection of 100 dB.

The position arrangement of the two BPFs and the separation of the AGC power supplies for 4 channels have brought up an enhancement of around 20 dB on the suppression of harmonics and other spurious frequency components, compared to the previous prototype.

B. Design of the coupling circuits for ADCs

The coupling circuits for ADCs (LTC2208-14, 14 bit resolution with the sampling rate up to 130 Msps and the analog Full Power Bandwidth up to 700 MHz) are shown in Fig. 5, which are used to convert the single-ended signals to differential pairs to meet the ADC input requirement, as well as to implement impedance termination. A two-balun (balance-unbalance) type transformer configuration is used, which provides additional isolation and reduce the unbalanced capacitive feedthrough of a single transformer [8]. The balun transformer acts like a

transmission line, which has greater bandwidth, lower loss and better frequency response than the standard flux type transformer [9], the type of which was used in the previous prototype.

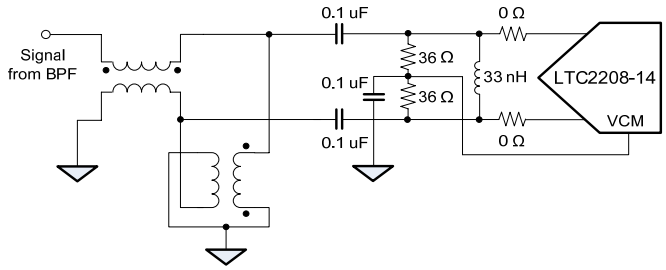


Fig. 5 Block diagram of the ADC coupling circuits

C. Design of the clock system for ADCs

The 499.654 MHz (f_{mc}×720) signals from the BPF are converted to digital IF signals with the under sampling technique. With a careful choice of the sampling frequency (f_s=f_{mc}×169, around 117.2799 MHz), the IF signal frequency is set to be f_{mc}×(720-169×4) = f_{mc}×44 (around 30.5344 MHz) according to the Nyquist-Shannon sampling theorem, which is just in the middle of the f_s/2 to avoid being interfered by noise at the brims of the Nyquist Zone.

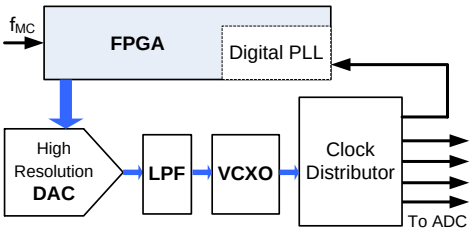


Fig. 6 Block diagram of the first clock system

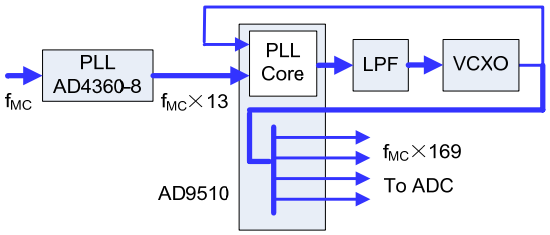


Fig. 7 Block diagram of the second clock system

As for high-speed high-resolution A/D conversion, the performance of the sampling clock is paramount [10]. Two clock systems are implemented and tested for comparison. The first one is based on the incoherent sampling technique. As shown in Fig. 6, the output signal frequency from the high quality VCXO is controlled by a high-resolution DAC, which can be tuned among the range of (f_{mc}×169) ± 6 kHz.

As shown in Fig. 7, the other clock system is based on the coherent sampling technique; the PLL AD4360-8 is used to generate the signal with the frequency of f_{mc}×13, which is further sent to the second PLL AD9510 to generate the clock signals (f_{mc}×169).

These two clock systems are tested, with the results compared. As mentioned above, the input signals are narrow pulses with the repetition frequency of 499.654 MHz. Moreover, these narrow pulses are further modulated by a macro pulse from the accelerator, with a repetition frequency of f_{mc} and a duty ratio of 500: 220. Test results indicate that the amplitude waveform fluctuates for the first clock system, and stabilizes for the second. This is probably due to the variation of the average number of RF signals per TBT cycle for the incoherent sampling technique. Thus the second clock system is selected in the final system design. Furthermore, the coherent clock system scheme could also be implemented by the employment of a digital PLL in the FPGA, as shown in Fig. 6, which will be studied in future.

IV. DIGITAL PROCESSING BOARD

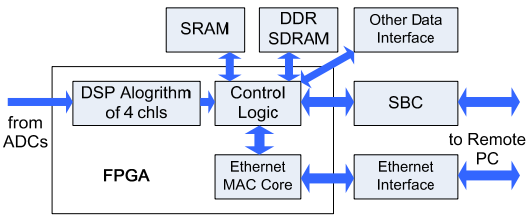


Fig. 8 Block diagram of the Digital Processing Board

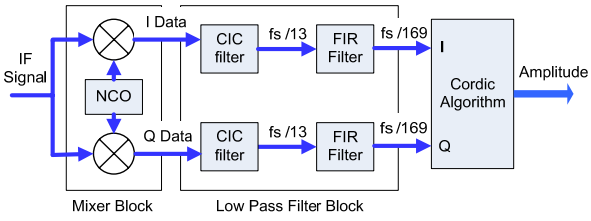


Fig. 9 Block diagram of the kernel DSP algorithms for one channel

The digital IF signals are sent to the Digital Processing Board (DPB), the block diagram of which is shown in

Fig. 8. All DSP algorithms are implemented in one single FPGA. The calculated results are sent to the remote computer directly from the FPGA through the Ethernet interface (debugging mode) or through the SBC.
The kernel of the DSP algorithm includes the Digital Down Convertor (DDC) [11] composed of the Mixer Block and the Low Pass Filter (LPF) Block, as well as the Cordic algorithm for amplitude calculation, as shown in Fig. 9.
The mixer block includes a Numerically Controlled Oscillator (NCO) and two multipliers. The NCO generates two In-phase and Quadrature-phase signals (I and Q) at the ADC sampling rate, which are used as the local oscillator signals for the two multipliers. The output of the mixer are expressed as

$$I = \frac{1}{2}A\left\{\cos\left[2\pi(f_{IF} - f_{NCO})nT_s + \varphi - \theta\right] - \cos\left[2\pi(f_{IF} + f_{NCO})nT_s + \varphi + \theta\right]\right\}$$
$$Q = \frac{1}{2}A\left\{\sin\left[2\pi(f_{IF} - f_{NCO})nT_s + \varphi - \theta\right] + \sin\left[2\pi(f_{IF} + f_{NCO})nT_s + \varphi + \theta\right]\right\} \quad (1)$$

（Note: f_{NCO} is the frequency of the signals generated by the NCO; f_{IF} is the frequency of the digital IF signals）

After the digital LPF, only the difference frequency components (f_{IF} - f_{NCO}) of the I and Q data remain; then the amplitude can be calculated as in

$$Amplitude = \sqrt{I^2 + Q^2} \quad (2)$$

The NCO is implemented with Xilinx IP DDS Core, the structure of which is shown in Fig. 10. The output signals from the NCO are of 16 bit width, while the phase word is of 29 bit width (corresponds to 0.22 Hz frequency resolution with 117.2799 MHz sampling rate), thus the accumulated phase word must be truncated to fit the 16 bit width of the Lookup Table (LUT) address. This error introduced by the truncation creates undesired spurious frequency components; to suppress this, an additive randomizing signal (dither sequence) is added to the phase word [12], which brings up an increase on the SFDR of around 12 dB [13].

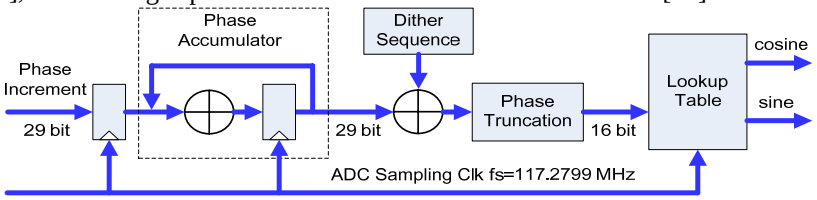


Fig. 10 Block diagram of the NCO with dither technique

The Low Pass Filter (LPF) Block is used to decrease the sampling rate from the ADC sampling rate to the TBT frequency, meanwhile filtering out the sum frequency and other aliasing components in I and Q data. To achieve both high operation speed and filtering performance, a Cascaded Integrator-Comb (CIC) filter and a Finite Impulse Response (FIR) filter are cascaded to obtain a down-sampling ratio of 169.
The CIC filter [14] is remarkable for its simplicity, which consists of only adders, subtractors and delay elements. The input signal first goes through an integrator section with 6 stages, then decimated by 13, and finally processed by a comb stage also with 6 stages. In the magnitude response of this CIC filter, the maximum side lobe is lower than -79 dB. As for the FIR filter, it is a 489 order equal-ripple filter [15] implemented with Semi-Parallel FIR Filter structure. Its normalized passband frequency is 0.07 with the manitude ripper of 0.1 dB, while the normalized stopband frequency is 0.084 with the stopband suppression of around 80 dB.
The FIR filter outputs the orthogonal I and Q data at the sampling rate of fs/169 (e.g. f_{mc}). The Cordic alogrithm (using Xilinx IP Cordic 3.0 [16]) is implemented to calculate the amplitude of each channel, the kernel of which is to convert the vector (I, Q) in Cartesian coordinates to vector (Amplitude, Phase) in Polar coordinates.

V. RESUTLS OF INITIAL TESTING

Fig. 11 shows the system under test. The signal source Rohde & Schwarz SMA 100A is used to generate a sine wave signal of 499.654 MHz, the amplitude of which is tuned by an external attenuator, and then it is distributed to 4 channels by a power splitter. The output of another signal source Tektronix AFG3251 is used as the macro pulse to generate the modulated signals. These modulated 499.654 MHz RF signals are then manipulated in the Analog Front End (AFE) and A/D converted to digital IF signals, which are further processed in the DPB. A remote PC communicates through the Ethernet with the DBP, which is responsible for the data readout and further analysis, as well as results display.

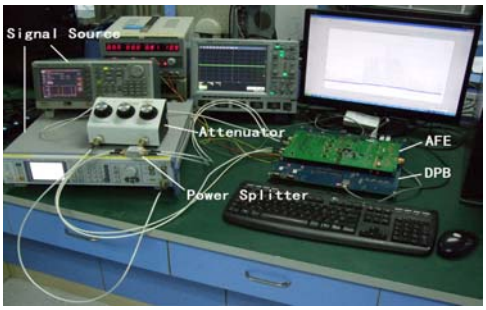
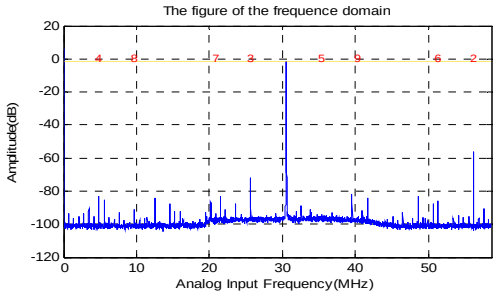


Fig. 11 System under test

A. ADC test results

In this test mode, 499.654 MHz sinusoid signals without modulation are input to this system. The output data of 16 section, each section with 16384 sampling points is analyzed through Fast Fourier Transform Analysis method according to the IEEE Std. 1241-2000 [17, 18]. The typical frequency spectrum of the ADC output signal is shown in Fig. 12 (input signal is -5 dBm). Fig. 13 shows the Effective Number of Bit (ENOB) of the ADC with different input signal amplitudes.



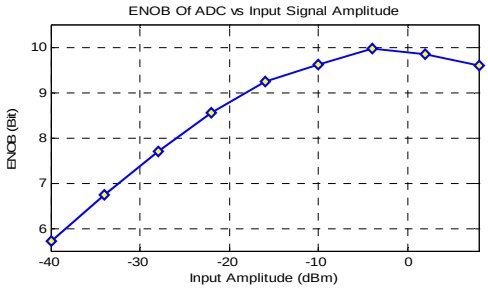
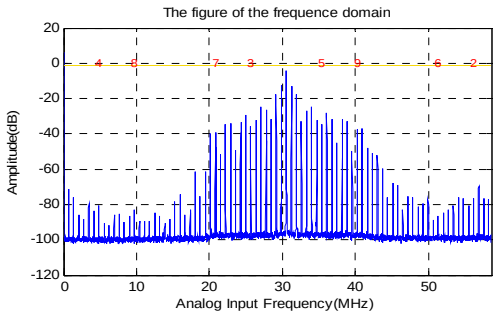


Fig. 12 Typical frequency spectrum of the ADC output signal
Fig. 13 ENOB with different input signal amplitudes

B. Initial Test Results of Position Measurement



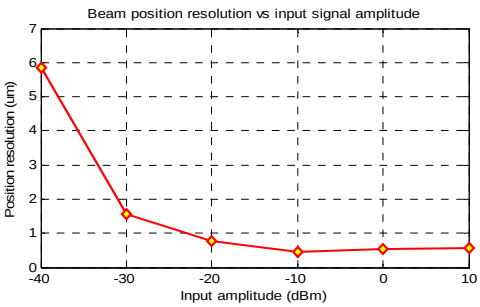


Fig. 14 Frequency spectrum of the ADC output signal with modulated input signal
Fig. 15 Beam position resolution with different input signal amplitudes

As mentioned above, the actual signals from the PSDs of the accelerator are modulated signals. To estimate the beam position resolution, modulated signals of 4 channels are generated as input signals. The typical frequency spectrum of the ADC output signal is now changed, as shown in Fig. 14. Fig. 15 shows the position resolution result, which indicates that this system has a position resolution better than 7 um over the dynamic range of -40 dBm to 10 dBm (at the TBT rate of 694 kHz).

C. Results of the Initial Commissioning Test with the SSRF Accelerator

After compeleting the system test in the laboratory, the commissioning test with the SSRF accelerator is conducted. The test results indicate that the beam position resolutions of X and Y direction are 3.76 um and 1.51 um respectively, which are better than requirement. The deterioration of the beam position on Y direction is probably due to the beam signal vibration.

As for the data transfer, the intial test results indicate that a total transfer speed up to 62 Mbps is achieved, which is better than requirement. The detailed information about this will not be included here.

VI. CONCLUSION

The structure and basic techniques of the beam position measurement system for SSRF were introduced and studied. By the use of fully digital architecture, a good system simplicity and reliability is achieved. Different electronics circuits have been designed and tested for comparison and selection. This fully digital beam position measurement system has achieved a position resolution better than 7 um over the input signal amplitude range of -40 dBm to 10 dBm; meanwhile all signal processing is implemented by DSP algorithms within one single FPGA.

ACKNOWLEDGMENT

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