Dynamic DAC Testing by Registering the Input Code when the DAC output matches a Reference Signal

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***Abstract*-** The accuracy of Digital to Analog Converters (DACs) is becoming important proportionally to the requirement on low distortion of the generated signals. This paper presents a new method for measuring the transfer characteristics of high resolution DACs under dynamic condition. The proposed method is based on the comparison of the DAC analog output voltage with a reference signal by using a fast comparator and registration of the DAC digital input code word in the moment when the DAC analog output voltage exceeds the reference voltage. The registration of the digital input code word into a fast memory is controlled by the comparator output. The reference signal is the superposition of the DC voltage generated by the DAC and a slow dithering voltage. Its average value is measured by a precision voltmeter which secures the required metrological accuracy. After digital processing the registered sequence of digital code words is used to determine the Integral-nonlinearity (INL) and the Differential-nonlinearity (DNL) of the DAC under test..

I. Introduction

DAC converters are core elements of precise synthesizers. The use of such DACs requires a simple and reliable testing procedure realizable in the laboratories equipped with general purpose instruments. Many DAC procedures have been proposed by different authors [1] - [13]. Some of them have been assessed both by simulation and experimental implementation. The implementation of the proposed methods is limited by the hardware restrictions. Some of them require spectral analyzers with accuracy higher than the nonlinearities of the DAC under test.

The authors proposed in a previous paper [13] a dynamic DAC testing procedure based on the conversion of the DAC output level into a time interval. The advantage in comparison to the previous proposals and standardized methods was the transfer of precision requirements from the waveform recorders to the time interval measurement. The time interval is measurable with higher precision than the dynamic output voltage. The drawback of this method was that besides the comparator accuracy the time jitter of the clock frequency corrupted the final accuracy. In order to avoid errors caused by using counters for measurement of short time intervals the presented method is proposed. It avoids counters by direct registration of code levels in a fast memory.

The principle of the proposed method is based on the comparison of the dynamic output voltage of the DAC under test with the reference DC voltage by using a comparator. The moment when the DAC analog output voltage exceeds the reference level serves for registration of the corresponding digital input code. The output of the comparator is used as the control signal to register the digital input code word of the DAC under test in a fast memory. This approach allows assigning to the DAC input digital code the precise (real) value of the DAC output voltage which is utilized as the reference voltage. In order to avoid quantization uncertainty the triangular dithering voltage with known peak-peak value is superimposed to the reference voltage. The quantization error is avoided by the digital averaging of registered codes during the testing interval which corresponds to the integer number of dithering signal periods. The output value from a precise DC voltmeter during one testing interval determines the reference voltage with the required accuracy. The impact of the dithering voltage is suppressed due to the averaging effect during an integer number of dithering periods. The metrological traceability of the proposed method is being protected by the precision of the voltmeter. In such a case the requirement on the precision of determination of the DC voltage is granted by using a precision voltmeter and no special instruments like reference DC source, signal analyzers with accuracy higher than DAC UT are required. The main advantages of the proposed method are the insensitivity to frequency jitter the method does not requires the use of an ultra fast converter and the possibility to suppress comparator's error by numerical correction taking into

account that the delay remains constant. DAC UT works under dynamically changing input codes with constant slope.

II. The proposed method for DAC testing

The principle of the proposed method is based on the comparison of the dynamic output voltage of the DAC under test with the reference DC voltage by using a comparator. The analog output voltage of the DAC under test (DAC UT) corresponds to the conversion to the analog domain of an input digital sawtooth sequence (Fig.1). When the DAC analog output voltage exceeds the reference level the digital input code is stored. The output of the comparator is the control signal to register the digital input code word of the DAC under test in a fast memory. This approach allows assigning to the DAC input digital code the precise (real) value of the DAC output voltage which is utilized as the reference voltage. In order to avoid quantization uncertainty the triangular dithering voltage with known peak-peak value is superimposed to the reference voltage ($U_{SUM} = U_{DC}+U_{DITH}$). The required amplitude of dithering is achieved by using an appropriate resistive divider. The impact of real dithering amplitude is being suppressed by digital post processing. The distortion of triangular dithering voltage can involve uncertainty. The amplitude reduction by the passive divider decreases the existing distortion of the generated dithering voltage at the output of the dithering DAC.

Moreover the amplitude reduction allows the use the dithering DAC with a lower resolution than the resolution of the DAC under test. The resolution of dithering DAC corresponds to the required digital resolution in the determination of integral nonlinearities.

The quantization error is avoided by the digital averaging of registered codes during testing interval which corresponds to the integer number of dithering signal periods. The output value from the precise DC voltmeter during one testing interval determines reference voltage with required accuracy. The impact of dithering voltage is suppressed because of averaging effect during integer number of dithering periods. The metrological traceability of the proposed method is being protected by the precision of utilized voltmeter.

The offset error and time delay of the comparator are being reduced by the digital post processing. INL error at the beginning and at the end of DAC UT full scale range should be according the terminal definition equal to zero. Achieved difference between measured level and theoretical one is being used for correction the whole output DAC range. The only consideration is that time delay is constant or is changing linearly along full scale range. The main problem related with comparator is oscillation around the comparation level. The small hysteresis suppressed partially this problem. Another possibility is the implementation of nonlinear digital filtering of registered data.

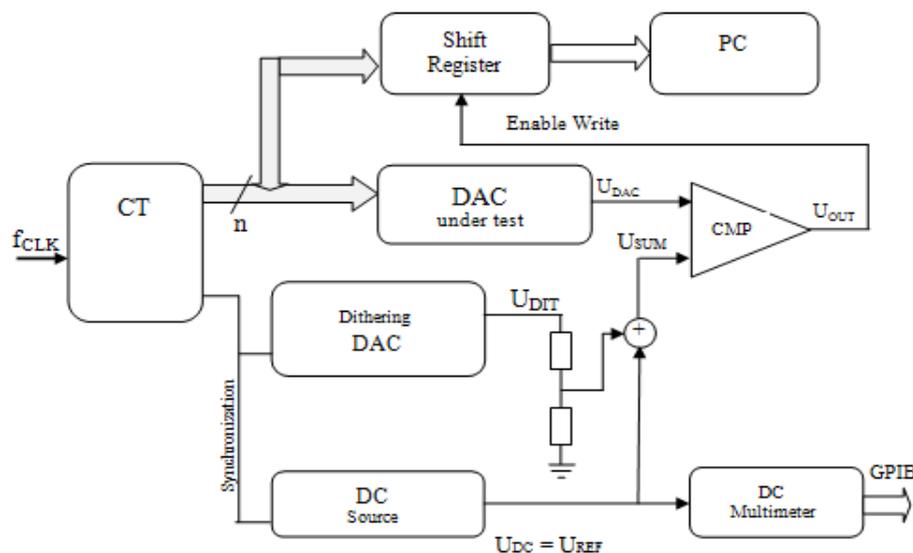A block diagram of the measurement system is shown in Fig. 1.

Figure 1. Block diagram of the proposed measurement system.

One measuring cycle contains L periods of the sawtooth voltage generated by the DAC under test and M periods of the dithering voltage, as shown in Fig. 2. The peak to peak value of the dithering voltage W corresponds to a few LSBs of the DAC under test. The DC voltage measured by the precise DC voltmeter during this measuring cycle averages the reference voltage and determines only the precise value of the voltage from DC source.
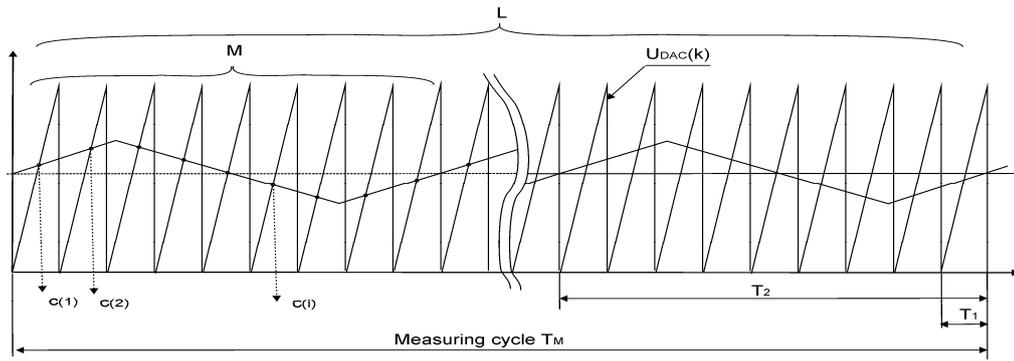
Figure 2. Analog output voltage $U_{DAC}(k)$, from the DAC under test and reference voltage U_{REF} as superposition of the dithering voltage U_{DITH} on DC voltage Ua.

Therefore, the measurement cycle is defined as $T_M = L.T_1 = MT_2$ where T_1 is the period of digital sawtooth at the input of the DAC UT and T_2 is the period of the dithering voltage. The sawtooth voltage at the input of the DAC under tests in the period i with $i \in (1, L)$ is generated linearly from 0 to 2^N-1 levels. The period T_1 of the analog voltage generated by the DAC under test is given by:

$$T_1 = \frac{2^N}{f_{CLK}} \qquad (1)$$

where f_{CLK} is clock frequency for setting a new digital input code word. The period of generated analog sawtooth voltage T_1 can be adjusted by changing clock frequency f_{CLK} and in such a way the slope of the tested signal can be changed

$$S = \frac{U_{FS}}{2^N} * f_{CLK} \qquad (2)$$

In order to avoid coherence between dithering voltage U_{DITH} and sawtooth voltage the constant L and M must be ordinary prime numbers. To meet the described requirement, we can write the following statement for periods of both signals and also the constant L and M:

$$\frac{T_2}{T_1} = \frac{L}{M} = \frac{f_1}{f_2} \qquad (3)$$

During each sawtooth period in the raising phase the comparator determines the instant when the output voltage of the DAC under test exceeds for the first time the voltage U_{SUM}, which is the sum of the DC voltage (U_{DC}) and the dithering voltage (U_{DITH}). This time instant is determined by a positive derivation of the output voltage of the comparator U_{OUT}. We can write the following condition for this instant:

$$U_{DAC}(k(i)) \geq U_{SUM} = U_{DC} + U_{DITH} \qquad (4)$$

The recorded code word c*(i)* from the DAC under test input match the following conditions:

$$U(k(i, j)) \geq U_{SUM} = U_{DC} + U_{DITH}$$
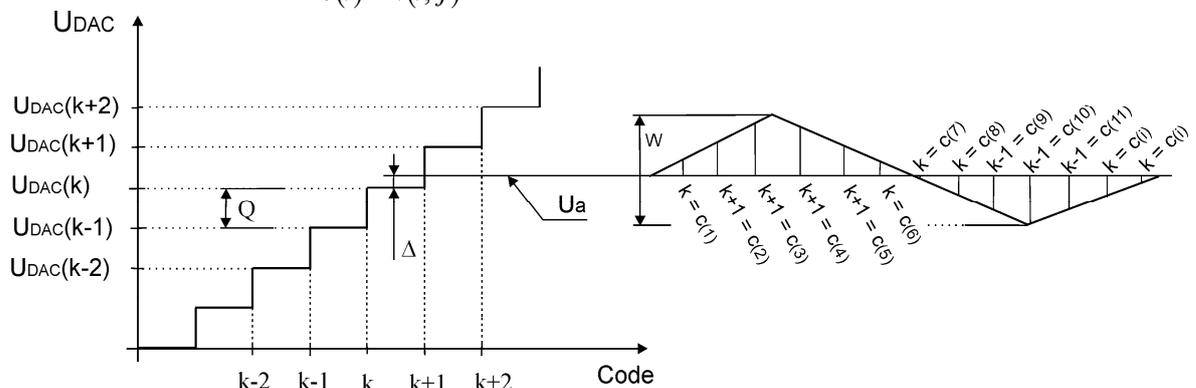$$U(k(i, j-1)) < U_{SUM} \qquad (5)$$
$$c(i) = k(i, j)$$

Figure 3. View of transfer characteristic tested DAC together with reference voltage UDC and dithering voltage UDITH and also the way of obtaining array of input digital code words.

During one measuring period T_M the shift register stores an array of L values c*(i)*, i = 1....L. Those values code words c*(i)* are directly influenced by the difference between U_{DAC} *(k)* and voltage U_{DC}. In real conditions the adjusted reference voltage U_{DC} should be set as close as possible to the measured code level $U_{DAC}(k)$

The measured deviation Δ between real value UDAC (k) and the reference voltage UDC measured by a precise voltmeter is being determined by the following procedure.

At the end of measurement cycle specified by time interval TM the registered array of c(i) values is transferred to a PC. Here the c(i) array is being transformed into a new array p(i), i = 1....L, where for each i value p(i) suit the following condition:

$$c(i) \leq k \quad \Rightarrow p(i) = 0$$
$$c(i) > k \quad \Rightarrow p(i) = 1$$

(6)

This transformation serves mainly to suppress the influence of neighboring quantization levels errors and nonlinearities dithering voltage on the overall accuracy of measurement. In addition makes the measurement almost completely independent of the amplitude and period of used dithering, which considerably simplifies the measuring conditions. From this obtained array *p(i)* is then calculated the average value:

$$\overline{P} = \frac{1}{L} \sum_{i=1}^{L} p(i)$$

(7)

The deviation Δ between real value U_{DAC} *(k)* and analog voltage U_{DC} is than determined by:

$$\Delta = W\left(\overline{P} - \frac{1}{2}\right)$$

(8)

The exact value of the analog output voltage of the DAC under test for code *k* is determined by:

$$U_{DAC}(k) = Ua - \Delta = Ua - W\left(\overline{P} - \frac{1}{2}\right)$$

(9)

If the real value of the DAC analog output voltage is known then we can determine the value of the integral nonlinearity from:

$$INL(k) = \frac{U_{DAC}(k) - k*Q}{Q}$$

(10)

The INL determined from (12) has to be corrected in both ends of FS to zero values. To increase the precision of the determination of the resulting values and the suppression of random effects and interference entering the measurement stand dithering with amplitude several times greater than the amplitude of the ideal quantization step.

III Experimental results

The proposed approach has been evaluated both by simulation, modeling a DAC with imposed nonlinearities and experimentally. Figure 4 shows the so-called front panel of simulator of a DAC testing by using the proposed method, created in LabView environment.
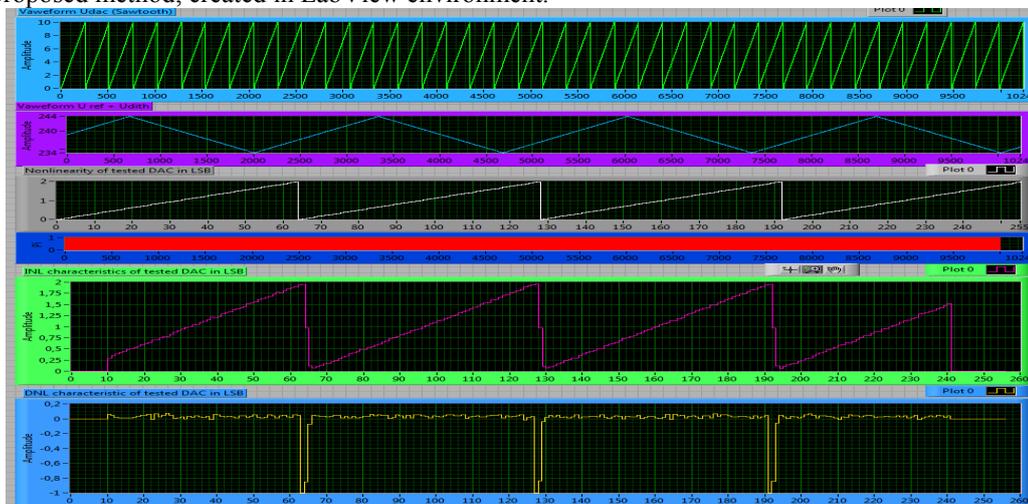

Figure 4.   Front panel of simulation of DAC testing by registration of input code in the moment when the analog output from DAC under test exceeds the reference one for 8-bit DAC.

In this case a 8-bit DAC with known added nonlinearity error (shape is shown in the third graph from the top and amplitude is 2 LSB) and characteristics of Integral and Differential nonlinearities (the last two graphs) evaluated using the proposed method with using the following parameters: number of sawtooth period L=10.000, number of dithering periods M=957 (this ensures that the ratio between frequencies of the DAC analog output voltage and dithering signal is not an integer) The amplitude of the used dithering voltage equal to 10 LSBs of the DAC. Gausian noise with a standard deviation of 0.25LSBwas added to the dither.

Simulation confirmed the expected ability of the method to measure INL and DNL characteristics with high resolution (below 0,25LSB) and also the independence the amplitude and period of used dithering signal. The problem with precise measurements (including the proposed method) is the noise and interference, which adversely affect the resulting measurement accuracy but this is suppressed by using averaging.

The experimental validation of the proposed method was performed by using a commonly available comparator LM 319N, the reference signal ($U_{SUM}=U_{DC}+U_{DITH}$) was generated by a DAQ card NI PCIe 6251 and a 8-bit DAC was tested. As expected, the biggest experimental problem to solve was the influence of noise, which caused oscillation of the comparator at the moment of comparison. Comparator oscillation was suppressed by using hysteresis (HYST=1,6mV corresponding to approximately 1/23LSB of tested DAC). Another problem discovered during the experimental preliminary validation was glitch on DAC analog output sawtooth, or system errors greater than 1LSB near the test level, which can cause incorrect assessment of conditions, resulting in load of incorrect code words (respectively over a set). Negative effects of noise on the measurement discovered during experimental verification were suppressed by using a more suitable arrangement grounding and rearranging the entire involvement. Registering incorrect code words was suppressed using an algorithm that can remove most of the incorrect code words in the registered sequence. A dynamic INL characteristic of the DAC under test obtained by the proposal method are shown in Figure 5. The static INL characteristic obtained by a traditional method is shown in Figure 6.

Figure 5   Dynamic INL characteristic of tested 8-bit DAC for f_{CLK}= 512kHz, obtained by the proposal method using triangular dithering with 10LSB peak to peak amplitude and L=20.000, M=1871
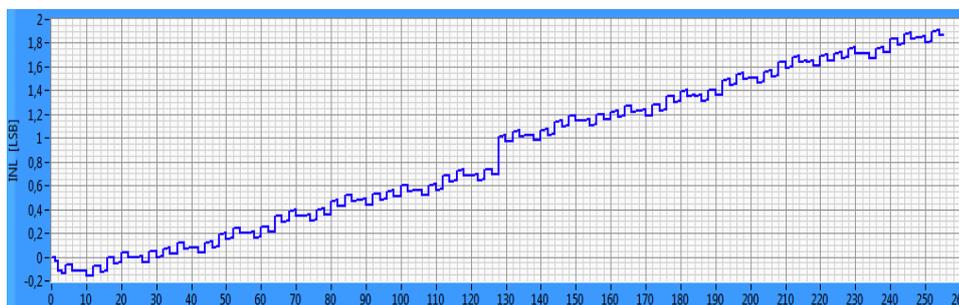

Figure 6   Static INL characteristic of tested 8-bit DAC obtained by known procedures using the precise digital voltmeter Agilent HP34410A

IV. Conclusion

In the paper, a new method for design and implementation of the measurement stand for DAC performance assessment has been presented. The method is primary addressed to the characterization of high resolution DACs

under dynamic condition. It is based on the comparison of the dynamic output voltage of the DAC under test with the reference DC voltage by using a comparator. The output of the comparator is used as the control signal to register the digital input code word of the DAC under test in a fast memory in the moment when the DAC analog output voltage exceeds the reference level.

The advantage of the proposed method is based on the determination of the functional DAC parameters (INL and DNL) in dynamic mode using predominantly digital signal processing of registered data Another advantage of the proposed method is the possibility to test DAC properties for discrete values of slope S. The only restriction for slope selection is that L/M must be ratio of two prime instruments or the time step ΔT must be integer number of minimal time intervals.

The method relies on the properties the precise DC voltmeter. DC voltmeter is the instrument where required precision is highest in comparison to other instrument for the same price. A fast and precise comparator is required. Its time invariant errors could be removed by digital post processing.

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