

An LCF-ADC Model Using Co-simulation Technique

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Abstract-Event-driven analog-to-digital conversion, particularly level crossing A/D conversion (LC-ADC), and associated signal reconstruction techniques are still novel approaches that need further improvements to be more efficient in term of energy consumption and bandwidth resources. Among several components, this type of converter is composed of a timer block, which essentially controls the output resolution and reconstructed signal. In this paper, Authors present a level-Crossing Flash ADC (LCF-ADC) model made with Co-simulation technique where Simulink ADC model and HDL timer are associated. Besides, different interpolation algorithms are studied for signal reconstruction.

Keywords: LCF-ADC; mixed modeling; Timer; reconstruction of signal.

I. Introduction

Basically, all physical signals are analog and most of them are non-stationary with different statistical properties. Traditional A/D converters (ADC) are based on uniform sampling according to the Shannon theorem plus quantization process. So it can digitalize useless information, especially for signals with small sporadic variation such as electrocardiogram, phonocardiogram, seismic signal, etc... In this case, this approach is not efficient regarding the power consumption.

To solve this issue, many event-based approaches have been proposed: jittered random sampling, additive random sampling, uniform sampling with random skip, additive pseudorandom sampling, signal crossing sampling and level crossing sampling [1]. All these sampling techniques are non-uniform.

The study described in this paper focuses on the level crossing sampling technique. First, level crossing sampling scheme is presented. Then, LCF-ADC model is reviewed with a particular attention on the timer block model. Finally, this paper is concluded after describing the signal reconstruction method used.

II. General Basics

A. Level Crossing Sampling Scheme (LCSS)

The concept of level crossing sampling, also known as an event-based sampling, is described in Figure 1. The sample is captured only when the analog input signal crosses a predefined threshold. It means that samples are not equidistant in time. Actually, the time interval between each of them depends on the variation of the input signal.

The choice of the level distribution is related to the variation of the input signal $x(t)$. Figure.1 represents a linear distribution of the thresholds, where q is defined as the quantum.

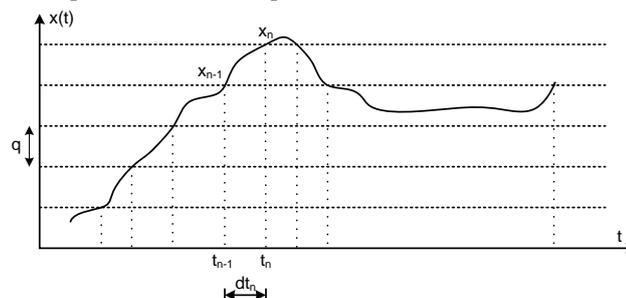


Figure 1. Level crossing sampling process.

For this type of sampling, each sample is referenced by coordinates (x_n, t_n) , where x_n and t_n are respectively the amplitude and the sampling time. x_n corresponds to a threshold whereas t_n can be calculated as follows:

$$t_n = t_{n-1} + dt_n \quad (1)$$

where t_{n-1} is associated with the previous sample and dt_n the time interval between them.

B. Level crossing A/D conversion

For a classical ADC, sampling instants are known, where the samples amplitude are quantized at the ADC resolution. The resulting quantization error can be illustrated by the Signal-to-Noise Ratio (SNR). Using input sine wave that spans the ADC full scale range, theoretical SNR of an ideal ADC can be expressed by the following equation:

$$SNR_{dB} = 6.02N + 1.76 \quad (2)$$

where N is the ADC resolution.

For an ADC using LCSS, amplitudes of sample are known exactly, while sampling instants are unknown and quantized at the timer resolution. In practice, a clock is used to store the sampling times. A temporal error (δt) occurs because of the finite clock resolution. If T_{timer} is the clock period, δt has a value in the range $[0, T_{timer}[$. During the reconstruction process, this time error generates an amplitude error δv according to the following relation:

$$\delta v = \left(\frac{dx}{dt} \right) \delta t \quad (3)$$

As δt is considered uncorrelated to the input signal, it can be modeled by a white noise [2]. So, the two terms in the right-hand side of (3) is considered as two independent random variables. To simplify our calculus but without lack of generality, the first one is supposed to be a zero mean random variable and the second one is uniformly distributed in $[0, T_{timer}[$. Consequently the SNR can be expressed as:

$$SNR_{dB} = 10 \log \left(\frac{3P}{P} \frac{x}{x} \right) - 20 \log T_{timer} \quad (4)$$

where x' is the input signal sampled at the timer instant. If the input signal $x(t)$ is a sinusoidal, according to [2], the SNR becomes:

$$SNR_{dB} = -11.19 - 20 \log \left(F_{sig} T_{timer} \right) \quad (5)$$

where F_{sig} is the input signal frequency.

LC-ADC has many advantages like reducing energy consumption and minimizing the silicon area. Indeed, this technique enables to simplify the analog part of the ADC. Moreover, it is adapted for a non-stationary signal and it has low electromagnetic emission. In addition, as shown in (5), if F_{timer} is doubled then effective number of bit (ENOB) increases by one bit.

As described above, we have formulated the SNR for the LCSS, as it is an essential parameter to evaluate its performance. In the next section, a mixed model of LC-ADC obtained by co-simulation method using MATLAB, SIMULINK and MODELSIM is presented.

III. LCF-ADC Model

In this study, a four bits flash ADC is used for our model (as presented in Figure 2) and simulated using MATLAB code, SIMULINK models and HDL code. To link the two first representations to the last one, an EDA simulator link has been used. This link ensures a bidirectional communication between HDL simulator and MATLAB server. Usually, co-simulation is employed to verify different steps of synthesis process.

The first part of the LCF-ADC is based on a previous work detailed in [3]. It is exploited to provide values to timer block that is detailed in the next subsection.

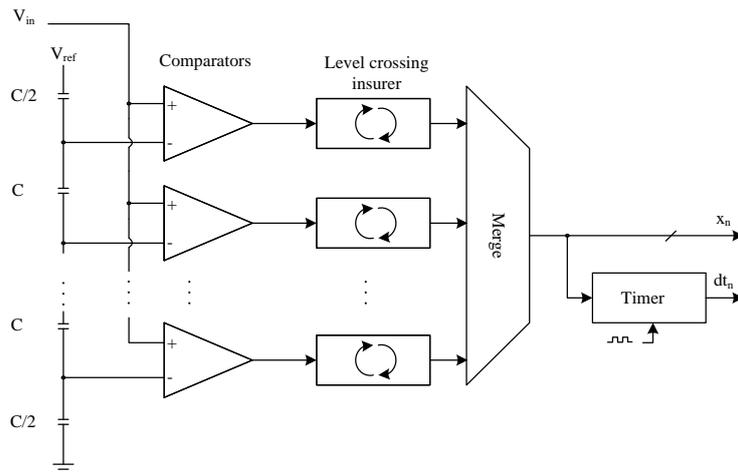


Figure 2. LCF-ADC Model.

A. Timer

As mentioned above, LC-ADC has as outputs a couple of values; the sample amplitude and its period of time. The timer is the major part of the model. It is described by a HDL language and linked to the model via EDA link. The timer operating principle is similar to the Time-to-Digital Converter (TDC), which quantifies time intervals between two rising edges [4]. Those rising edges will be generated at each level crossing.

The timer needs an external clock and its period is determinate thanks to the relationship:

$$T_{timer} = \frac{10^{\left(\frac{SNR+1.19}{-20}\right)}}{F_{sig}} \quad (6)$$

To achieve the SNR specified in (6), the timer should be realized with the following constraint: the error between the true sampling instant and the measured one has to be in the range $[0, T_{timer}]$. This condition is necessary to avoid additive non linear error. Figure 3 shows the timer time error and validates the timer model described in HDL language.

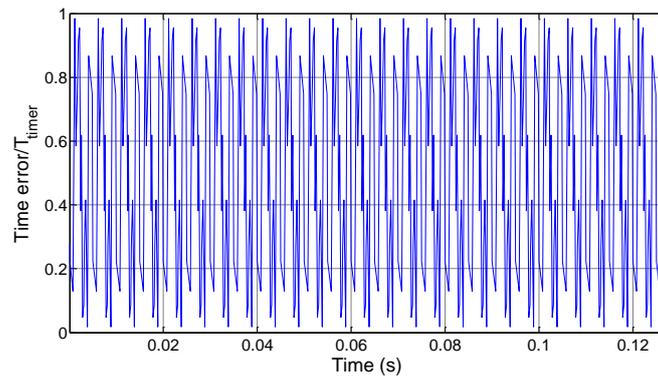


Figure 3. Timer error of the timer.

B. Signal reconstruction

Figure 4 presents dt_n measures. This figure shows that at each sample this parameter is under the Nyquist period (T_{nyq}). Therefore, referring to H.G. Fechtinger and al. [5] the obtained irregular sequence can be reconstructed.

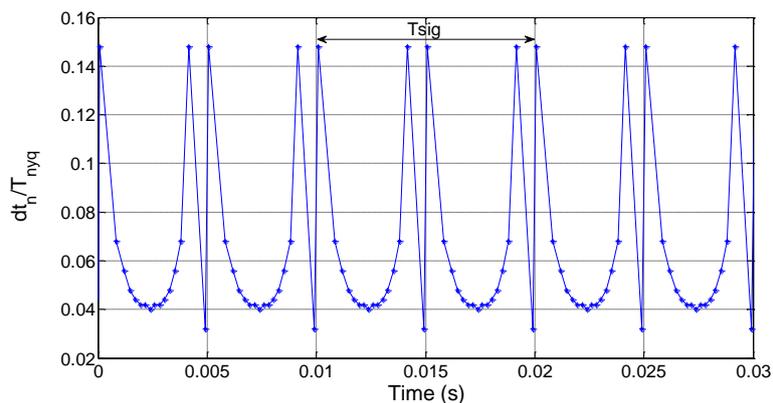


Figure 4. Time intervals measure for a 100 Hz sinusoidal signal.

To rebuild the original signal, many approaches are proposed in literature and some of them are described in [6-8]. Thus, the interpolation approach is chosen. It consists in uniformly re-sampling the irregular sequence. A comparison of different interpolation methods has been done: spline, cubic, linear and nearest neighbor. Table 1 shows SNR and ENOB obtained using these interpolation methods as well as and the theoretical ones obtained from (5).

<i>Interpolation Methods</i>	<i>SNR (dB)</i>	<i>ENOB (bit)</i>
<i>Spline</i>	65.001	10.506
<i>Cubic</i>	47.980	7.677
<i>Linear</i>	38.391	6.085
<i>Nearest neighbor</i>	24.970	3.855
<i>Theoretical value (5)</i>	66.737	10.793

Table 1. Reconstructed method performances comparison with theoretical measurements.

As shown in Table 1, the more the interpolation technique is efficient the more the SNR measurement is close to the theoretical SNR value.

Figure 5 shows the power spectral density (PSD) of the reconstructed signal using spline method.

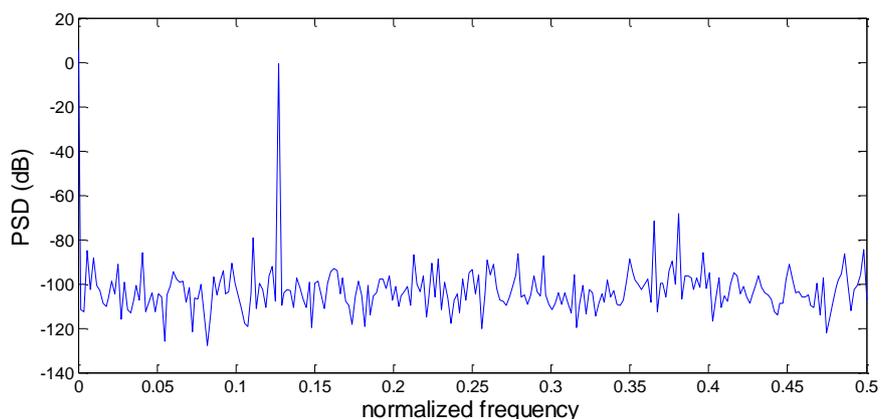


Figure 5. Reconstructed signal with spline method PSD.

IV. Conclusion

In this paper, an LCF-ADC model was presented. This model was realized using a co-simulation with MATLAB/SIMULINK and MODELSIM. It allows us to use a new timer block model described in HDL language. This block is very important as the reconstruction process performance depends on the precision of the measurement of the time sampling instants. After the implementation and the validation of this block, different interpolation algorithms have been studied for the signal reconstruction. By this way, it was confirmed that Spline methods is the best solution in terms of precision.

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