Power optimization of High-resolution Low-bandwidth SC ΔΣ Modulators

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Abstract- This paper presents a procedure for the power-optimal design of high-resolution low-bandwidth switched-capacitor (SC) ΔΣ modulators (ΔΣMs). The most power efficient ΔΣ architecture is identified among single-loop switched-capacitor (SC) feedback (FB) and feed-forward (FF) topologies with different loop order N, oversampling ratio OSR, and quantizer resolution B. Based on the results obtained, an experimental prototype is implemented in a 0.18μm CMOS process, achieving a signal-to-noise ratio (SNR) of 95 dB over a signal bandwidth f_{BW} of 10 kHz. The prototype operates with a 1.28MHz sampling rate and dissipates a total power of 210uW from a 1.8V supply.

I. Power optimization procedure

Low bandwidth (up to few tens of kHz) high resolution (>14 bits) Analog-to-Digital Converters (ADCs) are important for portable biomedical devices, such as digital hearing-aids [1]. These applications require large dynamic range (*DR*) as well as very low power consumption in order to extend battery lifetime. We address this ultra-low-power challenge by presenting a procedure for the power-optimal design of high-resolution ΔΣ modulators (ΔΣMs). This study is focused on switched capacitor (SC) single-loop architectures, both feedback (FB) and feed-forward (FF). A block diagram of FB and FF single-loop ΔΣMs implemented using SC techniques is shown in Figure1.a and Figure1.b respectively. Single-loop architectures are more robust to circuit non-idealities [2] and can be made conditionally stable by properly setting the loop coefficients [3].
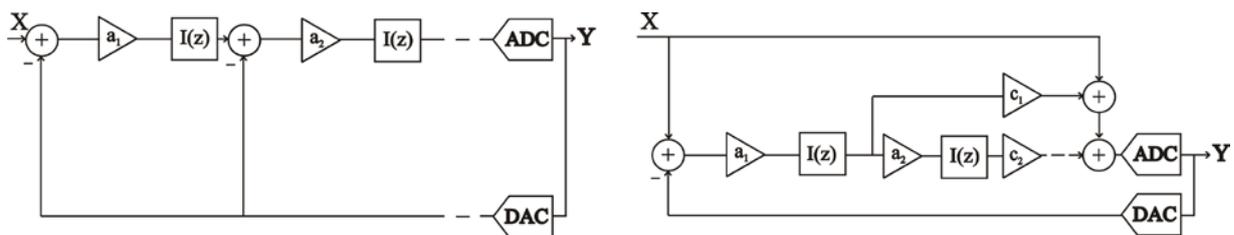

Figure 1. Conventional second order FB (a) and FF (b) single loop ΔΣ modulators.

The first step toward the implementation of the modulator consists in selecting the architecture that can fulfill the specifications with the best *FOM* (see Table II). To identify the power optimal ΔΣM it is necessary to explore the solution space defined by the three main design variables that determine the Effective Number of Bits (ENOB) of ΔΣMs [4]: *N*, *OSR* and *B*.
For each combination of these variables, the power consumption is estimated by first calculating the minimum value of C_s which allows to achieve the specified *ENOB* and f_{BW} and then by evaluating the different power contributions.
C_s is calculated from the *DR* requirement according to [4]:

$$DR = 3 \cdot 2^{2 \cdot ENOB-1} = \frac{P_{in,MAX}}{P_{Th}} = \frac{V_{in,MAX}^2 \cdot OSR \cdot C_s}{2kT} = \frac{(V_{ref} \cdot OL)^2 \cdot OSR \cdot C_s}{2kT} \tag{1}$$

where P_{Th} is the in-band thermal noise power, and $V_{in,MAX}$ is the full-scale input range for stable operation of the modulator. V_{ref} is the integrators' reference level and OL is the overload level, which is $V_{in,MAX}$ normalized to V_{ref}. In this expression only the thermal noise from the switches is considered [4].

Matching requirements set another constraint for the value of C_s. The total capacitance implementing a B-bit feedback DAC has indeed the same size as the correspondent sampling capacitor and it is composed by 2^B-1 unit elements C_u. The matching accuracy of its unit elements has to be of the order of resolution of the entire $\Delta\Sigma$ modulator according to:

$$3 \cdot \frac{\sigma_{C_u}}{C_u} = \frac{1}{2} \frac{1}{\sqrt{2^{ENOB}}} \tag{2}$$

Once the minimum value of the first-stage sampling capacitor C_s is known as a function of N, B and OSR, it is possible to estimate the power dissipation of the $\Delta\Sigma$ modulator. The total power consumption P_{TOT} consists of four contributions: the static power P_{STAT} of the integrator stages, the dynamic power P_{DYN} for charging the load of the integrator stages, the power dissipated by the quantizer P_{QUANT} and the digital power dissipated by the circuitry implementing the DAC mismatch-shaping system, based on data weighted averaging, P_{DWA}.

In single loop $\Delta\Sigma$ architectures, the OTA static power is determined by the settling requirements rather than by the DC gain [3]. A conservative choice to ensure settling of the amplifier before the subsequent sampling moment is $GBW = 5 \cdot f_s = 5 \cdot OSR \cdot (2 \cdot f_{BW})$, where GBW is the OTA gain-bandwidth product [6]. In both $\Delta\Sigma$M architectures, a two-stage Miller OTA topology has been considered as in [4]. The dynamic power for charging a capacitor C_{TOT} at the frequency f_s to the reference voltage is $P_{DYN} = V_{ref}^2 \cdot C_{TOT} \cdot f_s$. C_{TOT} is the total capacitance in the $\Delta\Sigma$M and can be expressed as a function of Cs: it is approximated to 4xN capacitances in FB topologies [6], and to the sampling and integrating capacitors of the first integrator in FF topologies. The power dissipated by a B-bit flash quantizer comprising 2^B-1 comparators has been calculated as in [8]. Finally, the digital power penalty for correcting the capacitor mismatch error by using the data weighted approach (DWA) [8] has also been taken into account.

To identify the most power-efficient $\Delta\Sigma$ modulator configuration able to achieve a DR of 98dB (ENOB=16) within a 10-kHz signal bandwidth we have considered $N \in [2, 4]$, $B \in [1, 5]$ and $OSR \in [16, 128]$. In Fig.2, for each combination of N, B satisfying the modulator specifications, P_{TOT} is drawn as a function of OSR. Incomplete curves represent combinations not able to achieve the target resolution.
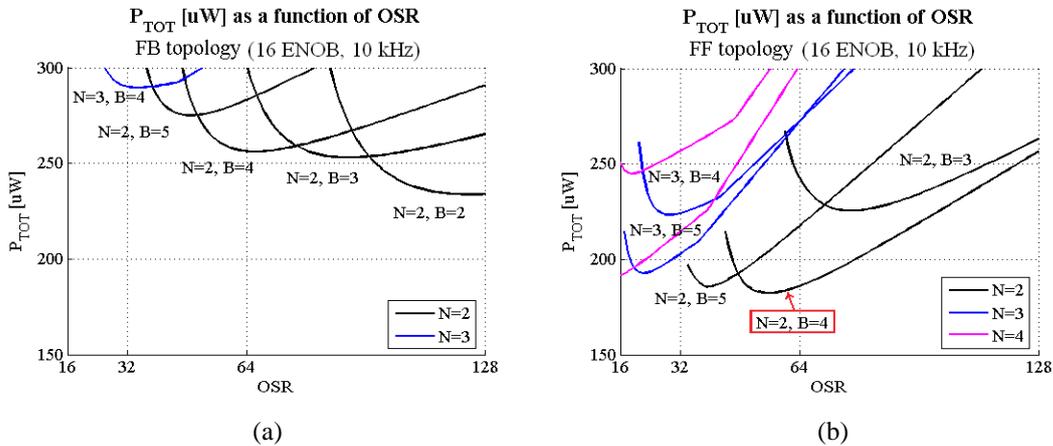

Figure 2 . Estimation of P_{TOT} as a function of OSR in FB (a) and in FF (b) implementations

FF architectures exhibit lower power consumption: the signal passing through the loop filter in FF modulators is the quantization noise, which is much smaller than the input signal in amplitude. Therefore, the ability to handle input signals is increased without overloading the quantizer, and higher OLs minimize the sampling capacitor size accroding to Eq.(1) [4]. The power efficiency is higher for low-order circuit topologies and the minimum power consumption is obtained both for FF and for FB architectures with a second order modulator: P_{STAT} and P_{DYN} terms dominate the overall power budget and their values are minimized for a small number of integrator stages. Multibit implementations are preferred over single-bit ones, because multibit quantizers further reduce the internal swings inside the filter loop; the best efficiency is achieved for B=4. OSR is approximately 64, so that f_s= 1.28 MHz.

This power optimization methodology is confirmed by recent works in the literature. The best power-efficiency relies on a second-order, 4-bit ΔΣM as in [9]; this implementation chooses indeed to dimension the capacitances following a procedure similar to the one described in this paper, targeting the same resolution and bandwidth.

II. SC implementation

To validate the results obtained with the described power optimization procedure, a second order 17-levels FF ΔΣM has been designed at transistor level. Figure 3 illustrates the implementation of the modulator, drawn as a single-ended circuit for simplicity; the actual implementation is fully differential.
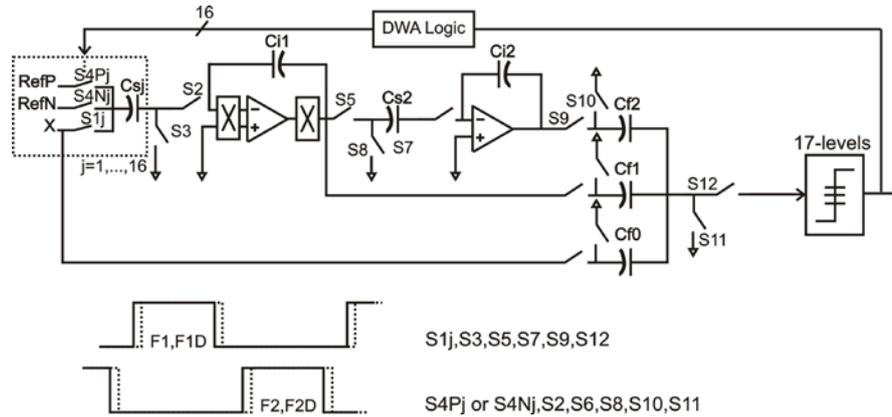

Figure 2.SC implementation of the FF modulator

TABLE I
CAPACITOR SIZES OF THE ΔΣM

Sampling capacitors	Integrating capacitors	Feed-forward capacitors
		$C_{f0} = 2*36.5$ fF
$C_{s1} = 2.08$ pF	$C_{i1} = 0.32$ pF	$C_{f1} = 7*36.5$fF
$C_{s2} = 0.32$ pF	$C_{i2} = 0.32$ pF*5/9	$C_{f2} = 15*36.5$fF

The performance of single-loop architectures is greatly influenced by the in-loop coefficients (see Fig. 1.a and 1.b). On the one hand, these coefficients have to be selected to provide a stable operation in the whole input range [10]. On the other hand, they can be scaled in order to reduce the swing at the outputs of the integrators with respect to the reference voltage [12]. The values of the in-loop coefficients have been selected using the "Delta Sigma Toolbox" for Matlab [13], being adjusted so that the integrators output range is 50% of the reference level. This makes the design of the OTAs easier, especially when considering a low voltage for the supply [4]. The first integrator sampling capacitors are dimensioned from kT/C noise requirements according to Eq.(1) and they consist of 16 unit capacitors, $C_u = 0.13$pF. The size of the sampling capacitors in the subsequent stage can be reduced as the noise requirements drop; considering the matching property of the capacitors, the second sampling capacitor is set to 0.32 pF. The feed-forward signals are summed by a passive adder and then fed to the 17-levels quantizer. All the capacitor sizes are summarized in Table I. Note that the first amplifier includes a chopper technique to attenuate the influence of its offset and low-frequency noise. The timing of the modulator consists of two non-overlapped phases and two delayed versions of them, used to avoid signal-dependent charge injection.

The reduced output voltage swings allows use of single-stage OTA instead of the two-stage architecture assumed in the theoretical model. In the actual implementation, a single-stage folded-cascode OTA has been chosen. The multi-bit quantizer consists in 16-comparators Flash ADC. ΔΣMs show little sensitivity to the static and dynamic errors induced during the internal quantization, as the position of the quantizer in the loop causes these errors to be shaped and attenuated in the signal band. For this reason, a dynamic architecture like the one in [14] is used for the fully-differential comparator. The output codes of the multi-bit quantizer are the thermometric codes driving the unit-elements of the feedback DAC after the DWA operation. Five binary outputs, from B0 to B4, form the output data of the quantizer and are given as input to the DWA block.

III. Implementation results

Table II summarizes the power consumption and *FOMs* values for the theoretical model and for the simulated prototype; power contributions are detailed for both cases. In simulation the static power is 1.2x times lower that the one predicted by our calculations. In the theoretical estimation a conservative approach has been applied as P_{STAT} is calculated for a two-stage Miller OTA, while in our implementation a power-efficient single-stage OTA has been used. The dynamic power consumption is the same in both cases since the capacitances have been dimensioned following the procedure described in this paper. On the other hand, our theoretical estimation does not include power contributions present in the real implementation: the resistor string in the Flash ADC makes the quantizer contribution higher than predicted; the clock generator circuit determines additional power consumption not considered in our calculations.

TABLE II

	THEORETICAL MODEL	TRANSISTOR LEVEL IMPLEMENTATION
N	2	2
B	4 (17 LEVELS)	4 (17 LEVELS)
OSR	64	64
C_s **[pF]**	1.92	2
P_{TOT} **[µW]**	186	210
FOM **[pJ/c.s.] ***	0.2	0.23
P_{STAT} **[µW]**	110	96
P_{DYN} **[µW]**	48	48
P_{QUANT} **[µW]**	10	28
P_{DWA} **[µW]**	18	20
Other contributions [µW]	-	20

$$^*FOM = \frac{P_{TOT}}{2 \cdot f_{RW} \cdot 2^{ENOB}} [\,J\,/\,conv.step\,]$$

Figure 4 shows the comparison between output spectra obtained by transistor-level simulation in Cadence environment (blue curves), and by behavioral simulation in Simulink enviroment (red curves). SNDR and ENOB values in the inset result from the transient noise simulations of the ΔΣM, in which both the OTAs and the Flash ADC are described at transistor-level.
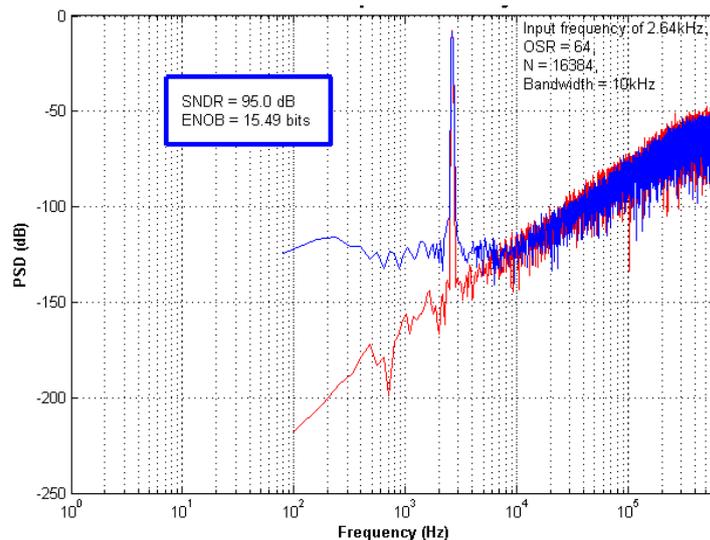

Figure 4.Output spectra obtained by transistor-level simulation in Cadence enviroment (blue curves) and by behavioral simulation in Simulink enviroment (red curves).

Figure 5.a and 5.b show the output spectra obtained by transistor-level simulation with post-layout extraction (in blue), and by behavioral simulation in Simulink (red). In Figure 5.a, the OTAs are post-layout extracted while the Flash ADC is simulated at transistor-level; in Figure 5.b, the OTAs are simulated at transistor-level while the

Flash ADC is post-extracted. This approach has been chosen to avoid the post-extracted simulation of the whole ΔΣM which turned out to be too time-consuming. In all the simulations, chopper operation is activated.

The good agreement between the curves simulated at behavioral level and the curves simulated at transistor-level confirms the validity of the design of the modulator.
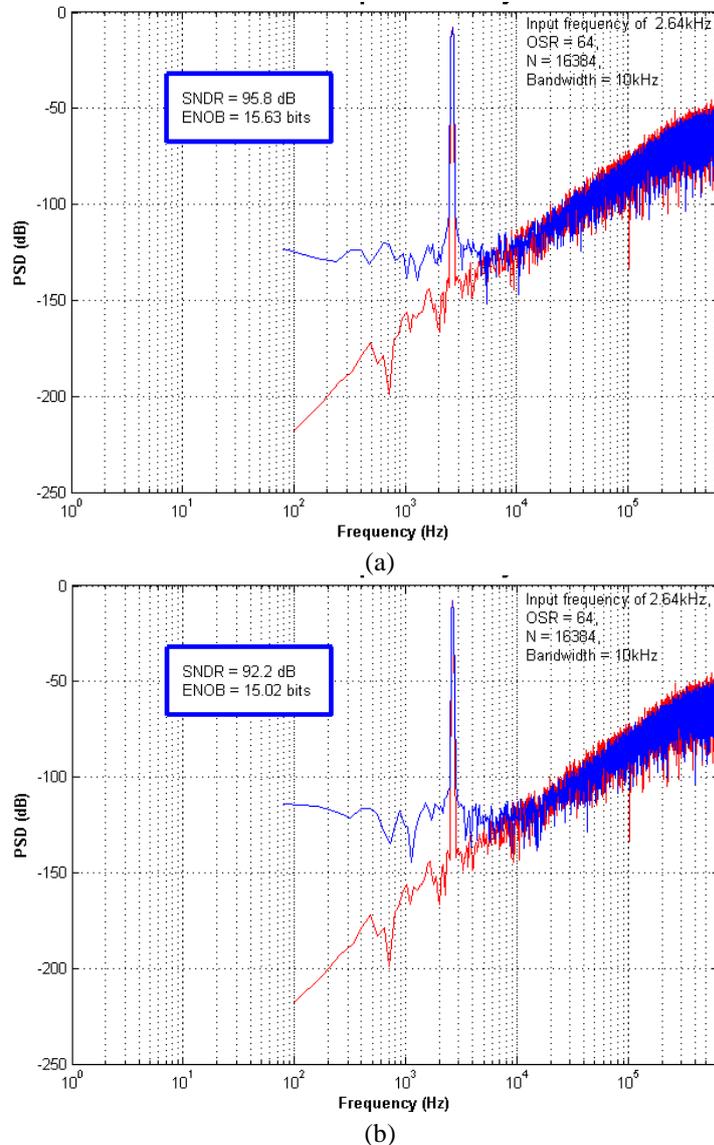

(a)

(b)

Figure 5.Output spectra obtained by post-extracted simulation in Cadence enviroment (blue curves) and by behavioral simulation in Simulink enviroment (red curves).

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