Audio ADC for mobile applications featuring a novel gain control technique, dithering insertion and idle tones shifting

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Abstract- One of the main parts in the audio uplink path for mobile transceivers is an Analog-to-Digital-Converter (ADC) operating in the audio band. The ADC is usually preceded or followed by a Programmable Gain Amplifier (PGA) which allows, together with a digital signal processor, the gain control of the audio transmit path. Changing the gain is an operation which can lead to artifacts as it inserts discontinuities in the audio wave which behave as distortion sources. This paper describes a novel technique for embedding the gain change in the ADC body. In particular, this technique allows a smooth gain change directly in a sigma delta ADC [1] reducing distortions effects and replacing the programmable gain amplifier in the uplink chain, hence allowing performance enhancement and area and power reduction of the overall integrated circuit (IC). In addition, possible implementations of dithering at a minimum area overhead are discussed.

I. Introduction

The audio uplink subsystem of a typical present-generation mobile-telephone transceiver has the structure that is shown in Figure 1, where a Pre Amplification (PreAmp) stage and Programmable Gain Amplifier (PGA) feature a controllable gain architecture. These stages are placed before the audio ADC and works together with a Zero Crossing Detector (ZCD), to form a gain change control loop. Since the gain change can cause plop or click noise in audio systems [2], the ZCD will detect the zero crossing of the input signal and will allow the gain switching only when the signal amplitude is very close or equal to zero. This technique reduces the noisy effect.
The aim of this paper is to describe a novel technique for embedding the gain change in the ADC body that allows the implementation of a smooth gain change directly in it. The technique reduces distortion effects and enables the replacement of the programmable gain amplifier, with performance enhancement as well as circuit area and power reduction.

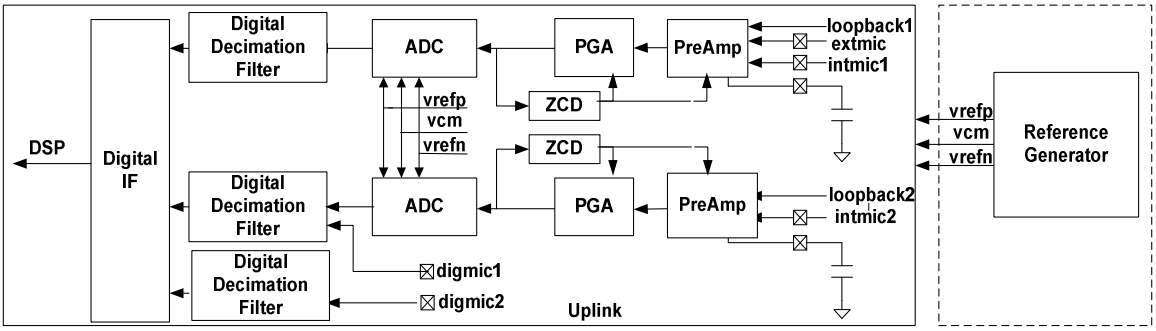

Figure 1: Audio uplink path for mobile telephone block diagram

II. Gain control in the Audio uplink path for mobile application

A. The novel gain switching method

The ADC described in this paper adopts a 1-bit feed-forward third-order switching caps sigma delta as shown in Figure 2. It has been modeled and tuned as described in [3], from which the resulting transfer function is

$$\frac{\left\{s_1 + (g_3 \cdot s_3 - s_2) \cdot g_2\right\} + (s_2 \cdot g_2 - 2 \cdot s_1)z + s_1 \cdot z^2}{z^3 - 3z^2 + 3 \cdot z - 1} \qquad (1)$$

where g_1, g_2, g_3, g_{ref} represent the integrators and DAC coefficients, given by the ratios between sampling and

integrating capacitor, while s_1, s_2, s_3 are the ratios between the respective capacitor in the adder and their sum. The *gref* coefficient is implemented by two capacitors and switches and allows the change of the overall gain, by changing the feedback coefficient of the system. In particular, the proper *gref* coefficient can be selected by adopting a set of capacitors and a binary switching algorithm, as described in Figure 3.

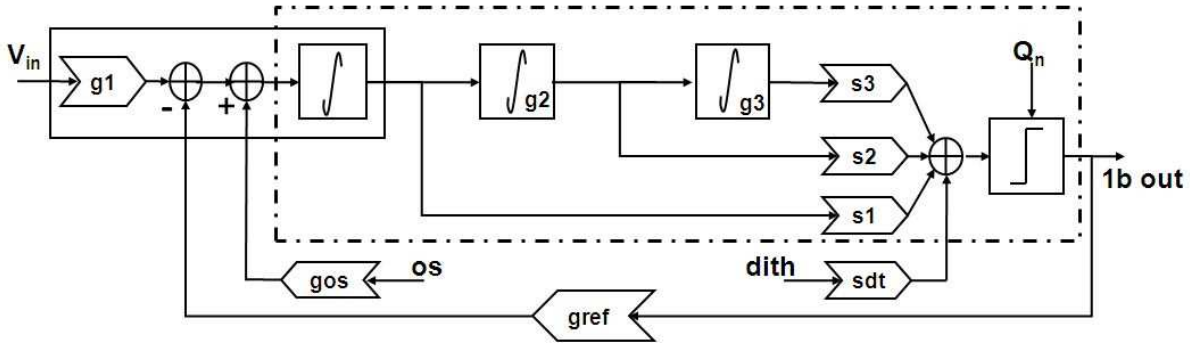

Figure 2: Model block diagram with offset (os) and dithering (dith) insertions.
(dashed line represents Open Loop section)

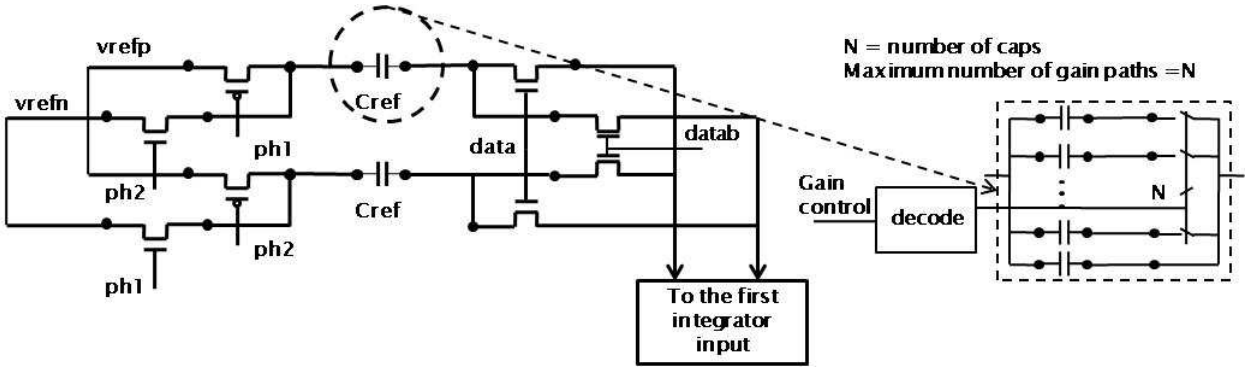

Figure 3: *Gref* coefficient and switching gain capacitors implementation details.
(ph1 and ph2 are two opposite clock phases, data and datab are opposite output data feedbacks)

Each capacitor represents a binary weight and their combination allows the implementation of a large number of possible values. Since 11 possible gain settings have been used in the case study that it is going to be fabricated in silicon, 3 gain control bits are adopted to set-up the proper combinations of binary weighted capacitors that give the resulting values, according to the table shown in Figure 4.

decoded bits →	gain-set <0>	gain-set <1>	gain-set <2>	gain-set <3>	gain-set <4>	gain-set <5>	gain-set <6>	
always on 1	binary weights (in number of unit caps)							
1	0.125	0.25	0.5	1	2	4	8	total unit caps 1
ON				ON	ON		ON	12.00
ON			ON				ON	9.50
ON	ON		ON		ON	ON		7.63
ON				ON		ON		6.00
ON		ON	ON	ON	ON			4.75
ON		ON	ON		ON			3.75
ON					ON			3.00
ON	ON	ON		ON				2.38
ON	ON	ON	ON					1.88
ON			ON					1.50
ON		ON						1.25

Figure 4: Capacitor selection: the decoding and switching table

It is easy to verify that the step between each of the 11 gain settings corresponds to a gain change of 2dB.
To further smoothen the transition and the consequent audible unwanted effects, a switching algorithm that adopts a PWM (Pulse Width Modulation) on each gain step change is realized. This is possible because of the low rate of the gain changing, if compared to the ADC clocking frequency.

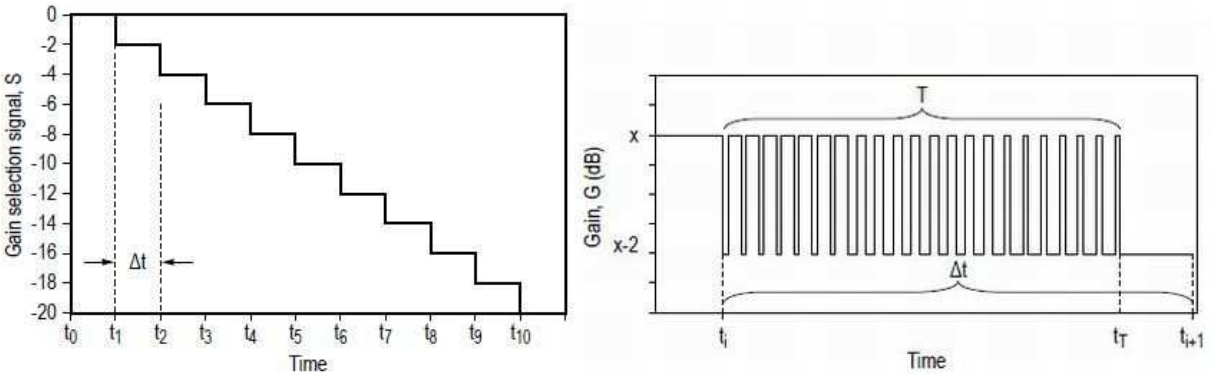

Figure 5: Staircase gain switching example (left) and PWM driving method (right)

The signal driving the capacitor switches changes linearly its duty cycle from 0 to 1 in a T transition time, whereas the gain is slowly switched in 2dB steps. The improvement achieved by this novel switching method is clearly visible when plotting the reconstructed waveform and comparing the two cases with and without PWM stepping, as it is reported in Figure 6, where the smoother gain change effect is appreciable.

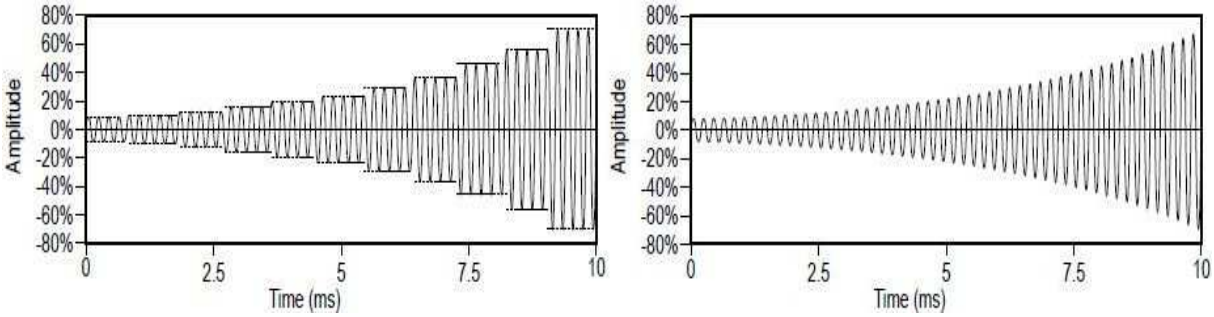

Figure 6: Staircase gain switching reconstructed waveforms: without PWM (left) and with PWM (right)

B. Gain switching parameters tuning

The behavior of the gain control is affected by a number of parameters such as:
f_s = sampling frequency (6 MHz);
T = transition duration; determines the duration of the gain transition (a ramp in the example),
g_o = old gain value (in the range 0-20dB in steps of 2 dB);
g_n = new gain value (in the range 0-20dB in steps of 2 dB);
N_{pwm} = PWM pulses; determines the number of clocks cycles in a PWM controlled transition.
If we assume a 2 dB minimum step size the following relations hold:

$$\frac{\left|g_o - g_n\right|}{2} = \text{number of 2 db steps in a gain transition} = n_{steps} \quad (2)$$

$$\frac{2*(f_s*T)}{\left|g_o - g_n\right|} = \text{number of clock cycles in a 2 db step} = ns_2 \quad (3)$$

$$1 < N_{pwm} < ns_2 \quad (4)$$

Based on previous relations two implementation options are possible:

1) set the transition time T, calculate ns_2 and program N_{pwm} in the given range
2) set ns_2, calculate t_t and program N_{pwm} in the given range

Option 1 is probably preferable at system level, as gain transitions will have a uniform duration. It should also be considered that a transition time long enough to smoothen the transition and a sufficient number of pwm pulses are needed, to really enjoy the benefits of the PWM switching.
In standard audio application, the transition time for gain change is not a critical parameter as the rate of the gain change signal is very low (normally below 10 kHz). However, the value of t_{pwm} is programmable in the designed silicon case study, so that the best settings can be found during the validation phase.
The N_{pwm} value has an impact on the spurious position during the gain transition, as it is revealed by the simulations. In fact, the Discrete Fourier Transform (DFT) of the signal reveals the position of the spurious components in the frequency band of interest. Figure 7 shows two simulation results featuring the DFT of a 5 kHz sine input, when the gain is switched from 0 to 10 dB in 10 ms, for two different values of N_{pwm}. Note that the maximum value of $N_{pwm} = ns_2$ is 1200 clock cycles, in this case.

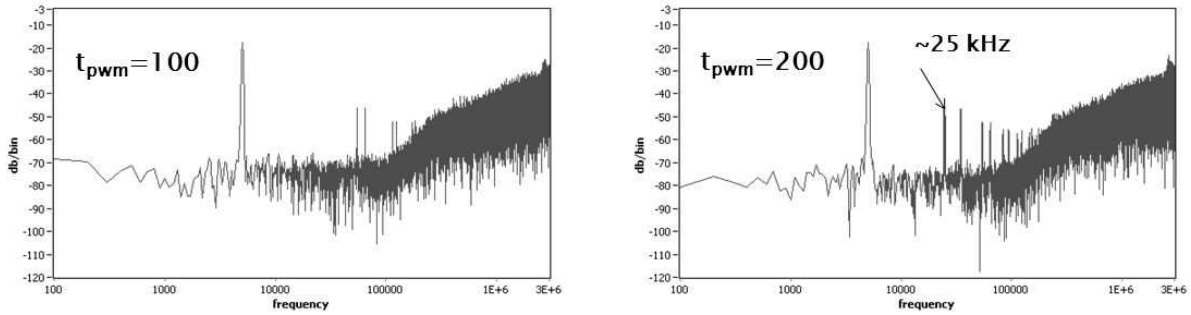

Figure 7: DFT plots of PWM modulated gain transition output waves for two N_{pwm} values

It should finally be noted that the gain changing technique changes the ADC transfer function in the desired way, but it also affects the dithering path causing its effect to be amplified by the gain value.

III. Gain and output amplitude dependent dithering

For a full suppression of idle tones a 0.5 LSB dithering should be added to the input signal just before the 1 bit quantizer [4]. On delta sigma converters this could lead to saturation and instability [5], as well as to an influence on the noise floor, as it is possible to notice in Figure 8. Dithering must be limited in order to prevent such effects.

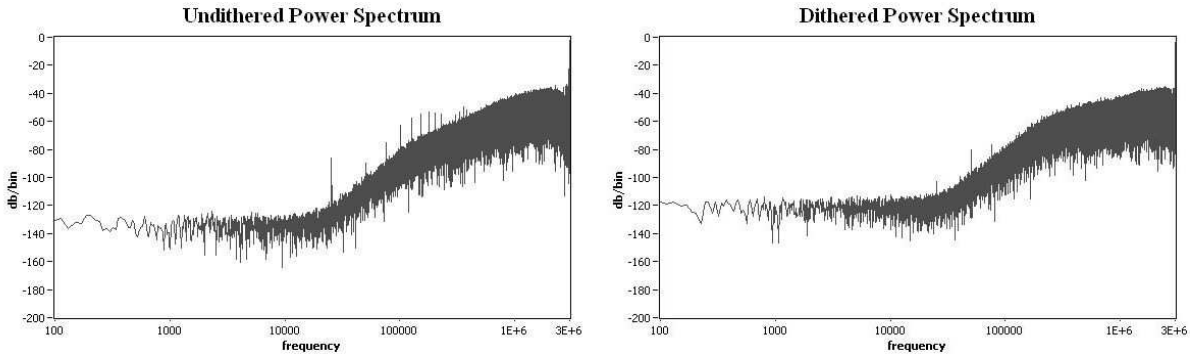

Figure 8: Undithered vs. dithered idle channels power spectrum plots width 6 mV input offset.

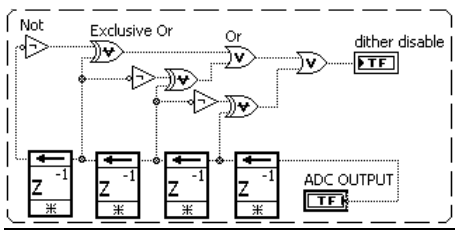

Figure 9: Dither disable filter

The dithering effectiveness is associated with the rms value of the dithering signal, as it is shown in [5].
By monitoring the output signal it is possible to detect when the output is reaching the saturation limits and to prevent the dithering insertion, which would be not useful. The output monitoring has been implemented by a simple digital filter that collects four consecutive output samples and disables dithering in the occurrence of two equal samples out of the last four monitored samples as shown in Figure 9.
The evaluation of the maximum dithering coefficient at each gain

value has also been done and a consequent gain based tuning of the dithering coefficient has been applied. This, together with the above described monitoring of the output level, prevents the system to enter the saturation critical regions.

IV. Stability analysis

The stability has been analyzed by plotting the root locus of the open loop transfer function at (1). It must be considered that the gain applied to the system depends on the nonlinearity introduced by the comparator as described in [6]. Let us define $Vcomp_{in}$ as the voltage at the comparator input. By referring to Figure 3, we say $Vref = Vref_p - Vref_n = 2$ V. The gain of the feedback loop is expressed as:

$$K = \frac{Vref * gref}{Vcomp_{in}} \quad (5)$$

The resulting analysis gives the critical gain for stability $K_f = 0.42$ as shown in Figure 10. Considering that $Vref = 2$ V and $gref_{nom} = 0.32$, we get the condition for the comparator input to result in a stable system:

$$Vcomp_{in} < \frac{Vref * gref}{K_f} = 1.5V \quad (6)$$

And when the maximum gain is applied $gref = 0.1 * gref_{nom}$ the condition will become:

$$Vcomp_{in} < 0.15V \quad (7)$$

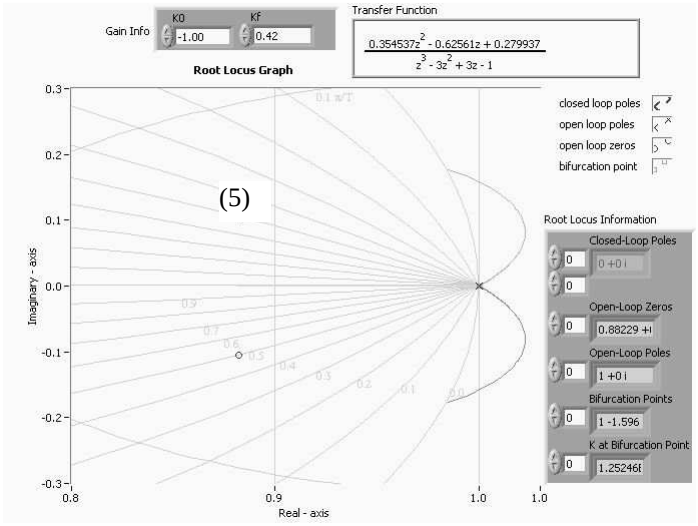

Figure 10: Root Locus of the system

The comparator input histogram has been plotted to verify those conditions.
The input range has to be changed when switching the gain to prevent saturation, so that a 1 V sinusoidal signal was applied in the case of 0 dB gain and a 0.1 V sine wave was used in the case with 20 dB gain.

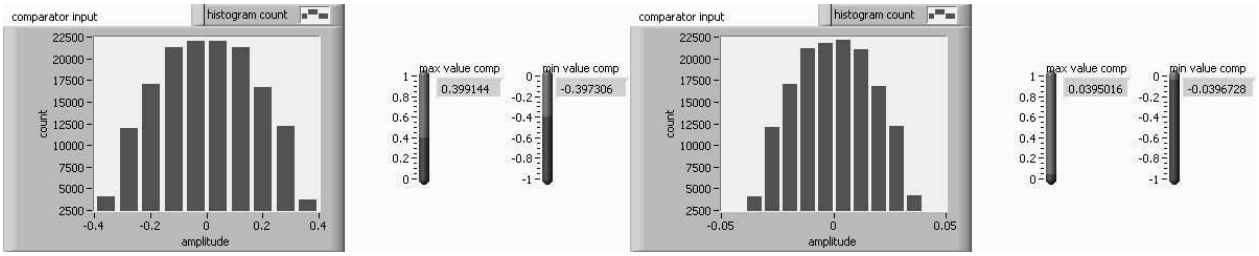

Figure 11: Histogram plots at comparator input; gain = 0 dB (left) , gain = 20 dB (right)

The histograms show that the conditions in (6) and (7) are achieved in both cases. A degrade mode has also been implemented as additional safety measure, that lowers the ADC order to 2 (bypassing the 3rd order integrator). The mode can be activated by the digital control part which monitors the output level.

V. Conclusions

The gain control implemented in this paper has allowed, by eliminating the PGA and ZCD of the audio ADC front-end, a reduction of 25% in current and 30% in area of the uplink path developed for commercial GSM projects.
The switching control logic for the gain setting has been moved out of the mixed signal area with a minimum impact in the digital block complexity.
The silicon (shown in Figure 12), currently in the validation phase, has been realized in a CMOS 040 technology and the ADC core silicon area is 0.073 mm^2.

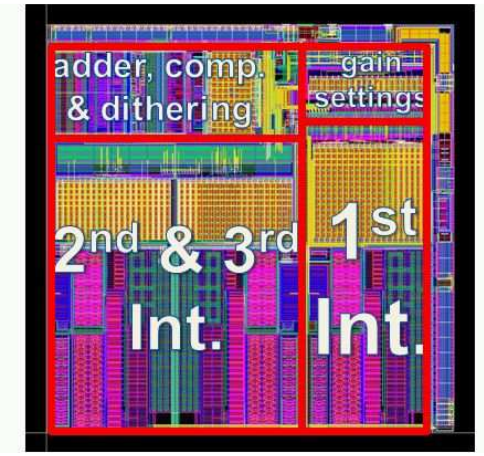

Figure 12: Silicon layout of the ADC core

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