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A continuous-time first order Σ-Δ converter with offset calibration for biological application

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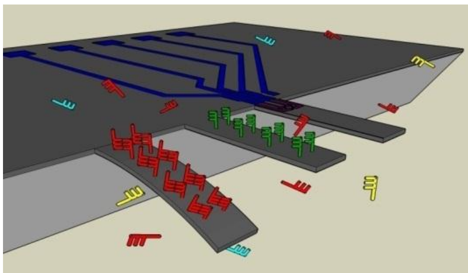
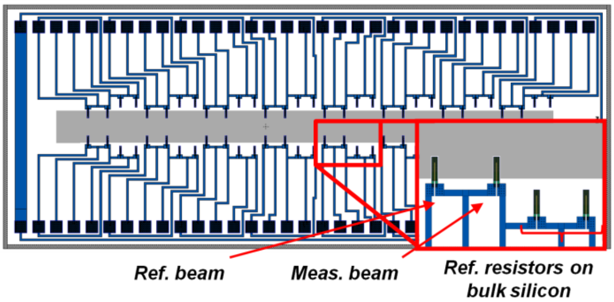
Abstract-In the present paper, a continuous time Σ−Δ converter for biological application is presented. The implemented ASIC has been designed for reading piezo-resistive MEMS cantilever used as DNA detector. The readout channel consists of a first analog front-end circuit able to reduce possible input offset and electronic mismatch, followed by a continuous-time 9b first order Σ−Δ converter for digital conversion. Simulation results show a circuit accuracy on the measurement of resistance variation in the order of 10 ppm within a maximum range of 10%.

I. Introduction

DNA detection is widely used for many applications and in particular can be very useful for monitoring particular diseases thanks to a genomic analysis. In order to make a fast and more practical measurement a Lab-On-Chip (LOC) instrument is desirable for its compactness and portability. LOC devices can be implemented in many ways depending on the type of detectors and readout technique. One of the most used approach for DNA detection is based on optical fluorescence. In this case the DNA is labelled with a fluorescent marker which emits light in appropriate conditions when properly excited. Another interesting method to read the DNA signal is to use cantilever MEMS-based detectors [1]. This label-free approach allows to reduce the complexity of the system, avoiding light source and optical components, and, in the meanwhile, allows to easily extend the number of detections, realizing an array of cantilevers each one devoted to a specific detection. This last feature introduces redundancy or complementary detections improving the robustness of the measurement.
The present work is referred to a readout channel to be connected to an array of piezo-resistive cantilevers for DNA detection. The detector consists of a couple of piezo-resistive cantilevers properly functionalized in order to perform a differential measurement (see figure 1a). In addition to the couple of cantilevers there is another couple of bulk resistances with same nominal value, used in order to implement an integrated Wheatstone bridge (see figure 1b where the whole array is also depicted).



a)



b)

Figure 1: a) Hybridization process on the cantilever DNA detection ; b) detector implementation.

Differently from the frequency based technique, where the cantilever is excited at the resonant frequency and the frequency variation is measured after the deposition of a matter on it, the present cantilever is based on a static measurement because of the low DNA mass. In this technique the hybridization process induces a complex mix of phenomena, ranging from electrical interaction of DNA built-in charge to steric hindrance of probes, resulting in an equivalent differential stress between the top and the bottom surfaces of a cantilever, which in turn results in a deflection of the beam.
Many high resolution readout circuit based on resistive sensors are proposed in literature for different

applications [2-6]. The approach used in [2-3] is based on resistance to period conversion by simply reading the frequency resulting from the charging and discharging capacitor due to the current flowing through the biased detector resistance. Main benefit of the approach in [2] is the immunity to parasitic capacitors placed between the sensor and the ASIC interface. In both works a wide range of input resistance is measurable reaching a best accuracy of 0.5% which is not adequate for the present application. The architectures proposed in [4-5] use a programmable analogue front-end before digital conversion for mismatch and offset calibration with gain correction. The final performance of the readout channel is of about 160dB with a reported accuracy of 0.1% over the entire range of work. Finally best performance are obtained in [6] where a 21 bit analog to digital converter over a ±40mV of range for bridge transducer is presented. The shown architecture is complex and includes three stages current feedback instrumentation amplifiers with chopping technique plus a 21 bit Δ–Σ incremental modulator.
The presented work, similarly to the idea proposed in [4], consists of two stages: a first continuous mode analog interface followed by a digital conversion naturally implemented by a continuous time incremental Σ-Δ modulator. The first stage is used for converting the input voltage difference in a current using programmable circuit in order to adjust the presence of possible offsets and reduce electronic mismatches. This first stage has to be considered essential for the implementation of the system. In fact while cantilever resistance variation due to the DNA hybridization is expected in the order of few ppm, the possible voltage offset, introduced by process variations, can be in the order of few per cent. For these considerations the design of a calibration procedure is needed for correctly readout the input signal.
The paper is organized in the following sections: in section II the measurement method is described, while in section III and IV circuit implementation with some simulation results are shown.

II. Measurement Method

The measurement method used for extracting the resistance variation due to the DNA hybridization is based on three steps:

1) offset and mismatch calibration.
2) first measurement of the calibrated circuit (residual offset before hybridization): M_{off};
3) final measurement of the circuit after hybridization: M_{sig}.

The final value extracted from these measurements is the difference between the values obtained in steps 2) and 3): M_{sig}-M_{off}.
Let's take into account a single detector configured in a Wheatstone bridge where R_{b1} and R_{b2} are bulk resistances and R_{c1} and R_{c2} the cantilever resistances. Moreover let's initially suppose that, being the implanted resistors of a detector very close to each other and being the couple of cantilevers mechanically similar, $R_{b1} \cong R_{b2} \cong R_{c1} \cong R_{c2}$. Under these ideal conditions the value read at the output of the bridge ΔV_{AB} after a hybridization process, causing a $\Delta R_c << R_{c1}$, can be written as:

$$\Delta V_{AB} \cong V_S\left(\frac{\Delta R_c}{R_c + R_b + \Delta R_c}\right) \cong \frac{V_s}{2}\left(\frac{\Delta R_c}{R_c}\right)$$

Then considering a 10 ppm of resistance variation over 10kΩ, supplying the bridge with a V_S=3V, the resulting expected voltage variation ΔV_{AB} is of about 15μV.
Nevertheless the implemented resistances can suffer of changes due to process variations. Moreover the cantilever couple can suffer of mechanical mismatches related to different deflections of the beams detectable also in static condition reflecting in an additional resistance variation of R_{c1} and R_{c2}. In this way each real cantilever resistance R_{c_r} can be expressed as the result of three different contributions:

$$R_{c\_r} = R_{c\_id} \pm R_{c\_p} \pm R_{c\_d} + \Delta R_{c\_sig} = R_{c\_id} \pm \Delta R_{c\_sig} + \Delta R_c'$$

where R_{c_id} is the nominal value of the resistance, R_{c_p} is the contribution related to process variations, R_{c_d} is related to the static deflection, and ΔR_{c_sig} is the signal due the hybridization process. As consequence of the detector non-idealities, the real value of ΔV_{ABr} can be rewritten as:

$$\Delta V_{AB_r} \cong \frac{V_s}{2}\left(\frac{\Delta R_{c_{sig}}}{R_c}\right) \pm \frac{V_s}{2}\left(\frac{\Delta R_c'}{R_c}\right) \pm \frac{V_s}{4}\left(\frac{\Delta R_b'}{R_c}\right) = \Delta V_{AB} \pm V_{off}$$

where ΔR_b' takes into account of the variation also of R_b. This means that in absence of a signal (ΔV_{AB}=0) an equivalent offset V_{off} is present at the output of the bridge. Supposing to have a maximum resistance variation of 10% for R_{c1}, the equivalent maximum offset introduced is about ±150mV supplying the bridge at Vs=3V. At this offset it has to be added also the electronic offset of the readout circuit resulting in a V_{off_final}= V_{off}+V_{off_el}. Because this value is easily three order of magnitude greater than the expected input signal, the readout circuit has to implement a calibration block and a proper calibration procedure for reducing offset and mismatch. Due to the limited resolution of this operation, a first measurement (M_{off}) has to be held taking into account the residual offset of the readout channel in absence of signal, then final measurement (M_{sig}) can be obtained by differencing the value kept before and after the hybridization process. This technique allows to compensate signal drift due to temperature or extremely low frequency voltage variations.

III. Circuit Implementation

The proposed circuit is shown in figure 2 where it is possible to identify four main functional blocks: 1) a first couple of transconductors directly connected to the voltage input, 2) a coarse calibration circuit for reducing bridge and circuit offsets 3) a programmable current mirror for fine tuning the output current 4) an integrator followed by a clocked comparator for the Σ−Δ modulator.
The tranconductor is implemented by a resistor R_A (R_B) at which is applied a fixed voltage drop thanks to a programmable DAC (DAC_1 and DAC_2). The set values V_{DAC_A} and V_{DAC_B} are able to bias both circuits branches in order to assure a proper value of current and that I_A is approximately equal to I_B. This condition will be reached depending on the presence of bridge and circuit offset introduced by Op1-Op4. The goal of this first calibration stage (CAL1) is to roughly correct the presence of these offsets and to determine currents I_A and I_B, biasing the entire circuit. These currents, with obvious linear dependence on V_{DAC}, can be expressed by the following relationships:

$$I_A = \frac{V_{DAC\_A} - V_A}{R_A} \quad ; \quad I_B = \frac{V_{DAC\_B} - V_B}{R_B} \tag{1}$$

Supposing the DAC has a resolution of 1.5mV, the minimum current step available by the coarse calibration circuit is of about 1,5μA. The second calibration block (CAL2) is represented by transistors M3-M6 and DAC_3 and DAC_4. This circuit implements a tuneable current mirror able to slightly change the value of the output current in order to better approximate I_B.

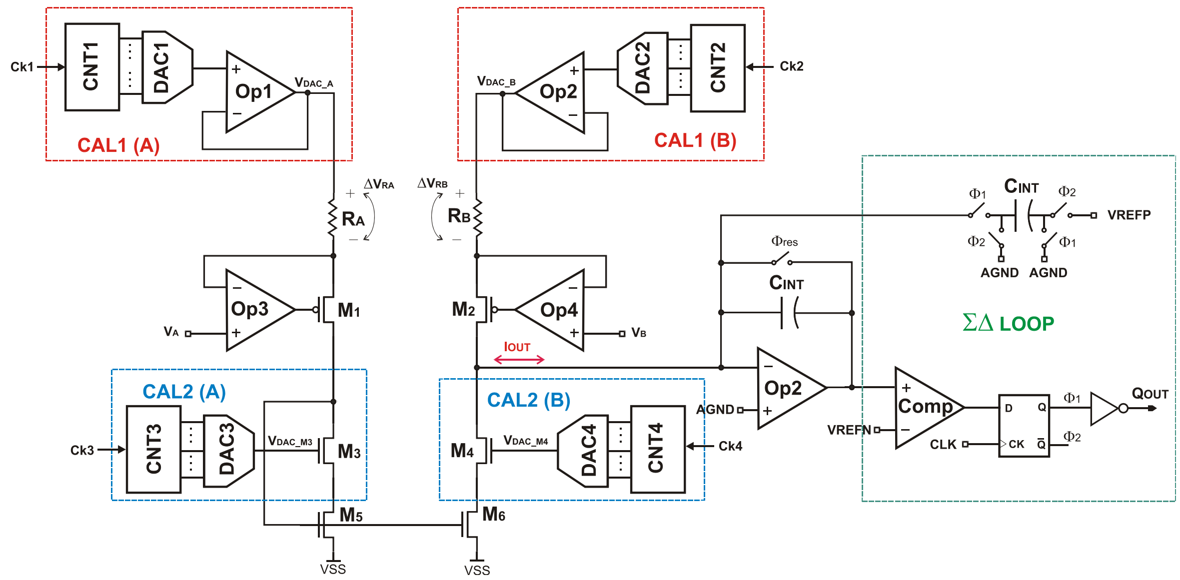


Figure 2: Detailed schematic of the analogue approach.

In this way the main role of fine calibration is to better compensate the input offset coming from the bridge, partially resolved by the coarse calibration, and also to reduce possible electronic mismatch due to the mirror circuit. In particular M3-M6, together with DAC_3 and DAC_4, form a voltage controlled current source circuit. The voltages forced by M3 and M4, induce M5 and M6 to work in triode region, by imposing a certain value of V_{ds}, while their V_{gs} is fixed by the bias current I_A. Acting on DAC_4, the output current of the mirror can be changed, with an approximately linear behaviour, by modulating V_{ds6} following the expression:

$$I'_A = \mu C_{ox} \left(\frac{W}{L}\right)_6 (V_{gs} - V_T) V_{ds6} \tag{2}$$

Supposing DAC_4 has a resolution of 1.6 mV, and using equation (2), the minimum allowed current variation due to the fine calibration is 2 nA when I_A=5 μA which is approximately three order of magnitude lower than the coarse calibration resolution. Considering M5 and M6 in triode region and approximating $V_{ds5}=V_{DAC\_M3}-V_{T3}-V_{DSsat3} \cong V_{DAC\_M3}-V_{T3}$ (same considerations can be applied also for V_{DS6}), the mirrored current (I'_A) can be expressed by the following relationship:

$$I'_A = I_A \frac{(V_{DAC\_M4} - V_{T4})}{(V_{DAC\_M3} - V_{T3})} = I_A k \tag{3}$$

This means that once fixed the value of V_{DAC_M3}, which defines the slope of the current variation, I'_A can be linearly modified as a function of V_{DAC_M4}. Using equations (1), (3) and (4), it is possible to compute the relationship between I_{OUT} and the contribution of each calibration controls as shown in the following approximated equation:

$$I_{OUT} = I_B - I'_A = \frac{(V_{DAC_B} - V_B)}{R_B} - \frac{(V_{DAC_A} - V_A)}{R_A} \cdot \frac{(V_{DAC\_M4} - V_{T4})}{(V_{DAC\_M3} - V_{T3})} \quad (5)$$

An integrator is responsible for the current integration on a capacitor C whose output is connected to a comparator and a synchronous flip-flop for implementing the switch-capacitor control loop for the Σ–Δ modulator. The analog path, from the voltage input to the output capacitor, should introduce a voltage gain of about 10^5 for an integration time of 100ms, meaning that a 10μV of input originates 200mV of output variation in about 20μs of integration time. The theoretical dynamic range can be computed as the ratio between the maximum allowable input voltage (4mV) over the minimum one (2μV), excluding the noise contribution, expressed in dB, resulting about 66dB or equivalently 11b.

IV. Simulation results

From simulations, three different curves are plotted in Figure 5, representing the output of the integrator, after calibration, in the presence of a ΔV_{AB} of 0, 10μV and 500μV respectively. The duration of the simulation is of 100μsec while the master clock of the converter is fixed to 20MHz in order to obtain a 11b conversion. When ΔV_{AB}=0 no output codes are generated because the signal at the end of the integration time is still above the threshold of the comparator (circuit perfectly calibrated). When instead a signal is applied (ΔV_{AB}=10uV) the comparator toggles six times, demonstrating the ability of the circuit to properly discriminate the input variation. Finally (for ΔV_{AB}=500μV) the output code of the last curve is about 910, representing the middle of the range of the converter.

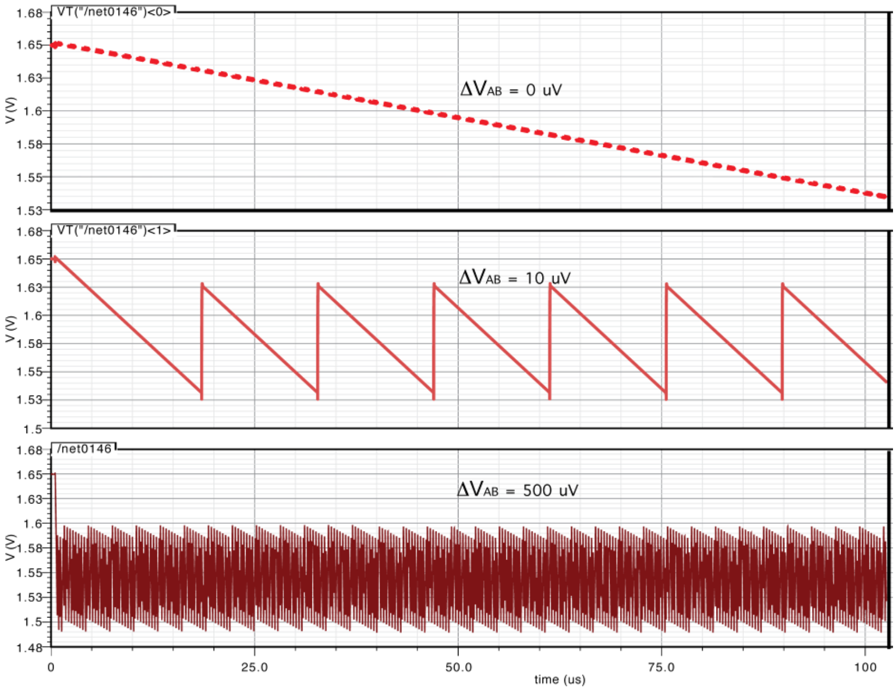


Figure 5: Simulation of the output of the integrator in three different situations: with ΔV_{AB}=0, ΔV_{AB}=10μV and ΔV_{AB}=500μV respectively.

Similar simulations were run by taking into account also offset and noise. In Figure 6 a noise-tran analysis have been executed to find the sensitivity of the whole ADC. Two different input signals have used during the simulations, one with a differential signal of 10μV and one with a signal of 0 considering the same offset in both simulations. The output codes are plotted in Figure 6 depending on the number of the run simulation. As reported above, 6 LSB is the estimation of the SNR with 10μV of input, showing also a noise figure of about 1.5 LSB.

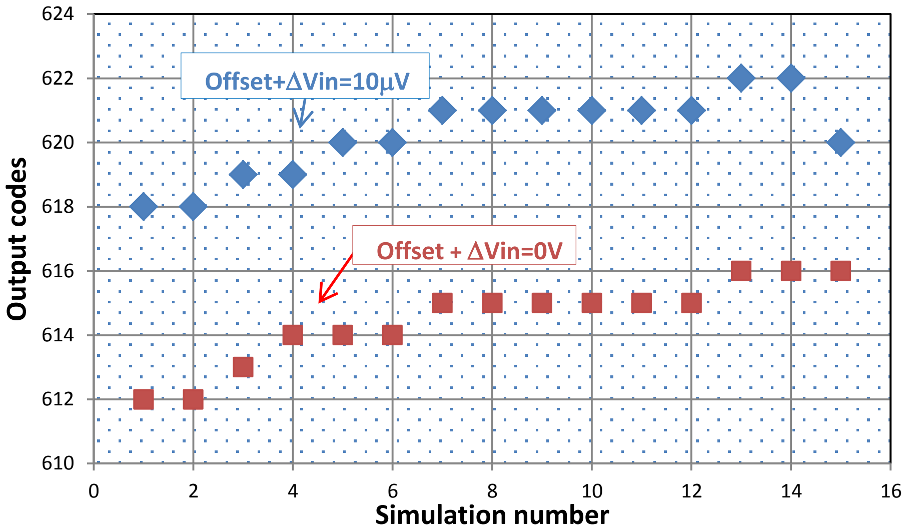


Figure 6: Noise analysis of the output codes of the A/D converter in the presence of offset with a 10µV (blu points) and without signal (red points).

The calibration procedure is described in figure 7 where an external ADC is used in order to properly set V_{DAC_A} and V_{DAC_B}. These DACs are programmed thanks to two integrated counters set to 0 during the reset. The procedure continuously compares V_{DAC_A} (and V_{DAC_B}) with respect to V_A (and V_B) and stops the counter as soon as V_{DAC_A}-V_A is about 3mV. Similar considerations will be done for the other two DACs related to V_{DAC_M3} and V_{DAC_M4} for the programmable current mirror. After fixing V_{DAC_M3} to 1V, V_{DAC_M4} will be swept until the output code is 1. Finally always in figure 7 is plotted the layout of the designed Σ–Δ converter where it is possible to identify the four DACs placed at the edges of the chip, the two resistances placed in the middle of the structure and the integrator and comparator immediately below.

III. Conclusions

As conclusions, a new integrated circuit for high accuracy signal readout designed for DNA detection has been here described. The circuit is characterized to have coarse and fine calibration used in order to overcome the presence of offset due to a no perfectly balanced input bridge or electrical circuit mismatch. Simulation results shows the possibility to reach an accuracy in the order of 10 ppm up to 10% of resistance variation. The expected electrical characteristic of the circuit are then summarized in table 1.

Table1: Main characteristic of the mixed-signal channel.

PARAMETER	VALUE
LSB Coarse Calibration	1.5 mV
LSB Fine Calibration	≅20 µV
Time for a single measure	100 µs
ADC master clock	20MHz
Maximum ROIC Offset Calibration	±1V
SNR @ Vin=10uV	≅ 6 LSB
Output Noise	± 1.5 LSB
LSB @ 5V	5 µV
Estimated Power Consumption	43 mW
Area	0.8 mm^2

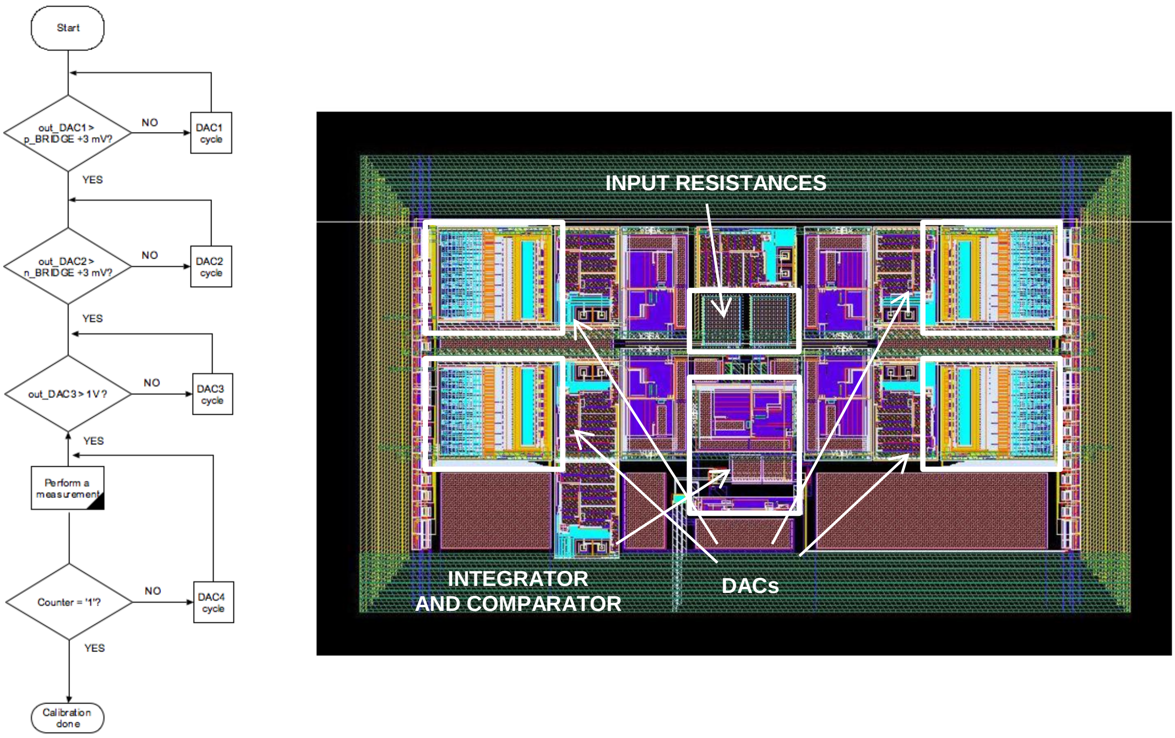


Figure 7: Flow chart of the calibration procedure and layout of the presented ROIC.

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