The New IEEE-Std-1241-2010 for Analog-to-Digital Converters

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Abstract- IEEE Standard 1241-2010 [1] "Terminology and Test Methods for Analog-to-Digital Converters" defines terminology and specifications and describes test methods for measuring the performance of ADC's. The standard is written for manufacturers and users of ADC's for use in both static and dynamic applications. The main purpose of this standard is to ensure that manufactures and users of ADC's have a well-defined set of terms, specifications and test methods so they can understand, describe, and compare the performance of these A/D converters using a common language, with clear definitions. IEEE-Std-1241-2010 was created by the Analog-to-Digital Converter Subcommittee of Technical Committee 10 (TC-10) Waveform Generation, Measurement, and Analysis. TC-10 is part of the IEEE Instrumentation and Measurement Society.

I. Introduction

Work on 1241 originally started soon after TC-10 had finished its development of IEEE-STD-1057-1994 [2] for waveform recorders. It was completed and the first publication of Std-1241 occurred in late spring of 2001 after approval in December 2000. Subsequent to the publishing of 1241-2000 at the request of the IEEE an effort began to create an IEC standard based on 1241-2000. This resulted in the International Standard IEC 60748-4-3 dated August 2006 entitled "Semiconductor devices – Integrated circuits – Part 4-3; Interface integrated circuits – Dynamic criteria for analogue-digital converters (ADC)" which was written to include dynamic criteria for ADC's to complement the previously published IEC standard developed for only static ADC parameters. At the conclusion of the 5 year cycle, the Analog-to-Digital Subcommittee was granted a Project Authorization Request (PAR) by the IEEE Standards organization to develop an updated version of the standard to improve and expand its content. The subcommittee began that work in 2005. An updated version of the ADC Standard, IEEE-Std-1241-2010 was approved in June 2010 and was then published on January 14, 2011.

A. Motivation for the "New" standard

This revision to the original IEEE-STD-1241-2000 was motivated by feedback from users since its publication and the desire of the standard working group to synchronize all TC-10 standards with a common format and as possible, also with synchronized terminology. During the original work, a new term had to be introduced called Signal-to-Non-Harmonic Noise Ration (SNHR). This was necessary so as not to conflict with other standards, until the term Signal-to-Noise Ration (SNR) could be properly re-defined without causing issue. It was also the desire of the working group to add some material related to the different architectures of ADC's that require some modification to the users test plan. This was accomplished through the addition of Annex A "ADC Architectures".

B. ADC usage today

In Figure 1 that shows the real world signal processing path, you can see how the ADC is a basic building block for all communications and process control in today's environment. At the heart of nearly every handheld mobile, appliance and gaming system, ADC's play an integral part in the necessary step to convert real world analog signals to their digital equivalent. This is necessary so the digital engines in use today can react to the ever changing analog world around them and provide a response or feedback mechanism to that change.

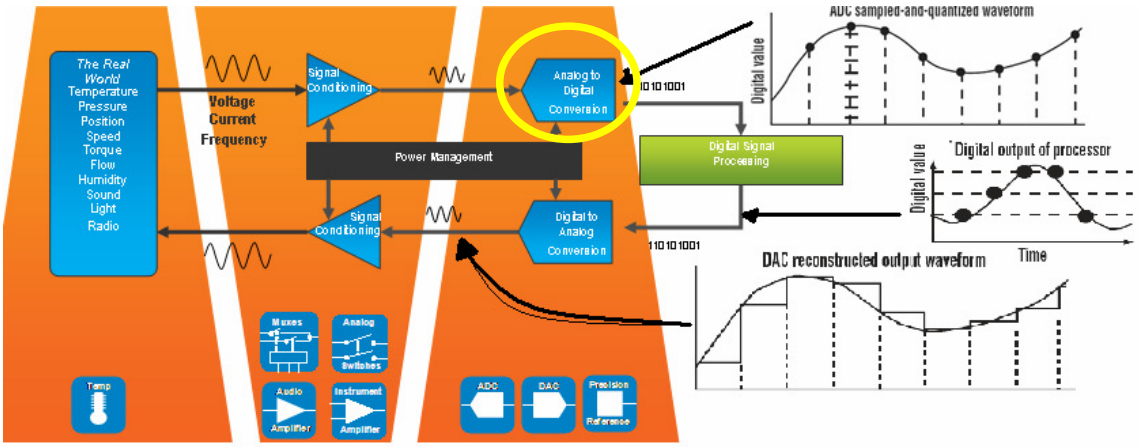

Figure 1 – Real world signal processing sampled data system signal path

It should be noted that the digitizing – signal processing – reconstruction process always adds significant delays. In areas such as telecommunications and instrumentation the delays are usually well bounded. When the ADCs and DACs are inside a fast feedback loop the delay can become intolerable.

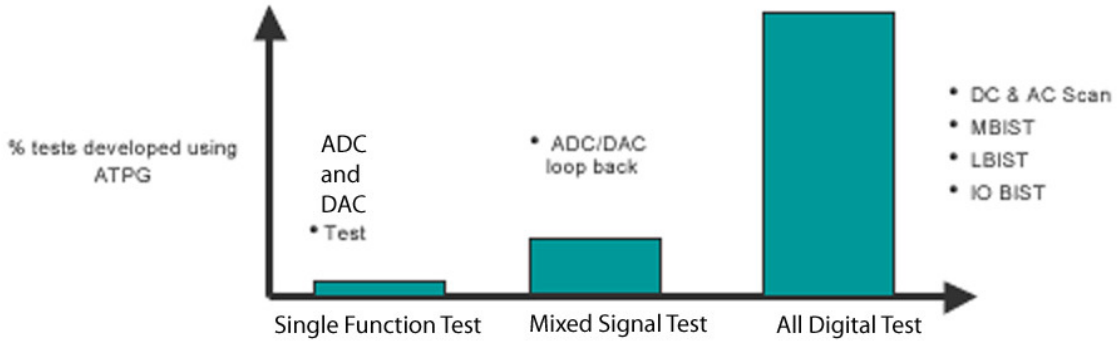

Figure 2 – Data Converter progress towards Automatic Test Program Generation

It has always been the goal of integrated circuit designers that the test program generation that permits the device manufacturers to rapidly create test programs that will fully verify the functionality of a device should be a totally automatic process (ATPG). This process is a very mature one for fully digital integrated circuits (the right column in Figure 2). It is marginally efficient in situations where both an ADC and a DAC are included in the device since some loop back testing can be ATPG generated. The process is almost entirely manual for devices that contain only an ADC or a DAC.

The new standard contains a section that describes ADC architectures, two of which are included below in Figure 3 and Figure 4. This provides a useful method for users of the standard to become aware of developments in ADC designs.

Figure 3 shows one of the early architectures, that of the Dual-slope integrating ADC which was popular early on before the need for speed kept pushing designers to push the envelope with much faster parallel architectures. This dual-slope architecture provided good precision at lower sampling rates and the precision market drove to the current Sigma-Delta ADC architecture prevalent in today's high-resolution field. Successive approximation is still used today up to resolutions of 18-20 bits. The flash converter grew in popularity and evolved into the sub ranging architecture which was followed by variants like the time interleaved and finally the folding and interpolating scheme shown in Figure 4.

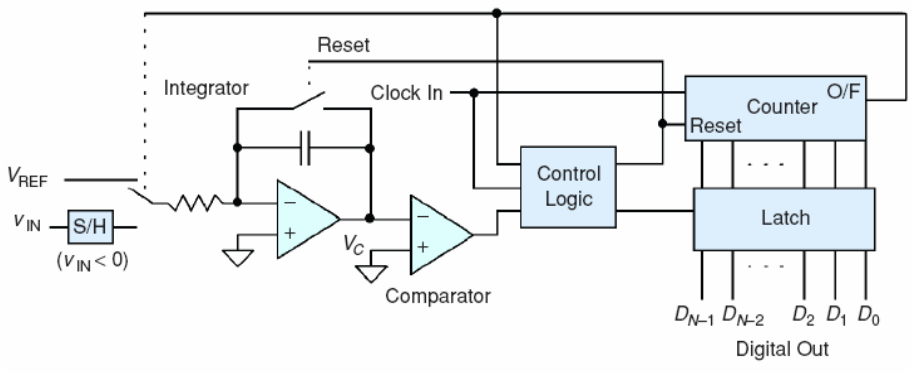

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Figure 3 - Dual slope integrating ADC architecture

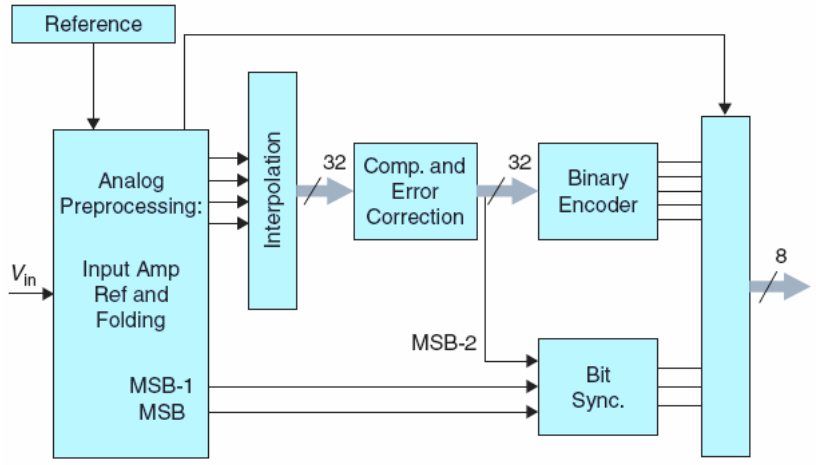

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Figure 4 - Folding and interpolation conversion scheme

Techniques that permit designers to examine data records visually are described in the standard. Figure 5 illustrates a time domain data record that can be transformed into the more understandable waveform shown in Figure 6. In Figure 5, a residual waveform has been collected in 1024 points of data. It includes 7 cycles of the input waveform. This waveform is transformed by an algorithm described in the paper, which permits more detailed examination of the nature of the residual. This is an example of a little bit of magic that has been developed by ADC engineers over the past decades, which permits careful analysis of test results.

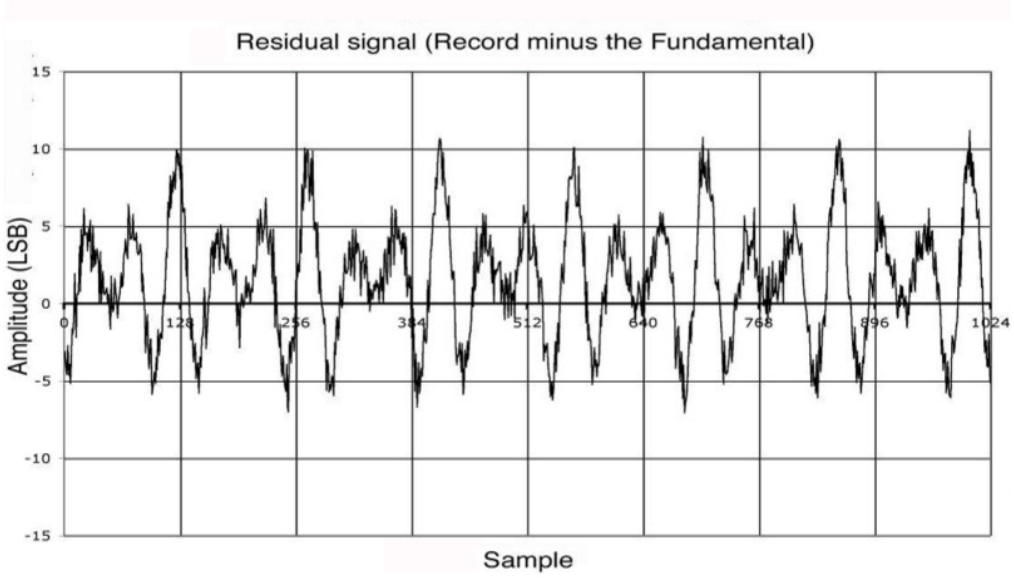

Figure 5 – Plot of Residual Signal

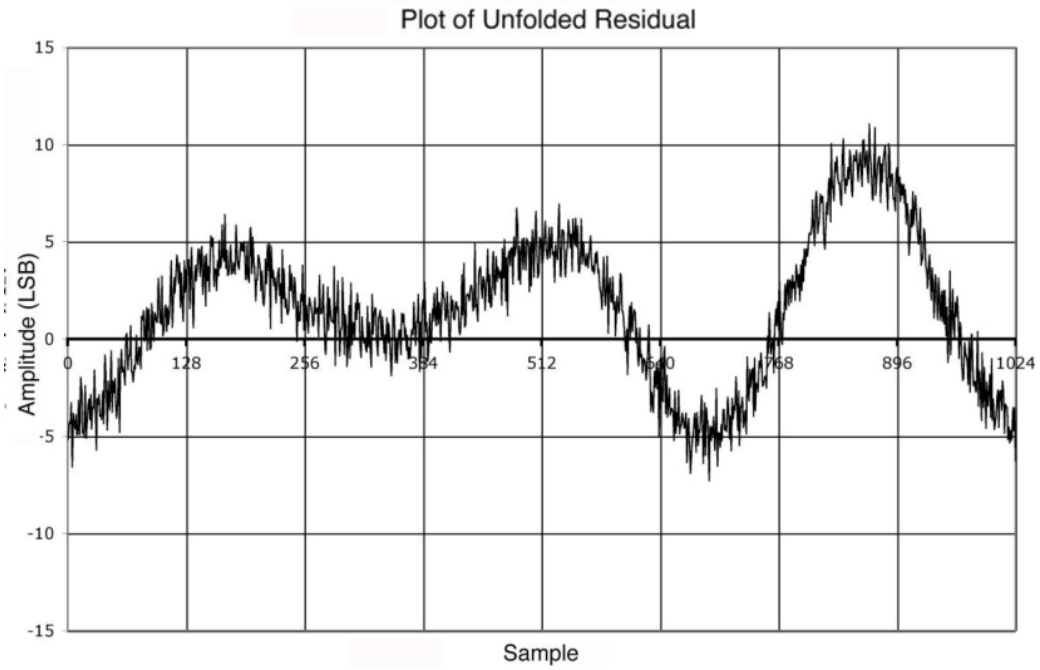

Figure 6, Plot of unfolded residual

An example of some of the other items covered in the ADC standard is a deeper look at hysteresis and alternation – qualities of an ADC which are subtle, but which can affect test results.

It is important to distinguish between real hysteresis, and the effect of transition noise. Hysteresis is present only when the rising and falling transitions differ significantly from the transition noise.

A phenomenon called “alternation” may also be observed. This occurs when a significant range of input voltages results in adjacent ADC output codes being alternately expressed. Alternation is a complementary function to hysteresis since both hysteresis and alternation are unwanted feedbacks to the input from previous output codes. If the feedback is positive then hysteresis is observed. If the feedback is negative then alternation is observed.

To illustrate the phenomenon of hysteresis and alternation, consider the 1-bit ADC shown in Figure 7.

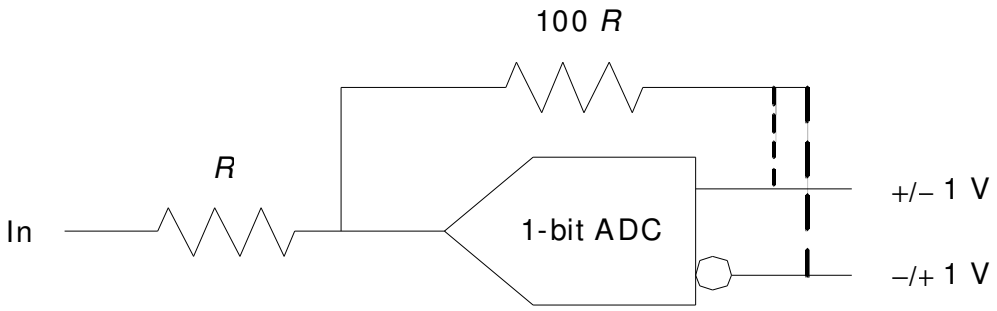

Figure 7—Block diagram to demonstrate hysteresis and alternation

Consider the case when the "True" output is connected to the divider. The input is gradually changed from a negative voltage, which has caused the "True" output to be at the −1 V level. The output of the ADC will go to its high state only after the input voltage has exceeded 10 mV. If the initial voltage had started from a positive value, and then decreased, it would have to go lower than −10 mV to force the output to the low level. This is the phenomenon of hysteresis.

Consider the case when the "False" output is connected to the divider. The input is gradually changed from a negative voltage that has caused the "False" output to be at the +1 V level. The "True" output of the ADC will go to its high state after the input voltage has exceeded −10 mV. From that point onward the output will alternate between the high and low states until the input voltage exceeds +10 mV. If the initial voltage had started from a positive value, and then decreased, the alternation would resume when the input dropped below +10 mV. This is the phenomenon of alternation.

The standard explains the often overlooked concept that ADC linearity can be expresses as either referring to code edges, or mid-riser (the input that will cause 50% of the digital outputs to exceed a specified code and 50% of the observed digital outputs to be less than the specified code) or code centers, mid-tread (the average of the lower code edge and the upper code edge). A graphical model of the two approaches is shown in Figure 7.

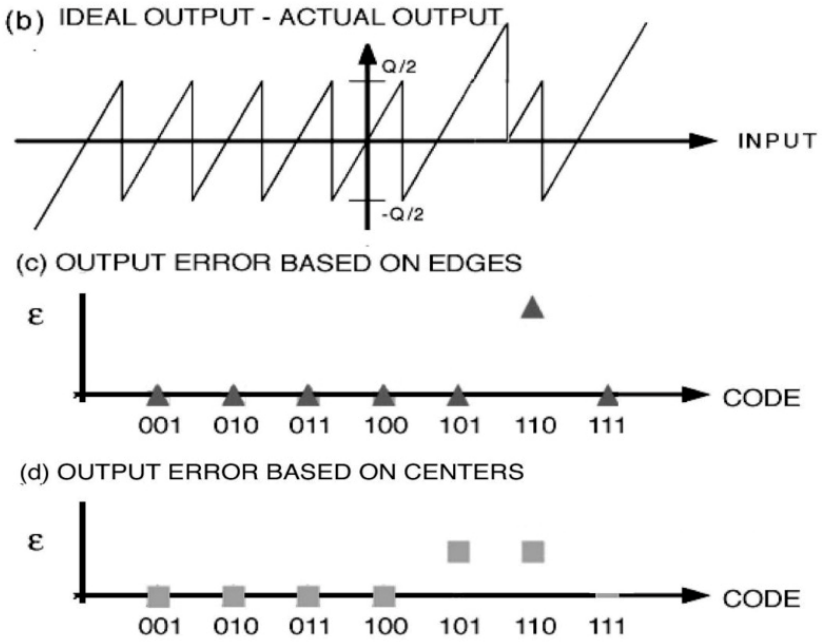

Figure 7 – Errors exhibited by an imperfect 3 bit converter

The standard states that;

There are advantages and disadvantages to both methods of analyzing ADC errors

a) Code center error analysis (mid-tread):
    1) AC analyses such as THD, SINAD, and SNR are better defined by code center error analyses.
    2) For a given converter, INL errors are smaller when based on code centers.
    3) Histogram error analyses are more closely related to code center error analysis.
b) Code edge error analysis (mid-riser):
    1) ADCs that are used for instrumentation are better defined by code edge analysis.
    2) Servo measurement techniques of an ADC transfer function identify code edges.

This kind of discussion of detailed ADC characteristics should help clarify how ADCs are used and tested.

II. Conclusions

Now that Std-1241 has been updated and most terms and test methods are well documented, the next challenge will be how to provide standardization for embedded ADC's. At the 2010 I2MTC conference held in May in Austin, TX USA several IP providers and users held a workshop to discuss how to standardize performance of ADC's in embedded applications. The challenge here is how to obtain advertised performance of embedded IP blocks in user applications when surrounded by hostile SOC environments, not easily obtained due to interference from nearby switching transients and other coupling mechanisms. This will be the next chapter in ADC test collaboration to solve real world problems.

The ADC sub-committee of TC-10 stands ready to accept this challenge and assist industry in solving this problem.

References

[1] IEEE Std 1241™ - 2010, IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters.

[2] IEEE Std 1057™ - 2007, IEEE Standard for Digitizing Waveform Recorders.

[3] Rapuano, S., Daponte, P., Balestrieri, E., De Vito, L., Tilden, S. J., Max, S., and Blair, J., "ADC Parameters and Characteristics," *IEEE Instrumentation & Measurement Magazine,* vol. 8, no. 5, pp.44–54, Dec. 2005.