

The Draft-IEEE-Std-1658-2011 for Digital-to-Analog Converters

Steven J. Tilden¹, Solomon M. Max²

¹ LTX-Credence Corporation, (1355 California Circle, Milpitas, CA 95035 USA, +1.408.635.4851(Ph), +1.408.635.4985(Fax), Steve.Tilden@ltxc.com)

² LTX-Credence Corporation, (825 University Ave, Norwood, MA 02062 USA, +1.781.467.5275(Ph), +1.781.329.6880(Fax), Solomon_Max@ltxc.com)

Abstract- The Draft IEEE Standard 1658-2011 entitled “Terminology and Test Methods for Digital-to-Analog Converters” (DAC’s) defines terminology and specifications and describes test methods for measuring the performance of DAC’s. The standard is written for manufacturers and users of DAC’s for use in both static and dynamic applications. The main purpose of this standard is to ensure that manufactures and users of DAC’s have a well-defined set of terms, specifications and test methods so they can understand, describe, and compare the performance of these D/A converters using a common language, with clear definitions. Draft IEEE-Std-1658-2011 was created by the Digital-to-Analog Converter Subcommittee of Technical Committee 10 (TC-10) Waveform Generation, Measurement, and Analysis. TC-10 is part of the IEEE Instrumentation and Measurement Society. This paper will describe some major sections and highlights of this new draft standard.

I. Introduction

Draft IEEE Standard 1658 was a natural progression following publication of other, similar TC-10 standards. Once the initial standard IEEE-STD-1057 [1] describing waveform recorders was published, TC-10 set about to generate IEEE-STD-1241 [2] which described Analog-to-Digital Converters that were used in waveform recorders, but required different and yet similar terminology and test methods. There was tremendous world-wide interest in these standards and a large international working group was quickly established to start work on P1658.

I.1 Motivation for the standard

Like ADC’s, DAC’s serve an important and ever increasing role in signal processing today. Figure 1 shows us the real world signal processing path pertaining to everything we do today relating to communications and process control. Real world signals are conditioned and transformed into digital data by ADC’s, sent to a processing computer and then adjustments are calculated and sent back to the real world through DAC’s and more signal processing. As in the case of ADC’s, DAC’s had many terms and definitions that were described in numerous ways. The TC-10 working group set about to clear these conflicts through a body of international experts at universities, laboratories and industry with extensive and diverse experience in data converter design, modelling and test.

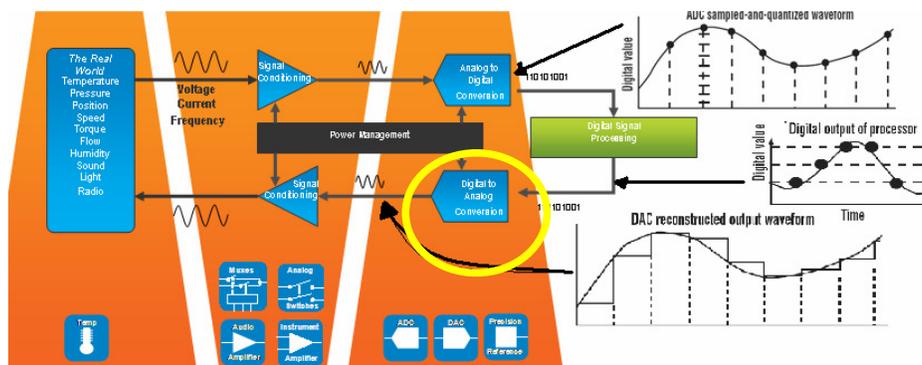


Figure 1 – Real world signal processing sampled data system signal path

In Figure 2 work towards Analog / Mixed-Signal test automation is shown, which is lagging far behind the past couple decades of advances in the digital test domain. Due to this lag, standardization comes from ad-hoc sources of concerned parties rather than mainstream EDA enhancements. For this reason, this standard evolved

out of the needs of industry for direction and methodologies for easy adoption by many differing users.

I.2 Differences in DAC testing

Although many tests performed on DAC's share the same name as ADC tests, they are in many cases quite unique. The differences are noted in the new standard. They include;

DACs and Analog to Digital Converters (ADCs) perform complementary functions. DACs receive a digital signal and generate an analog equivalent, while ADCs receive an analog signal and generate a digital equivalent. Some of the subtleties are summarized below.

- 1) Transfer function differences (See Figure 2)
 - a) For a DAC, each digital input corresponds to single average analog output amplitude.
 - b) For an ADC, each digital output corresponds to an interval of analog input values. The analog quantity defined in the transfer function of an ADC, the code edge, is usually defined to occur at the point where 50% of the output codes are greater than a specified digital output.

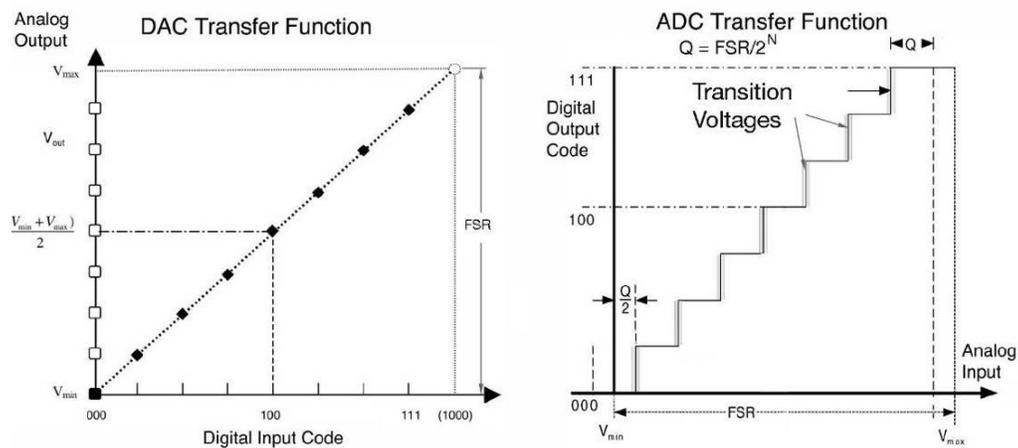


Figure 2 - Transfer functions of ideal 3-bit unipolar DAC and ADC

- 2) Quantization differences
 - a) In a DAC, the input is a digital input code and the output is an analog representation of the input.
 - b) In an ADC the input is analog and the output is the quantized representation of the input.
- 3) Time-domain differences
 - a) A DAC with a constant input code produces a continuous nominally fixed analog output that may contain additive noise.
 - b) An ADC with a constant input may generate a distribution of quantized outputs because of the presence of noise.
- 4) Frequency-domain differences
 - a) A DAC driven by a single-frequency digital sinewave at its input will produce at its output a single frequency between dc and $\frac{1}{2}$ the data rate. Additionally, other frequencies will be produced that are sums and differences of the input frequency and multiples of the data rate.
 - b) An ADC with any fixed frequency analog input will produce a data record that will appear to contain frequencies only up to one half the sampling rate.
- 5) Both a DAC and an ADC require an internal or external reference current or voltage that will cause the DAC to have an output that can be in someway traced to standard units of voltage or current.

There are also some subtle differences between ADCs and DACs in the area of aliasing and image frequency generation. Aliasing is a phenomenon usually associated with ADCs while the generation of image frequencies is usually associated with DACs. The two phenomena are very closely related. In both cases we there is a sampling frequency, f_s . For an ADC this is the clock rate, the rate at which samples are taken. For a DAC this is the data rate, the rate at which data words are supplied to the DAC.

Spurious Free Dynamic Range (SFDR) is another example of the differences between ADCs and DACs.

Spurious free dynamic range is used as a figure of merit for DACs. A tone is synthesized, and the non-fundamental frequency components are measured. The spread between the amplitude of the fundamental and the highest non-fundamental component is defined as the spurious free dynamic range.

There is a difference of opinion in the industry concerning the harmonics of the fundamental. Some argue that any component, even if it is a harmonic, should be counted in the SFDR measurement. Others argue that the harmonics are measured as a part of a total harmonic distortion measurement (THD). The controversy is visible in the following example of an SFDR result:

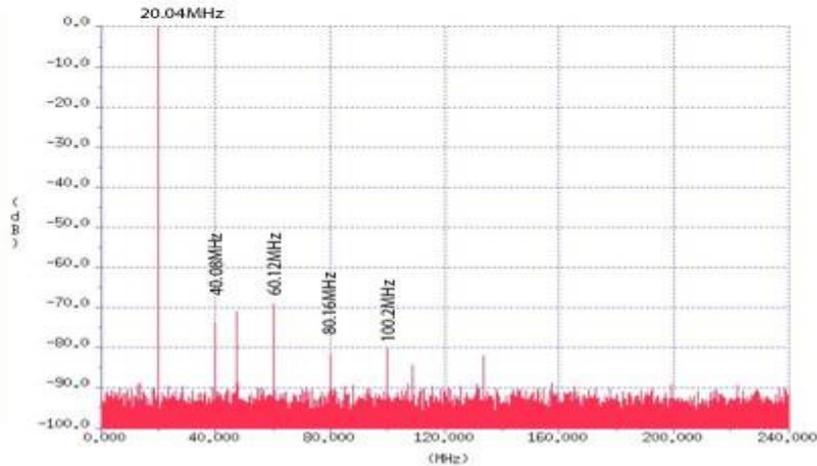


Figure 3 - Plot of DAC SFDR data

Frequency	Response	Comment
20.04 MHz	0 dB	Fundamental
40.08 MHz	-75.0 dB	2 nd Harmonic
47.53 MHz	-71.0 dB	Spur
60.12 MHz	-69.0 dB	3 rd Harmonic
80.16 MHz	-82.0 dB	4 th Harmonic
100.2 MHz	-80.0 dB	5 th Harmonic
108.471 MHz	-84.0 dB	Spur
133.571 MHz	-81.0 dB	Spur

Table 1 – Frequency components seen in typical SFDR plot from Figure 3

If the harmonics are included, the SFDR would be evaluated as 69.0 dB. If the harmonics are not included the SFDR would be 71.0 dB

A typical SFDR plot of that which is presented in data sheets of commercial DACs is illustrated in Figure 4. The DAC update rate is specified as 400 MHz. The frequency of the fundamentals generated were 10MHz, 20MHz, 40MHz, 70MHz, 100MHz, and 120MHz

The amplitudes of the fundamentals were 0dB relative to Full Scale, -3dB relative to Full Scale, and -6dB relative to Full Scale. The measurement sampling frequency and record length are unspecified.

An example of SFDR plots is in Figure 4 for the device DAC5675-EP [3]. About 12 fundamental frequencies were tested at 3 different amplitudes to generate the plot.

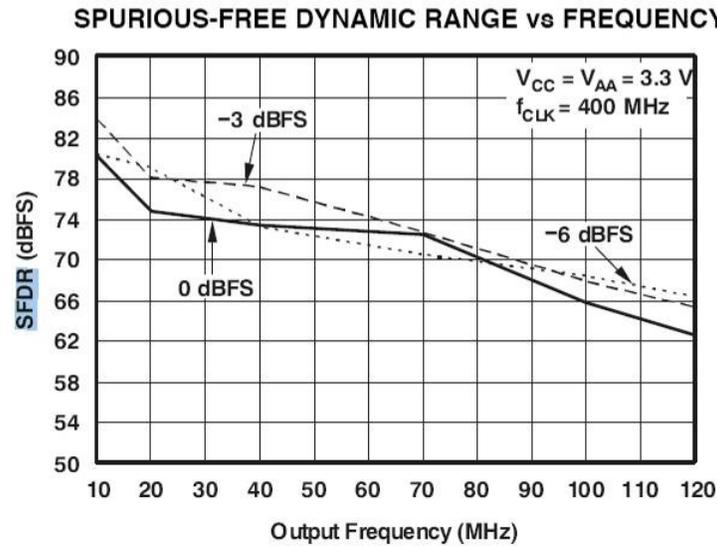


Figure 4 - Example SFDR plots

In previous standards, (IEEE1241 and IEEE1057), SFDR was defined as including harmonics. The two mentioned standards are ADC and digitizer standards. The SFDR in ADCs and digitizers is somewhat different from SFDR in DACs. Each of these devices will be considered separately.

I.3 Differences in ADC Sampling

When an ac signal is applied to an ADC, the spectrum of the digitized output produces frequencies only between the dc and the sampling frequency divided by 2 (the Nyquist bandwidth). The harmonics of the input signal fold-back into this band of frequencies if the harmonics are higher in frequency than half the sampling frequency. This phenomenon allows all high frequency harmonics to show up as spurs. The following table illustrates the effect for the approximate frequencies used in PCM Audio.

Input Frequency	Sampling Frequency	2 nd Harm.	3 rd Harm.	4 th Harm.	5 th Harm	6 th Harm	7 th Harm	8 th Harm	9 th Harm	10 th Harm
1KHz	44KHz	2KHz	3KHz	4KHz	5KHz	6KHz	7KHz	8KHz	9KHz	10KHz
2KHz	44KHz	4KHz	6KHz	8KHz	10KHz	12KHz	14KHz	16KHz	18KHz	20KHz
3KHz	44KHz	6KHz	9KHz	12KHz	15KHz	18KHz	21KHz	20KHz	17KHz	14KHz
5KHz	44KHz	10KHz	15KHz	20KHz	19KHz	14KHz	9KHz	4KHz	1KHz	6KHz
10KHz	44KHz	20KHz	14KHz	4KHz	6KHz	16KHz	18KHz	8KHz	2KHz	12KHz
20KHz	44KHz	4KHz	16KHz	8KHz	12KHz	12KHz	8KHz	16KHz	4KHz	20KHz

Table 2 - ADC Spectra

If a DAC is programmed with a single frequency the possible output spectrum can become quite complex. Consider the case of a PCM audio DAC without a reconstruction filter generating a 1 kHz tone. The following spectrum in Figure 5 will be present if the DAC generates internal harmonics;

Harmonics of the fundamental add spurious tones in the region of the desired pass-band. The harmonic tones in the pass-band are tabulated below. Additional spurious tones appear because of the image frequencies. The image frequencies fall at the same frequencies as the folded-back ADC frequencies.

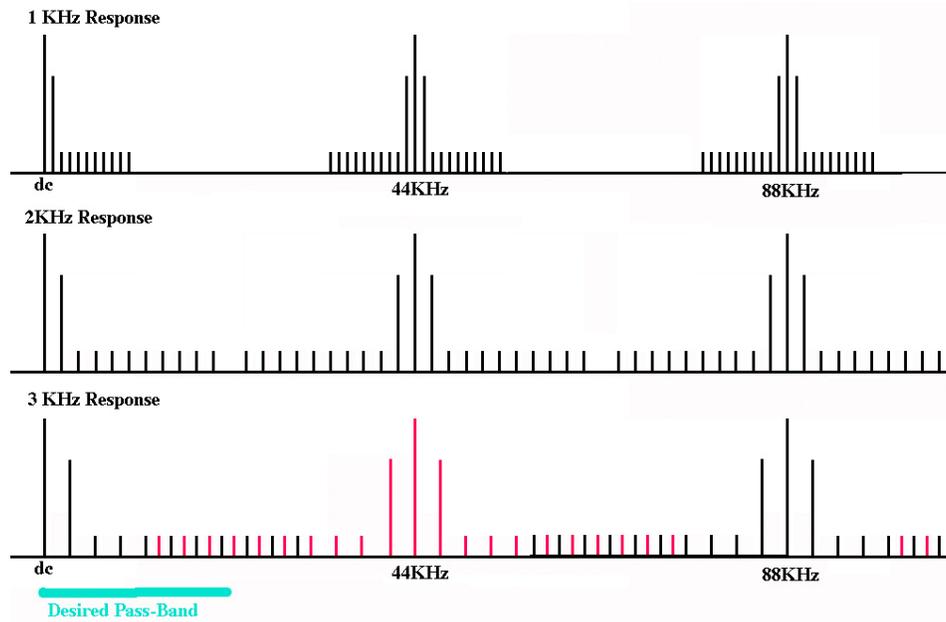


Figure 5 – DAC Spectra

Tone Frequency	Data Rate	2 nd Harm	3 rd Harm	4 th Harm	5 th Harm	6 th Harm	7 th Harm	8 th Harm	9 th Harm	10 th Harm
1KHz	44 KHz	2 KHz	3KHz	4 KHz	5 KHz	6 KHz	7 KHz	8 KHz	9 KHz	10 KHz
2KHz	44 KHz	4 KHz	6 KHz	8 KHz	10 KHz	12 KHz	14 KHz	16 KHz	18 KHz	20 KHz
3KHz	44 KHz	6 KHz	9 KHz	12 KHz	15 KHz	18 KHz	21 KHz	24 KHz	27 KHz	30 KHz
5KHz	44 KHz	10 KHz	15 KHz	20 KHz	25 KHz	30 KHz	35 KHz	40 KHz	45 KHz	50 KHz
10KHz	44 KHz	20 KHz	30 KHz	40 KHz	50 KHz	60 KHz	70 KHz	80 KHz	90 KHz	100 KHz
20KHz	44 KHz	40 KHz	60 KHz	80 KHz	100 KHz	120 KHz	140 KHz	160 KHz	180 KHz	200 KHz

Table 3 – DAC Spectra

The spurious tones appear at frequencies other than the harmonics, although they are caused by the harmonics.

Because DACs can have harmonic frequencies that may not be filtered completely by the reconstruction filter, the standards committee felt that it was appropriate to exclude harmonics from SFDR. The inclusion of the harmonics in SFDR for ADCs will be revisited at the time of the next revision of the ADC and waveform recorder standards.

I.4 Providing for DAC architecture differences

The following Table 4 is from P1658 informative Annex A in the standard, users can find several common architectures, their description, features, variations, advantages and disadvantages. Although not exhaustive, these help the user of the standard decide what tests are important and less important to properly characterize and use each DAC architecture as well as hints to application of same.

As DAC architectures evolved, testing also had to change. For example, early designs had many challenges in producing linear DAC's and testing was laborious and costly. The evolution of test methods progressed in stages, occasionally leap-frogging technology, such as extending performance and dynamic range through hybrid or composite ATE instrumentation architectures.

Section #	Description	Features	Variations	Advantages	Disadvantages
A.1	Binary Weighted	N Resistors N switches	Current sources or capacitors can replace resistors	Simple, Minimum components. Minimal Digital encoding	Difficult to manufacture Not necessarily monotonic
A.2	Resistor String	2N-1 Resistors, 2N Switches	Parallel current sources can replace resistors	Simple, All resistors are identical. Inherently Monotonic	2N Resistors
A.3	Segmented DAC	Tapped potentiometer fed into tapped potentiometer	Current or voltage output	Inherently monotonic. Fewer resistors than resistor string	Resistor matching errors may degrade INL
A.4	R-2R (Ladder)	2N resistors, 2N switches	Equal current sources can drive R-2R ladder	Easy to fabricate, all resistors are similar in value. Constant impedance	Not inherently monotonic. Impedance lower than other DAC architectures
A.5	Sigma-Delta	Input data stream feeds a digital interpolation filter which drives a 1 bit DAC followed by a filter	DAC can be more than 1 bit	High linearity. Easily integrated into standard digital ICs	Low bandwidth Can be noisy May have artifacts such as baseband tones
A.6	Pulse-Width Modulation	Pulse width proportional to input data	Current or voltage pulses	Very low cost Low internal power dissipation	Low bandwidth Nonlinear frequency response

Table 4 – DAC Architectures (from Annex A of P1658)

I.5 Example DAC architecture

Figure 6a & 6b shows a common DAC architecture in use today, the R-2R ladder. As can be seen, this architecture lends itself to either current or voltage steering mode.

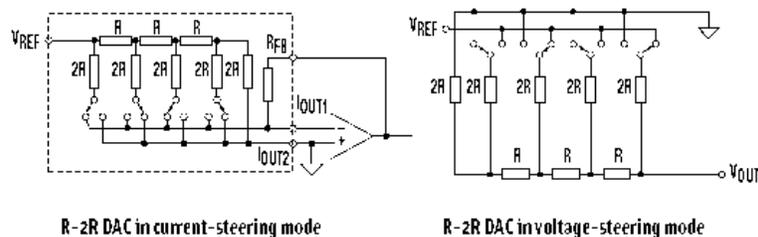


Figure 6(a) – R-2R DAC in voltage mode / (b) – R-2R DAC in current mode [4]

II. Conclusions

The TC-10 DAC working group expects that Draft IEEE Standard 1658-2011 will proceed through the balloting process and be approved by the IEEE RevCom committee this year. Publication will occur a few months after approval once final IEEE editing has been completed and then will be available from the IEEE on-line [Standards Portal](#).

References

- [1] IEEE Std 1057™ - 2007, IEEE Standard for Digitizing Waveform Recorders.
- [2] IEEE Std 1241™ - 2010, IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters.
- [3] DAC5675-EP product data sheet, Texas Instruments Inc.
- [4] Morrison, D. G., „Basic of digital to analog converters design“, Supplement to Electronic Design, November 10, 2003.