Flash Caliper Subranging Architecture

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Abstract – The paper presents a subranging version of an already presented architecture based on a electrical transfer of the well known technique used to improve the accuracy of length measurements, namely the "nonio". The particular feature of this last architecture is that greatly reduces the requested voltage reference levels that are necessary for the whole conversion. This in turn reduces the number of the requested resistors which, in an integrated realization, must have a great area to reduce the dispersion of the resistor values due to the alignment errors of the masks. Unfortunately this technique not reduces the number of the requested comparators. The subranging structure, widely used to reduce the number of comparators in the flash ADC architectures, is here adopted to reduce the number of comparators and implemented without performing the folding of the input signal to be converted. This last common practice is here avoided and replaced by an use of a mobile voltage reference scale of the some kind of the mobile scale requested by the electrical nonio implementation. The result is a very compact architecture.

I. Introduction

It is well known that the flash converter is the simplest and the fastest among the possible architectures of A/D converters. It requires a set of voltage reference levels and a an array of comparators, which sample the analogue input simultaneously. Each quantization level requires a comparator. So an N-bit flash converter requires an array of 2^N comparators. This means that an increase of one bit of the requested wordlength implies that the number of comparators is doubled in the architecture of the converter. This fact represents the drawback of this implementation from the point of view of the complexity of the architecture and the related power dissipation. To overcome this inconvenience, the architecture of the two stage (subranging) flash converter was proposed. A first stage determines the most significant bits of the output; a second stage, driven by the first one, determines the less significant bits of the requested wordlength. In this way the complexity, mainly for large wordlengths, is conveniently reduced and the number of requested comparators is drastically diminished. However, the related conversion speed is reduced of a factor of about two. Following this possibility of hardware reduction, this work presents an architecture of a two stage flash converter obtained by a cascade of two caliper converters. So a new architecture is realized which presents some interesting features.

II. Brief remember of caliper ADCs

Caliper ADCs were firstly introduced by one of present authors [1,2,3]. The main purpose of these architectures is the reduced number of voltage reference levels. This, when the voltage reference thermometric scale is realized by a resistive voltage partition, greatly reduces the number of requested resistors. This in turn reduces the linearity problems and, in an integrated realization, reduces the dispersion of the resistors values due to its reduced distance inside the chip.

The basic concept of caliper ADCs is that the voltage reference levels are obtained using an electrical version of the "nonio", i.e. a combination of two scales of voltage levels: a fixed scale and a mobile scale driven by the input voltage to be converted. This mobile scale is driven by the second op-amp of the sample&hold circuit.

A simple example of caliper ADC using this electrical nonio is shown in figure 1. This example regards an ADC having 16 "virtual" reference levels obtained by a comparison between 8 levels of the fixed scale and 4 levels of the mobile one, following the general rule of these architectures. This general rule [3] states that 2^N "virtual" levels can be obtained from a fixed scale having $2^{\frac{N}{2}+1}$ effective levels and a mobile scale having $2^{\frac{N}{2}}$ effective levels. So 2^N reference levels are generated by $3 \cdot 2^{\frac{N}{2}}$ effective levels. This means that an 8-bit (256 levels) converter can be realized using only 48 effective levels and a 16-bit converter (65536 levels) can be realized by 768 effective levels. In the example of caliper ADC architecture of figure 1, a set of 16 comparators realizes a thermometric output scale which can be converted in 4 binary bits.
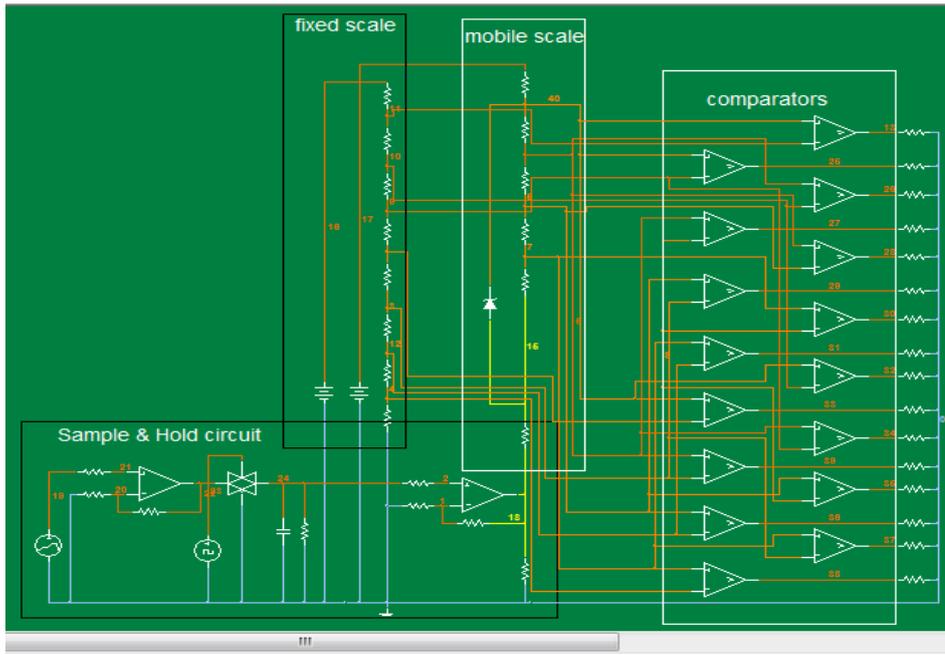
Figure 1.- Simple stage of caliper ADC: the rectangles evidenziate the sample&hold circuit, the two scales fixed and mobile respectively and the comparators and the related connections which realize the virtual levels.

III. Proposed architecture

Here a subranging architecture is presented that greatly reduces, as in the traditional architectures of this kind, the requested number of comparators. We compose in a whole architecture two stages of caliper ADC exploiting in the greatest way the features of these structures. In this architecture the "folding" of the input voltage, requested in this subranging architectures, is avoided and replaced by an equivalent operation performed on the voltage reference. The "fixed" scale of the second stage becomes a step by step "mobile" scale driven by the first stage: the first stage select a proper voltage as reference level of this second "fixed" scale. This reference voltage corresponds to the voltage already converted by the first stage but is here obtained by a resistive partition of an external main voltage reference. This said selection of the reference voltage for the second stage is obtained by a set of switches connected to the every node of the chain of series resistors. These switches are controlled in such a way that each active comparator closes a switch and, contemporaneously, opens the preceding one. In this way no manipulations of the input voltage to be converted are needed and the same input voltage, given by the second op-amp of the sample&hold (SH) circuit, is used for the comparison with the reference levels. The two stages of the subranging architecture are connected in analogue way so the whole structure can perform a conversion using only one clock cycle. The result is a very compact structure.

An example of these proposed caliper subranging architectures is shown in figure 2. In this figure a 256 virtual levels flash subranging ADC is depicted. In this example the floating "fixed" scale of the second stage is obtained using an op-amp which drive the bottom reference voltage and the scale is hunged up to a bias voltage and regulated by a zener diode.

The output of this structure given from a SPICE simulation when the input voltage is a ramp is shown in figure 3.

IV. Brief discussion of the features of the proposed architecture

A concrete discussion of the properties of the proposed architecture requires a realization using a proper integrated technology. Here this realization is not present, so we can discuss only from a theoretical point of view. The proposed architecture takes advantage of the two techniques employed: the electrical nonio and the subranging arrangement. These advantages become very important when large word length structures are realized. In this last case, since the determination of the least significant bits implies a comparison among very small voltage levels, all the available architectures become critical. The proposed architecture, in particular, present some solutions which can induce suspicions. Some of these solutions are here briefly dicussed.

The first, which regard the employment of the nonio: the reduction of the number of resistors is an advantage with regard to the accuracy of the conversion? The answer was already given in a preceding paper [4]: this

reduction is a very important advantage in a integrated realization, as already mentioned above in this paper. In a discrete realization, the resistors used for the voltage partition must have very small tolerances since the reduction of the number of resistors reduces the possibility of compensations among the resistor values variations.

The second is the subranging arrangement: here the transfer of the remaining voltage, to be converted by the second stage, from the first stage to the second one is the most critical step. From a theoretical point of view, the elimination of the input voltage folding would be an advantage. However, here a similar operation is performed over the reference voltage using switches and one operational amplifier (op-amp). This last one induces suspicion because it can introduce an offset voltage. Nevertheless here this op-amp is used as a buffer, giving only amplification of current, so the output voltage should be maintained equal to the input by the negative feedback. The same observation can be regard the op-amp which drives the mobile scales following the input voltage. On the other hand this last op-amp is the second of the SH circuit and is present in all the available architectures. In this present architecture should furnish a major amount of current, so must be chosen in a proper way.

The mobile scales are controlled by zener diodes. A variation of the input voltage induces a variation of the current flowing in the zener diode and, as a consequence, a variation of the zener voltage. A proper choice of this last component can reduce this already small variation.

This brief discussion means that this type of structure would be useful if carefully designed in a technological environment. Here is simply proposed and briefly described.
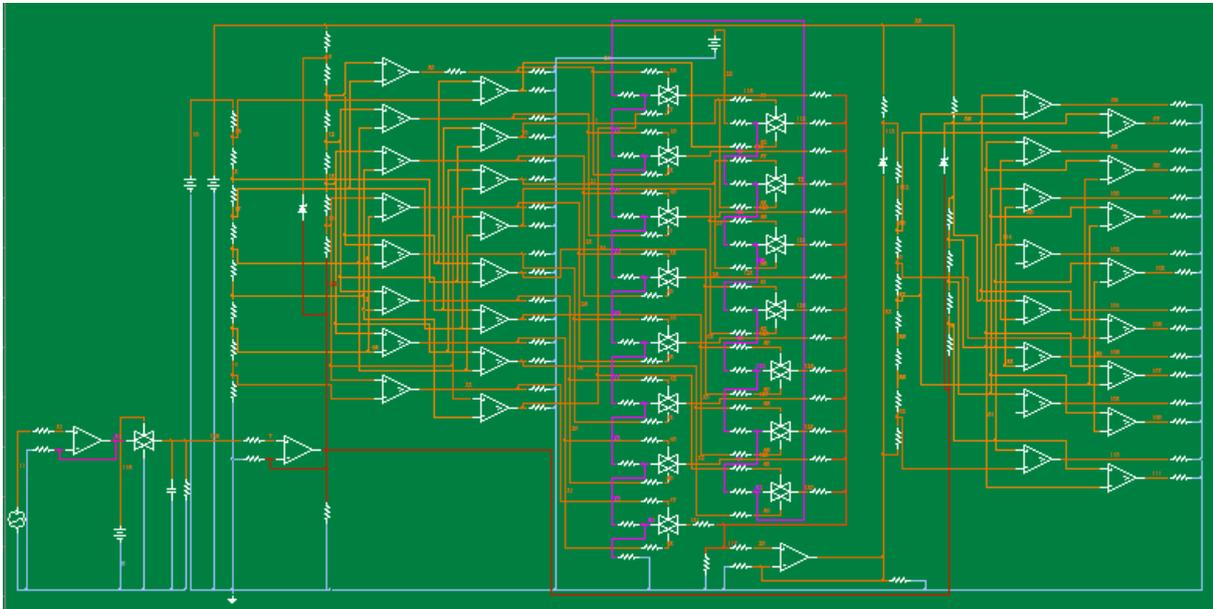

Figure 2. Scheme of the proposed architecture in the case of 256 "virtual" levels [8(fixed)+8("fixed") effective levels + 8(4+4) mobile levels, 16 "offset" levels and 32 comparators]. On the left hand side of the figure the first stage and on right hand part of the figure the second stage. In the middle the set of switches for the selection of the suitable reference voltages of the second stage.

V. Conclusions

A compact structure of flash ADC, obtained by a combination of two interesting architectural solutions, namely the subranging arrangement and the caliper comparison with a voltage reference scale, was proposed. An example of circuital realization is given and a performed simulation by SPICE confirm the rightness of the architectural proposal. The properties of the resulting architecture have been illustrated and the critical points of a possible implementation were focused. This presented work shows that the proposed architecture is valid and that it is reasonable to attempt a realization by a suitable integrated technology.
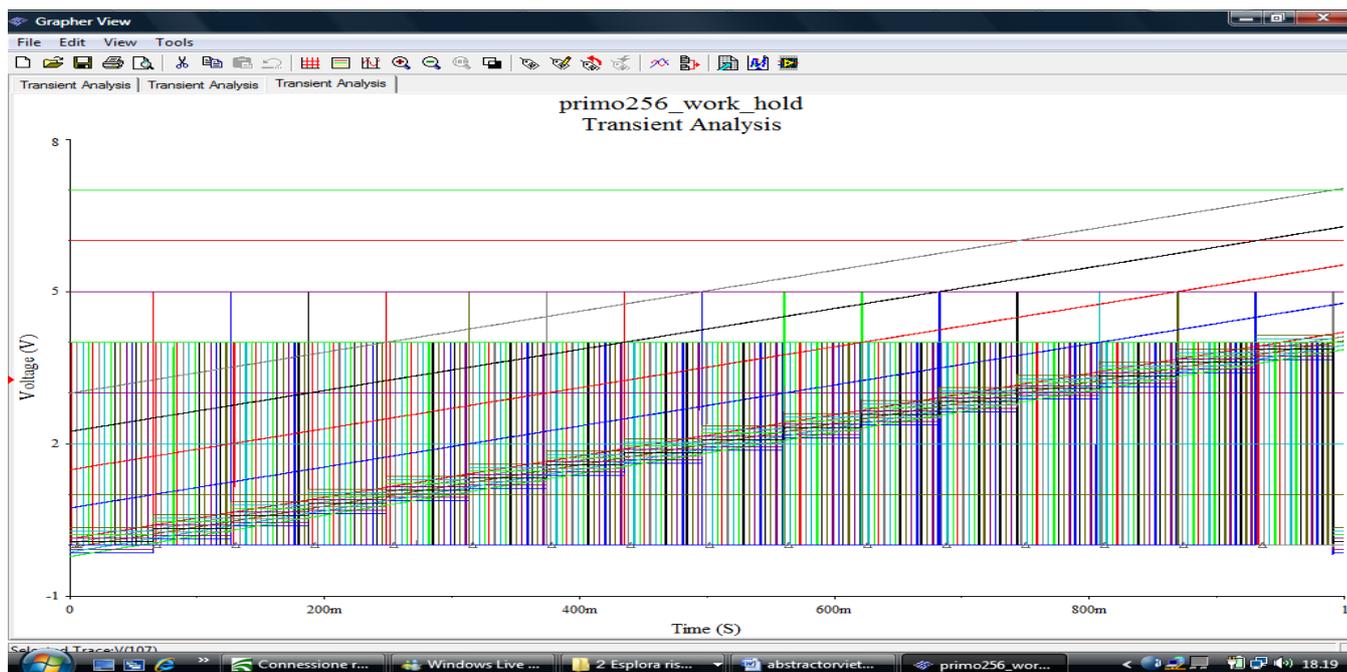
Figure. 3 The output of the example of the proposed converter when the input is a voltage ramp: the ascending lines are the levels of the mobile scales; the staircases are the voltages of the floating "fixed" scale of the second stage driven by the first one; the comparators of the first stage give 5 V when active and the comparators of the second stage give 4 V.

References

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