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Effect of the Resonator Settling Behaviour on SC Band-Pass ΣΔ Modulator Performance and Carrier Frequency Error Measurement

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Abstract- The impact of the settling behaviour of operational amplifiers (op-amps) used to implement switched-capacitor resonators on band-pass sigma-delta (BPΣΔ) modulator performance is investigated. Behavioural simulations of a second-order BPΣΔ modulator are performed by means of numerical models which allow the designer to well-describe high-order dynamics occurring in real op-amp circuit implementations. The results show that high-order poles and zeros in the resonator frequency response affect significantly the overall BPΣΔ modulator performances. In the paper, the effects of the resonator settling behaviour on the dynamic parameters and the carrier frequency error measurement for a Single Quantizer Loop (SQL) BPΣΔ Analog to Digital Converter architecture are also investigated.

I. Introduction

Over the last few years, software radio architectures have driven more and more functions of complex radio systems to be implemented in software. The current research trend is addressed to perform the digital conversions of the incoming signal right to the antenna of the radio system. The typical software radio architecture is constituted by three main functional sections: (i) the Radio Frequency (RF) section; (ii) the Intermediate Frequency (IF) section, and (iii) the base-band signal processing section. In the IF section, realised by the cascade of the Analog to Digital Converter (ADC) and the Digital Down Converter (DDC), the band-limited incoming signal centred at the IF is digitalized by the ADC and demodulated by software techniques [1]-[2]. ADCs based on band-pass sigma-delta (BPΣΔ) modulators employing switched-capacitor (SC) resonators are widely used to this aim [3]-[9].

Different SC resonator topology implementations are actually possible [6]-[7]. The double-delay resonator scheme is one of the most employed for implementing high-performance BPΣΔ modulator. It can be realised by employing two operational amplifiers (op-amps) [4], [8], or only one [3],[5],[9]-[11]. As in conventional SC low-pass (LP) ΣΔ modulator, due to the architecture complexity early-design specifications for SC BPΣΔ modulator building blocks are typically fixed by means of behavioural simulations. Instead, time-consuming transistor-level simulations are usually performed only at the end of the design flow to verify the correctness of circuit building blocks operation before the realisation in an integrated circuits technology. One of the most critical BPΣΔ modulator blocks is the resonator, whose performance depends mainly on parameters of the op-amp used to implement it. In particular, the settling behaviour of the integrator in SC LPΣΔ modulator or the resonator in SC BPΣΔ modulator plays a key role in determining the overall modulator characteristics. It causes the incomplete charge transfer during each clock phase and it depends on high-order poles and zeros in the integrator/resonator frequency response and to other nonidealities characterising the op-amp such as the finite dc gain, bandwidth (BW), slew-rate (SR) and output swing. These poles and zeros are introduced in the integrator/resonator frequency response by the op-amp open-loop transfer function [12], [13], the external feedback network [14], [15] and finite resistances associated to transistors used as switches [16].

In conventional BPΣΔ modulator behavioural simulations, the very simple single-pole model is used to describe the resonator output time evolution during the integration phase, aiming at determining the op-amp gain-bandwidth (GBW) product, and SR values needed to reach the desired modulator performances [5], [16]. As the matter of fact, as occurring in conventional SC LPΣΔ modulator [17]-[21], the real resonator time response is characterised by oscillations and undershoots/overshoots which can strongly affect the system settling time and the BPΣΔ modulator performance. In this scenario, single-pole model [5], [13] can turn out to be actually inadequate to predict resonator output evolution and, most of all, to properly fix SC BPΣΔ modulator building block parameters. Thus, the advantages of the behavioural analysis in making the modulator design more affordable and efficient may be almost completely wasted, forcing the designer to perform blind and time-consuming trial-and-error building block parameter adjustments in the transistor-level design phase.

The paper aims to develop a careful design strategy for SC BPΣΔ modulators since the early-design behavioural simulation phase. Therefore, the impact of the settling dynamics of resonators on the modulator performance is investigated. A high-order settling

model of the resonator is exploited in order to well-predict the combined effect of the op-amp GBW, SR and phase margin on the BPΣΔ modulator distortion and noise. In the circuit practice, this help the designer identify well-founded design guidelines to fix suitably important transistor-level parameters of the resonator, such as bias currents, transistor dimensions and frequency compensation elements of the used op-amp. Moreover, numerical simulations are carried out to investigate on the effects of high-order resonator dynamical model on dynamic parameters and carrier frequency error measurement [22], [23] for a Single Quantizer Loop (SQL) BPΣΔ ADC.

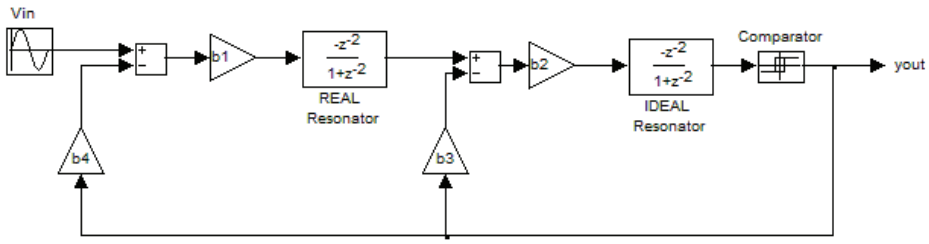

Figure 1. SIMULINK model of second order BPΣΔ modulator.

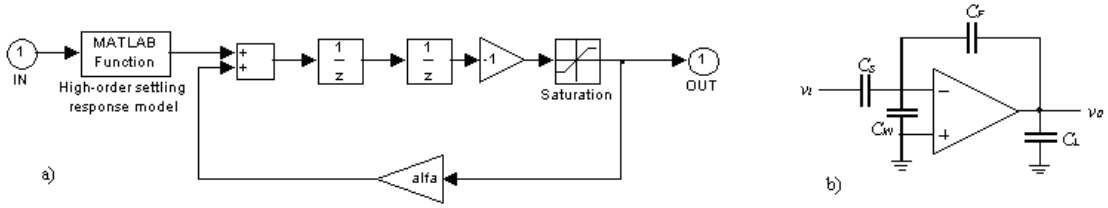

Figure 2. Real resonator: a) SIMULINK model, b) circuit model during the charge-transfer phase.

II. SC resonator main nonidealities effects on BPΣΔ modulators

The effects of the main nonidealities of real SC resonators on the performance of a second-order (fourth-order loop) BPΣΔ modulator, Fig. 1, are analysed in this section by means of behavioural simulations. In particular, the impact of the settling dynamics of the resonators on the Signal-to-Noise-and-Distortion (SNDR) ratio of the modulator is investigated. Without loss of generality, only the nonidealities for the first resonator are actually considered in the model of Fig. 1, since both the second resonator and the comparator can be reasonably assumed as ideal blocks owing to the noise shaping action [17], [20].

To this aim, the SIMULINK model in Fig. 2a is used to simulate the settling behaviour of a real double-delay resonator implemented in an integrated circuits technology. In order to describe it, let us consider the circuit of Fig. 2b which well models the SC resonators operation during a charge-transfer phase in a real ΣΔ modulator. C_S and C_{IN} are the sampling and the op-amp input parasitic capacitances, respectively. C_F is the integration capacitance, and C_L is the equivalent lumped load capacitance at the amplifier output. Similarly to the model in [5], the proposed one allows the designer to estimate the effect of the finite dc gain and output saturation level of the resonator, and the op-amp finite GBW and SR on the modulator SNDR. The finite resonator dc gain is mainly caused by the finite open-loop dc gain, namely A_0, and is modelled by the gain block $\alpha = A_0 C_F / (C_S + C_{IN} + A_0 C_F)$. The output saturation level is determined by the op-amp saturation voltage levels and is modelled by the saturation block inside the resonator feedback loop. However, differently from single-pole classical approaches [5], the MATLAB function of the model of Fig. 2a allows the effects of further poles/zeros in the resonator close-loop frequency response to be also investigated since the modulator behavioural simulation phase. The following aspects of real SC resonators are taken into account:

1) The open-loop frequency response of many real op-amp used to implement the resonator is well-described by two-pole transfer function. By considering $f = C_F / (C_S + C_{IN} + C_F)$ and $GBW = f \cdot UGF$ the feedback factor and the loop-gain unity frequency, respectively, UGF being the op-amp open-loop unity-gain frequency (in Hz), the two following parameters, damping factor $\zeta = \frac{1}{2}\sqrt{\frac{\tan(PM)}{f}}$ (PM is the op-amp phase margin) and natural frequency $\omega_n = 4\pi \cdot GBW \cdot \zeta$ can be carried out [21], [24];
2) At the beginning of the charge-transfer phase, due to the feed-forward signal path from the input to the output node introduced by the feedback capacitance C_F (Fig. 2b), the charge conservation law forces the output node v_0 to experience a change in the opposite direction with respect to the final waited value at the end of the charge-transfer phase [14], [15], [20].

Denoted by t_S the clock period, on the basis of the value for ζ, the evolution of the output node $v_0(t)$ (for $0 \le t \le t_S/2$) of the circuit in Fig. 2b during the *n-th* charge-transfer phase is well-predicted by following expression if no op-amp slew rate limitation occurs [21]:

$$v_o(t) = v_{o,LIN}(t) = v_o(nt_S - t_S) + \begin{cases} \alpha G_0 V_{IS}\left[1 - K\dfrac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}}\sin\left(\omega_n\sqrt{1-\zeta^2}\,t + \tan^{-1}\left(\dfrac{\sqrt{1-\zeta^2}}{\zeta}\right)\right)\right] & \zeta < 1 \\ \alpha G_0 V_{IS}\left[1 - K(1+\omega_{P1}t)e^{-\omega_{P1}t}\right] & \zeta = 1 \\ \alpha G_0 V_{IS}\left[1 - K\left(\dfrac{\omega_{P2}}{\omega_{P2}-\omega_{P1}}e^{-\omega_{P1}t} + \dfrac{\omega_{P1}}{\omega_{P1}-\omega_{P2}}e^{-\omega_{P2}t}\right)\right] & \zeta > 1 \end{cases} \quad (1)$$

where $G_0 = C_S / C_F$ is the integrator gain, $V_{IS} = v_i(nt_S - t_S/2)$ is the step amplitude in input to the op-amp, $K = 1 + C_F{}^2/[C_L(C_S + C_{IN} + C_F) + C_F(C_S + C_{IN})]$, and $\omega_{P1,2} = \omega_n(\zeta \pm \sqrt{\zeta^2 - 1})$. In general, the slope of the curve (1) is less than the op-amp SR only for $0 < t < t_1$ and $t_1 < t_S/2$. Starting from the point $(t_1, v_0(t_1))$, $v_0(t)$ is modelled by straight line of slope SR (the op-amp is in slewing) which ensures the continuity of both $v_0(t)$ and its derivative at $t = t_1$, until the slewing period ends at $t = t_{LS}$:

$$v_0(t) = v_{0,LIN}(t_1) + SR_0(t - t_1) \qquad t_1 < t \le t_{LS} \quad (2)$$

where $SR_0 = SR \cdot sign(\alpha G_0 V_{IS})$. After $t = t_{LS}$, the resonator dynamics is determined again by a linear response (namely $v_{SS}(t) = \dfrac{V_{SS}}{V_{IS}} v_{0,LIN}(t)$, where $V_{SS} = SR \cdot V_{IS} / \max[sign(\alpha G_0 V_{IS}) \cdot \dfrac{dy_{lin}(t)}{dt}]$) whose maximum slope, occurring in general at $t = \Delta t$ ($\Delta t \ge t_1$), is equal to SR_0. Taking into account that the continuity of both $v_0(t)$ and its derivative at $t = t_{LS}$ has to be guaranteed, (i.e. $v_{SS}(t)$ cannot be then roughly joined to the straight line of slope SR), simple geometric considerations lead to the following expression:

$$v_0(t) = v_{SS}(t - t_{LS} + \Delta t) + \alpha G_0(V_{IS} - V_{SS}) \quad t > t_{LS}, \quad (3)$$

where $t_{LS} = t_1 + \left|\alpha G_0(V_{IS} - V_{SS}) + v_{SS}(\Delta t) - v_{0,LIN}(t_1)\right| / SR_0$.

By implementing the above equations, the MATLAB function in the model of Fig. 2a predicts the evolution of the resonator output node, allowing the combined effect of the op-amp finite GBW, SR and PM to be analysed. Behavioural simulations of the second-order BPΣΔ modulator in Fig. 1 has been performed by considering the parameters in Tab. 1. A minimum SNDR value of 92 *dB* which equals to a resolution of 15 bits was supposed as target. Moreover, in order to emphasise the impact of the resonator dynamics, the other noise sources (such as the op-amp finite dc gain, saturation voltages, clock jitter and switch thermal noise) which are normally considered in behavioural simulations, were not included in the simulations.

First, a conventional dominant-pole behavioural simulation [5], [17], [18] was performed, by supposing the settling of the resonator to be well-predicted by using a single-pole system dynamics. According to the simulation results, a suitable choice for the op-amp is GBW=200 *MHz*, and SR=200 *V/μs*, for which SNDR=96.65 *dB*. However, real resonators are in general characterised by high-order dynamics. The impact of this behaviour cannot be neglected in order to guarantee efficient top-down BPΣΔ modulator design. As a consequence of this limited prediction capability of the single-pole modelling approach, an ineffective trial-and-error circuit parameters tuning in the transistor-level design phase of the modulator may give rise in order to fix the op-amp phase margin, for example, wasting the advantages of behaviour ΣΔ modulator simulation phase.

The proposed behavioural approach can be instead exploited to avoid this situation. The 3D plot in Fig. 3a shows the dependence of modulator SNDR on different GBW and SR values when PM=*60*°. White regions identify the couples of GBW and SR values for which $SNDR \ge 92$ *dB*. It is worth noting that although the phase margin of 60°, chosen according to a well-founded rule of thumb, guarantees sufficiently-high stability margin for the op-amp in many practical situations, the desired modulator SNDR is reached only when the couple of GBW and SR is actually carefully chosen. For the same values of GBW e SR previously considered (i.e. GBW= 200 *MHz* and SR= 200 *V/μs*) the modulator SNDR is equal to 25.43 *dB*. Instead, in order to limit the power consumption (higher GBW and SR, higher the power consumption) for PM=*60*° a suitable choice can be GBW=500 *MHz* and SR=500 *V/μs*, which guarantees SNDR=97.34 *dB*.

In a realistic power-constrained design scenario, the use of the proposed approach can then avoid a rough modulator building block parameters choices which may directly result in poor system performance. In fact, by considering different values for PM, similar plots to the one in Fig. 3a can be obtained with the aim of understanding clearly the combined

Sampling frequency f_S	102.4 *MHz*
Intermediate frequency (IF)	$f_S/4$
Oversampling ratio	256
Signal bandwidth	200 *kHz*
Samples number	65536
Resonator gains	b_1=0.125, b_2=0.125, b_3=0.25, b_4=1

Table 1. Simulation parameters of the modulator in Fig. 1

effect of GBW, PM and SR on the modulator performance, by identifying the triplet of values to reach the desired SNDR value. Moreover, the usefulness of the proposed approach can be further appreciated by comparing the base-band power spectral density (PSD) plots of the modulator output in Fig. 3b. Differently from the conventional approach, by considering the high-order dynamics effects of the resonator the proposed behavioural simulation is able to predict the presence of the harmonic distortion peaks in the signal band which actually arise if the strong impact of the op-amp PM on the modulator performance is neglected.

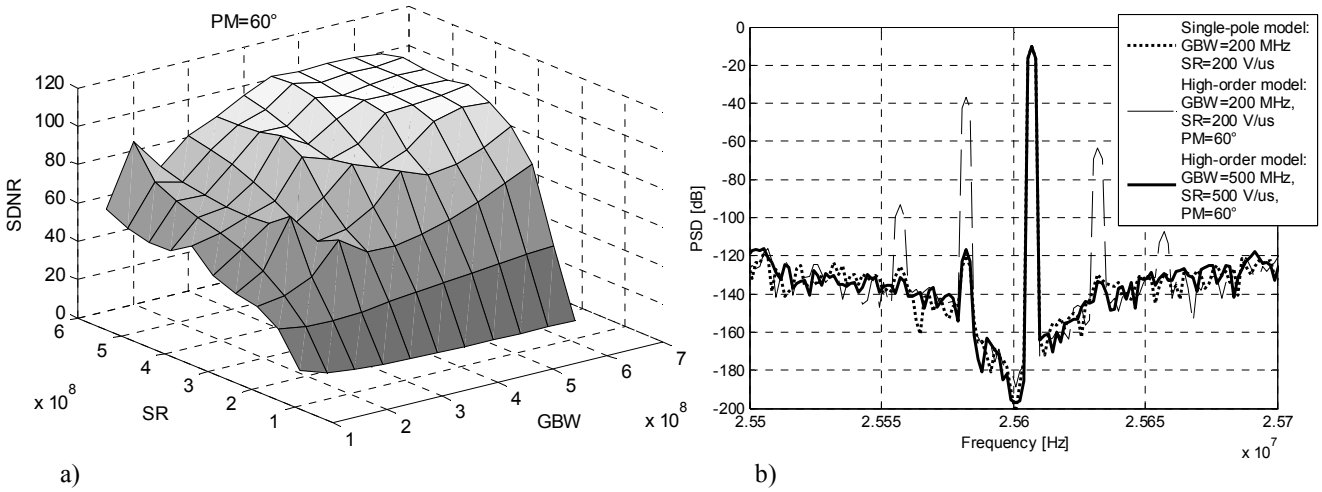

Figure 3. Effect of high-order settling of real resonator on second-order BPΣΔ modulator SNDR: a) 3D plot of SNDR versus GBW and SR, for PM=60°; b) PSD of the modulator output as predicted by the single-pole model [5] and the proposed high-order settling model

III. Band-pass ΣΔ ADC

The architecture of a BPΣΔ ADC with focus on its use for telecommunication measurement application [25] will be examined. The BPΣΔ ADC is composed by the BPΣΔ modulator, whose central frequency is equal to $f_s/4$, and the BP digital filter which cuts the quantization noise out of the band of the modulator. In this specific application, the converter architecture can be improved by using a digital down converter (DDC). The BPΣΔ modulator output feeds the DDC input that translates the frequency spectrum of the signal in base-band. Then, a low-pass decimator digital filter can be used to remove the high frequency quantization noise and increase the resolution. In particular, for this architecture two aspects are highlighted:

1) The DDC operates the frequency spectrum translation by multiplying the modulator output with a sinusoidal signal whose frequency is equal to $f_s/4$;
2) The low-pass decimator filter used into telecommunication standard with adequate band-width can be taken into consideration for cutting the quantization noise out of band of the modulator.

A. ADC dynamic parameters evaluation

In order to characterize the dynamic performance of the BPΣΔ ADC the most used parameters are the SNDR, the Effective Number of Bits (ENOB), the Signal to Noise Ratio (SNR), the Spurious Free Dynamic Range (SFDR), and the Total Harmonic Distortion (THD). These parameters can be estimated by the analysis of the acquired signal spectrum [26].

	Single-pole model	High-order settling model
SNDR	93.96 dB	32.28 dB
SNR	94.08	94.00 dB
ENOB	15.36 bits	5.07 bits
THD	3.33-4 %	2.43%
SFDR	107.80 dB	32.28dB

Table 2. Numerical results of the dynamic characterization

Preliminary numerical tests are devoted to highlight the effects of the resonator settling behaviour to the performance of the considered ADC architecture. In the setup of the BPΣΔ modulator, both the single-pole system dynamics and the proposed high-order model are used, taking GBW=200 MHz and SR=200 V/μs into account. For the BPΣΔ modulator based on proposed high-order settling model is also considered PM=60°. The plots in Fig.4 show the amplitude spectrum when the conventional single-pole model (Fig. 4a) and the proposed high-order settling model (Fig. 4b) are used, respectively. They highlight that several harmonics actually affect the spectrum

when the high-order dynamics is taking into account. In Tab. 2 the dynamic parameters estimation are reported. The data in the table confirm that although the SNR is similar, the other ADC dynamic parameters differ significantly when the single-pole model and the high-order one are used. In fact, the presence of the harmonics implicates that both the quality of the acquired signal and the results of the dynamic parameters evaluation get worse.

B. Frequency measure procedure

In the down conversion of a digital modulated signal, the input signal is multiplied by a sinusoidal reference signal with assigned frequency f_0 which is normally equal to the carrier frequency f_c and filtered at the Nyquist frequency to remove the mirrored effect. The signal obtained from the filter output is the correct down conversion in base band of the input signal. If the frequency f_0 is not equal to the f_c, the difference $f_{sh}=f_c - f_0$ can be attributed to the error affecting the carrier frequency. In [23], it was proposed a procedure to estimate this error based on the slope of the straight line representing the phase of the modulated signal down converted in base-band. The procedure provides a compensation of the effects generated by the symbol changing in the phase and estimates a regression line from the obtained samples. The slope of this regression line is the f_{sh}.

Numerical tests are devoted to investigate about the BPΣΔ modulator model influences into the frequency error measurement. With this goal, the 4-PSK modulated signal translated in frequency near $f_s/4$ feeds the input of the BPΣΔ ADC whose architecture is modified by means of two DDC with reference signal with a phase offset equal to $\pi/4$ [26], to detect the in-phase (I) and in-quadrature (Q) components of the acquired signal translated in base-band. The IQ components are used as input of the frequency error measurement procedure. The numerical test shows that no effect on the measure is actually appreciated for the two cases under examination. To further prove the impact of the high-order dynamics of the resonator of BPΣΔ modulator, the trend of the phase difference between IQ components when the two models are used is shown in Fig. 5. The plot highlights the phase difference has a sinusoidal shape. Nevertheless, the regression line estimated from the frequency error measurement procedure is not influenced by this effect.

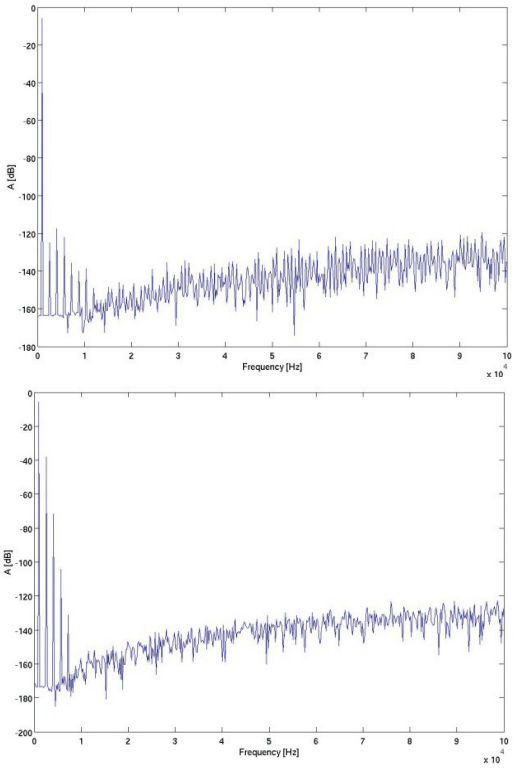

Figure 4. Signal spectrum a) single-pole BPΣΔ behavioural model, and b) proposed high-order model.

IV. Conclusions

In this paper, a behavioural simulations strategy based on a numerical model which allows the designer to predict accurately the impact of high-order dynamics of real resonators on the BPΣΔ modulators SNDR has been presented. Simulations results of a second-order BPΣΔ modulator have shown how high-order poles and zeros in the resonator frequency response affect significantly the modulator SNDR. Differently from the conventional single-pole model-based behavioural simulations, the proposed approach well-predicts the presence of the harmonic distortion peaks in the signal band which have a strong impact on the modulator SNDR. Moreover, other simulations based on a BPΣΔ ADC used in telecommunication applications have shown how harmonic distortions arise on digital modulated signal. These distortions influence strongly the ADC dynamic parameters, but they do not influence the result of the frequency error measure procedure.

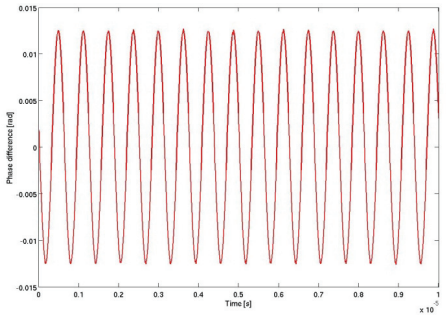

Figure 5. Trend of the difference between the phase of the digital modulated signals acquired by BPΣΔ ADC based on high-order settling model and single-pole modulator model.

References

[1] T. Hentschel, G. Fettweis, "Software radio receivers," *CDMA Techniques for Third Generation Mobile Systems,* Kluwer International Series in Engineering and Computer Science, vol. 487, pp. 257–283, 1999.

[2] F. Maloberti, "High-speed high-resolution data converters for base stations: technologies, architectures and circuit design," *Proc. of Workshop on ADC Modelling and Testing*, Prague, Czech Republic, June 2002, pp.1-6.

[3] F. Francesconi, V. Liberali, F. Maloberti, "A Band-Pass Sigma-Delta Modulator Architecture for Digital Radio," *Proc. of the 38th Midwest Symposium on Circuits and Systems, MWSCAS 1995*, Rio de Janeiro, August 1995, Vol. 2, pp. 885-888.

[4] F. Francesconi, G. Caiulo, V. Liberali, F. Maloberti, "A 30-mW 10.7-MHz Pseudo-N-Path Sigma-Delta Band-Pass Modulator," *Symposium on VLSI Circuits - Digest of Technical Papers, VLSIC 1996*, Honolulu, June 1996, pp. 60-61.

[5] S. Brigati, F. Francesconi, P. Malcovati, F. Maloberti, "Modeling Band-Pass Sigma-Delta Modulators in Simulink," *Proc. of International Workshop on ADC Modeling and Testing, IWADC 2000*, Vienna, Austria, September 2000, pp. 73-78.

[6] F. Singor, W. M. Snelgrove, "Switched-Capacitor Bandpass Delta-Sigma A/D Modulation at 10.7 MHz," *IEEE Journal of Solid-State Circuits,* vol. 30, pp. 184-192, March 1995.

[7] T. Salo, "Bandpass Delta-Sigma Modulators for Radio Receivers," Ph.D. Thesis, Helsinki University of Technology, 2003.

[8] S. Bazarjani, W. M. Snelgrove, "A 160 MHz Fourth-Order Double-Sampled SC Bandpass Sigma-Delta Modulator," *IEEE Transactions on Circuits and Systems II,* vol. 45, pp. 547-555, May 1998.

[9] T. Salo, S. Lindfors, K. Halonen, "A Low-voltage Single-Opamp 4th-order Band-Pass DS-modulator," *IEEE International Symposium on Circuits and Systems*, vol. I, pp. 352-355, May 2001.

[10] B. –S. Song, "A 4th-order bandpass SD modulator with reduced number of opamps*," IEEE Int. Solid-State Circ. Conf.,* pp. 204-205, San Francisco, CA, USA, Feb. 1995.

[11] S. Liu, C. Kuo, R. Tsai, J. Wu, "A Double-Sampling Pseudo-Two-Path Bandpass ΔΣ Modulator," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 276-280, February 2000.

[12] A. Pugliese, F. A. Amoroso, G. Cappuccino, G. Cocorullo, "Analysis of the Impact of High-Order Integrator Dynamics on SC Sigma-Delta Modulator Performances," *IEEE Trans. Circ. and Syst. –I: Regular Papers,* Vol. 57, No. 3, pp. 618-630, March 2010.

[13] A. Pugliese, F. A. Amoroso, G. Cappuccino, G. Cocorullo, "Effect of the Integrator Settling Behavior on SC ΣΔ Modulator Characteristics: a Theoretical Study," *2008 International Conference on Signals, Circuits & Systems (SCS'08)*, Hammamet, Tunisia, November 2008.

[14] A. A. Hamoui, T. Alhajj, M. Taherzadeh-Sani, "Behavioral Modeling of Opamp Gain and Dynamic Effects for Power Optimization of Delta-Sigma Modulators and Pipelined ADCs," *Proceedings of IEEE International Symposium on Low Power Electronics and Design*, pp. 330-333, 2006.

[15] R. Naiknaware, and T. S. Fiez, "Process-insensitive Low-Power Design of Switched-Capacitor Integrators," *IEEE Trans. On Circuits and Syst. I: Reg. Pap.,* Vol. 52, no. 10, pp. 1940-1952, Oct. 2004.

[16] U. Chilakapati, and T.S. Fiez, "Effect of Switch Resistance on the SC Integrator Settling Time," *IEEE Trans. On Circ. and Syst. II: Analog and Digital Signal Processing*, vol. 46, no.6, pp. 810-816, Jun. 1999.

[17] P. Malcovati, S. Brigati, F. Francesconi, F. Maloberti, P. Cusinato, and A. Baschirotto, "Behavioral Modeling of Switched-Capacitor Sigma-Delta Modulators," *IEEE Trans. On Circ. and Syst. I: Fund. Th. And Appl.*, vol. 50, no. 3, pp. 352- 364. Mar. 2003.

[18] F. Maloberti, P. Estrada, P. Malcovati, and A.Valero, "Validation of data converter specifications with behavioral modelling specifications," *Measurement, Elsevier*, vol. 31, pp. 231-245, 2002.

[19] P. Malcovati, S. Brigati, F. Francesconi, F. Maloberti, P. Cusinato, and A. Baschirotto, "Behavioral Modeling of Switched-Capacitor Sigma-Delta Modulators," *IEEE Trans. On Circ. and Syst. I: Fund. Th. And Appl.*, vol. 50, no. 3, pp. 352- 364. Mar. 2003.

[20] H. Zare-Hoseini, I. Kale, and O. Shoaei, "Modeling of Switched-Capacitor Delta-Sigma Modulators in Simulink," *IEEE Transactions on Instrumentation and Measurement*, vol. 54, no. 4, pp. 1646-1654, Aug. 2005.

[21] A. Pugliese, F. A. Amoroso, G. Cappuccino, G. Cocorullo, "Analysis of Op-Amp Phase Margin Impact on SC ΣΔ Modulator Performance", *Microelectronics Engineering,* Elsevier, Vol. 41, No. 7, pp. 440-446, July 2010.

[22] D.L. Carnì, D. Grimaldi, "Carrier frequency and phase offset measurement for general single carrier digital modulations," *Proc. of IEEE Instrumentation and Measurement Technical Conference IMTC/2004*, Como (Italy), pp.413-418, May 2004.

[23] D.L. Carnì, D. Grimaldi, "Sigma Delta ADC based frequency error measurement in single carrier digital modulations," *IEEE Transactions on Instrumentation and Measurement*, Vol. 55, n. 5, pp. 1523-1529, 2006

[24] G. Palmisano, G. Palumbo, S. Pennisi, "Design Procedure for Two-Stage CMOS Transconductance Operational Amplifiers: A Tutorial," *Analog Integrated Circuit and Signal Processing*, Springer, Vol. 27, pp. 179-189, 2001.

[25] L. Michaeli, J. Šaliga, M. Kollár, "Parameters of band pass ΣΔ-ADC and the comparison with the standard ones", *Measurement*, Vol. 40, Issue 5, June 2007, Pp. 473-478

[26] IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters, IEEE Std 1241-2000, 2000