

A Solution of The Integrated μ BIST for Functional and Diagnostic Testing in Mixed-Signal Electronic Embedded Systems

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Abstract- The paper concerns the testing of analogue circuits and blocks in mixed-signal electronic embedded systems (EESs), using the built-in self-test (BIST) technique. The integrated μ BIST based on reusing signal blocks already present in an EES, such as processors, memories, ADCs, is presented. The novelty of the solution is the extended functionality of the μ BIST. It can perform 2 testing functions: functional testing and fault diagnosis on the level of localization of a faulty element. For functional testing, the complementary signals (CSs), and for fault diagnosis the SBT vocabulary techniques have been used.

I. Introduction

Electronic embedded systems (EESs) with an embedded intelligent unit in a structure, (usually in the form of microcontroller), are widely used in many branches of industry, technology and science. The dominant group of EESs are mixed-signal systems. A common fact of these systems is the presence of analogue circuits, since there always must be an interface to the real world. Mixed-signal EESs bring new challenges to the test problem of the analogue circuits and blocks, because there is lack of general test methods and strategies.

The main direction of development of testing of analogue circuits in EESs is the built-in self test (BIST) technique. In last years many specific solutions of BISTs dedicated for concrete circuits have been reported: oscillation-based BIST (OBIST) [1], digital reuse [2], histogram based [3, 4], dedicated for fully-differential stages [5, 6], $\Sigma\Delta$ BIST [7, 8] and ADC BIST for AD converters. The common feature of these solutions is hardware excess, i.e. the necessity to build an overhead hardware into the EES's structure, which introduces additional costs.

One promising solution to reduce the hardware overhead and testing costs is reuse of signal blocks already present in the EES (such as processors and memories) for a BIST creation. The new generations of microcontrollers (e.g. AT91SAM, ADuC814) have hardware resources (ADCs, DACs, timers, counters, analogue comparators) that allow to generate stimulating signals and measure responses of a circuit under test (CUT), as well as the computing power to realize testing procedures. Therefore, the hardware and software resources of modern microcontrollers are sufficient for creation of microBISTs (μ BISTs). These resources are sufficient, but simultaneously they are rather modest, thus special signals and procedures adequate to microcontroller resources must be used.

The new solution of the μ BIST for functional testing based on special shape designed complementary signals (CSs) [9,10, 11] has been proposed by the authors in [12] and it was named as CS-BIST. The other solutions of μ BIST for component fault location have been proposed in [13, 14]. The common feature of these solutions is functionality limited only to functional testing or fault diagnosis.

The novelty of the solution presented in this paper is the extended functionality of the μ BIST including both functional and diagnostic testing. In the proposed solution (named the integrated μ BIST) for functional testing, complementary signals and for fault diagnosis SBT (simulation before test) techniques have been used.

The paper is organized as follows: Section II presents the CS method for functional testing. Section III describes a vocabulary SBT technique for diagnostic testing. Section IV presents experimental realization of the integrated two-functional μ BIST and its verification in an exemplary EES.

II. Description and investigation of the CS method

The essence of this method is stimulation of the CUT by a special shape-designed CS signal, with parameters exactly matched to poles of the CUT's transfer function. Typical examples of α_T -parameters and T_T -parameters

CS signals are shown in Fig.1a,b. The first impulse of the CS signal drives the CUT into an initial state $y_{T0}(t)$, whereas the remaining impulses $y_{T1}(t)$, $y_{T2}(t)$ compensate it, in the manner shown in Fig. 1c, that the CUT response $y(t_e)$ reaches zero state at the signal end time t_e . Such situation takes place when the CUT is in its nominal state. In a faulty state, when transfer function poles are deviating from nominal values, the CUT response after the end of stimulation is not compensated ($y(t_e) \neq 0$).

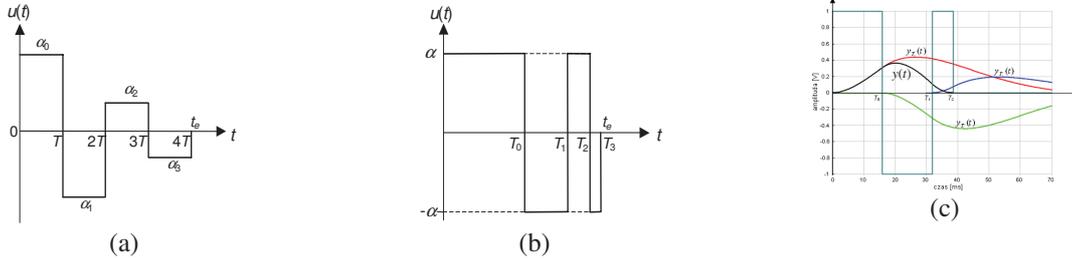


Figure 1. Examples of the 3rd order CSs: (a) α_i -parameters CS, (b) T_i -parameters CS and (c) CUT responses $y_{T_i}(t)$ to each T_i -parameter CS and its resultant response $y(t)$.

The relation between CUT transfer function poles and α_i -parameters and T_i -parameters used for design of matched CS signals are given in papers [11, 12].

The CS method has been widely investigated in a PhD dissertation [14] on the example of testing of 2nd and 4th order Butterworth low-pass filters, whose transfer functions are described by the following formulas:

$$G_{II}(s) = \frac{\omega_n^2}{s^2 + \frac{\omega_n}{Q_1}s + \omega_n^2}, \quad G_{IV}(s) = \frac{\omega_{n1}^2 \omega_{n2}^2}{\left(s^2 + \frac{\omega_{n1}}{Q_1}s + \omega_{n1}^2\right) \cdot \left(s^2 + \frac{\omega_{n2}}{Q_2}s + \omega_{n2}^2\right)}, \quad (1)$$

where: ω_n , ω_{n1} , ω_{n2} are cut-off angular frequencies, Q_1 , Q_2 are quality factors.

Here we present some selected results of investigations on the example of a 4th order low-pass filter with a cut-off frequency of $f_c=10$ Hz and the following parameters: $\omega_{n1}=\omega_{n2}=62,8319$ rad/s, $s_1, s_2=-58,0491 \pm 4,0447i$, $s_3, s_4=-24,0447 \pm 8,0491i$, $Q_1=0,54119$, $Q_2=1,30655$. The parameters of the CS signal matched to this filter, that were designed according to the method presented in [12], are as follows: $T_0=15,916$ ms, $T_1=37,393$ ms, $T_2=57,185$ ms, $T_3=70,397$ ms, $T_4=t_e=75,027$ ms. The investigation results of the influence of quality factors Q_1 , Q_2 and angular frequencies ω_{n1} , ω_{n2} on the CUT's output signal are presented in Fig. 2.

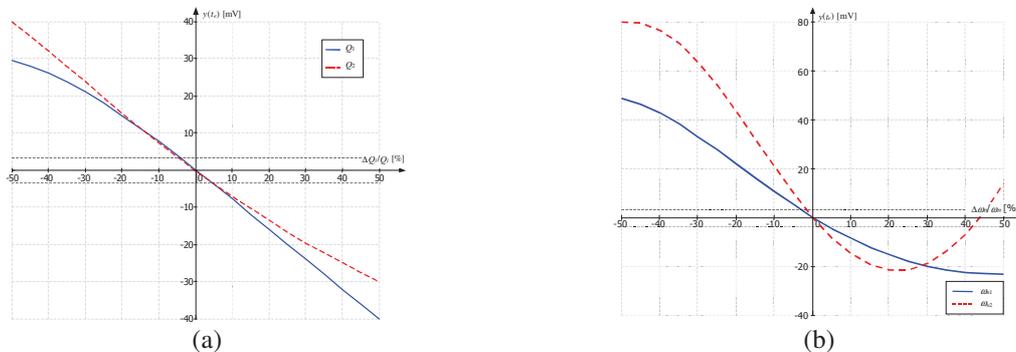


Figure 2. Responses $y(t_e)$ of the tested 4th order filter as a function of Q_i factor deviations (a) and as a function of angular frequency ω_{ni} deviations (b).

It is seen from plots shown in Fig. 2 that in the case of T_i -parameters CS, the sensitivity of the output signal $y(t_e)$ to Q -variations ($\Delta Q_i/Q_i=10\%$, $y(t_e)=10$ mV) and also to ω_{ni} -variations, is easy to measure using AD converters available in the microcontroller, and sufficient for implementation in the μ BIST. Generally, hardware resources of the ADuC814 microcontroller (12-bit ADC and DACs and 3x16-bit programmable counters) are good enough for generation of CS signals with adequate precision and for accurate measurement of CUT's output responses.

The metrological properties of the T_i -parameters CSs are better in comparison with the α_i -parameters CSs, and they are easier to generate basing on microcontroller resources. Therefore, T_i -parameter CSs are predestined for application in μ BISTs, for testing of frequency characteristics of analogue circuits, channels and blocks in the EESs.

III. Description and investigation of the SBT diagnostic method

For realization of fault diagnosis testing of analogue circuits in the EESs, which appears as the second function

of an integrated μ BIST, the vocabulary SBT method has been chosen. For application in the μ BIST, the fault dictionary with fault signatures in the form of identification curves in multidimensional spaces is predestined. Such form of the fault dictionary has 2 advantages:

- Identification curves can be scaled, thus they make possible fault localization and also identification.
- It is possible to introduce an additional distinctive feature of measurement signal to increasing dimension of measurement space, and in consequence rarefying curves in the space. In result it enables to increase distinctivity of fault localization and to decrease the fault masking effect of parameter tolerances.

There are few methods of creation the identification curves: using bilinear transformation, using as multi-dimensional coordinates the values $u_1(t_1), u_2(t_2), \dots, u_k(t_k)$ of samples of the CUT's output response at properly chosen time moments, and also taking as coordinates the time values $\tau_1(u_1), \tau_2(u_2), \dots, \tau_k(u_k)$ of the CUT's response crossing some chosen voltage levels u_1, u_2, \dots, u_k .

We explain this method on the example of the fault diagnosis of the 2nd order Butterworth low-pass filter whose configuration is shown in Fig. 3.

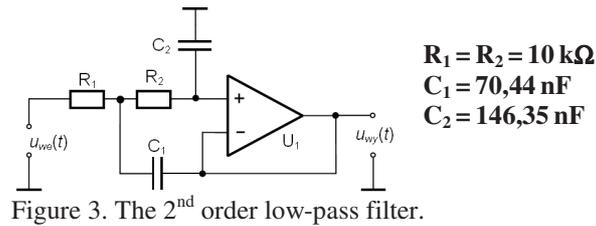


Figure 3. The 2nd order low-pass filter.

For the filter, on the basis of 2 or 3 samples of its output response to a single square-impulse stimulation, we can obtain the fault vocabulary in the form of a family of identification curves on a plane (for 2 samples $u_1(t_1), u_2(t_2)$) or in 3D space (for 3 samples $u_1(t_1), u_2(t_2), u_3(t_3)$) as shown in Fig. 4., for wide range of parameters changing: $-0,1p_{i \text{ nom}} \leq p_i \leq 10p_{i \text{ nom}}$. In this range curves can be strongly bent, difficult to describe and to interpolation.

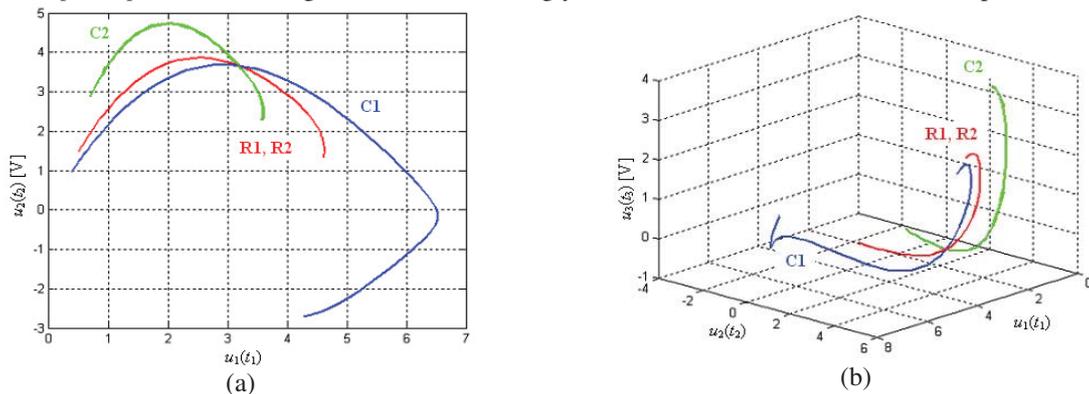


Figure 4. The families of identification curves on the plane (a) and in the 3D space (b).

In a practice, the soft faults are diagnosed in smaller ranges: $\pm 50\%$ ($-0,5p_{i \text{ nom}} \leq p_i \leq 1,5p_{i \text{ nom}}$) or even $\pm 20\%$. The family of scaled identification curves in the range $\pm 50\%$ is shown in Fig.5. In this range, as it is seen, the curves are smooth and easy to the point or PWL interpolation and to use as fault signatures, with small memory requirements.

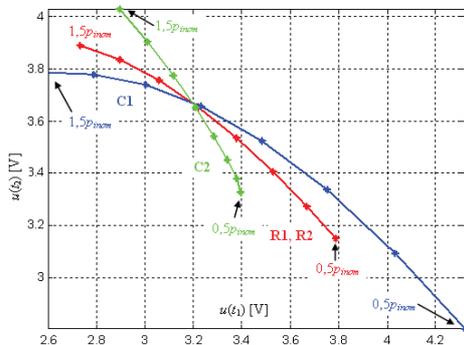


Figure 5. The family of the identification curves in the range $-0,5p_{i \text{ nom}} \leq p_i \leq 1,5p_{i \text{ nom}}$

The diagnostic procedure consists of two steps: fault detection and localization. In the first step the distance d between the measurement point $P_m=(u_1(t_1), u_2(t_2))$ and nominal point $P_n=(u_{n1}(t_1), u_{n2}(t_2))$ is checked. If the distance is less than an assumed value $d < \epsilon$, the circuit is treated as fault free and the algorithm is stopped. Otherwise, it goes to the next step, in which the search for minimum distance between the measurement point and curve p_i is performed. The i index for p_i curve with the minimal distance to the measurement point locates the faulty element. There is also a possibility to identify soft faults basing on the curve's scale. Described testing procedure can be useful for fault diagnosis of analogue circuits with small

parameter tolerances $\leq 1\%$.

In practise, analogue circuits have higher tolerances (in real circuits 2% or 5%), which cause dispersion of

identification curves in measurement space. The dispersed curves form in the 2D space kind of identification belts, and in the 3D space they form the identification snakes as shown in Fig. 6. Such families can be obtained from simulations using Monte Carlo method. Identification belts and snakes in general case have variable cross sections, but for moderate CUT's tolerances ($\pm 2\%$) their can be assumed as constant.

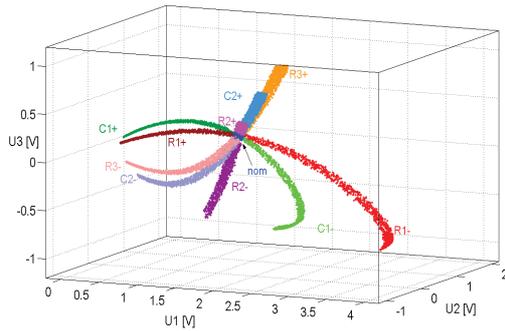


Figure 6. The family of dispersed identification curves of the exemplary circuit with tolerances of 1% for resistors and 5% for capacitors [16].

are described by 2 factors: *coordinates of interpolating points* of the nominal identification curve, and *the scaling factor δ* , which characterises the dispersion of the curve in these points. The testing procedure is simple. It is based on sequent checking of a distance between the measurement point P_m and the interpolating points of identification curves, with use of a conventional point distance classifier.

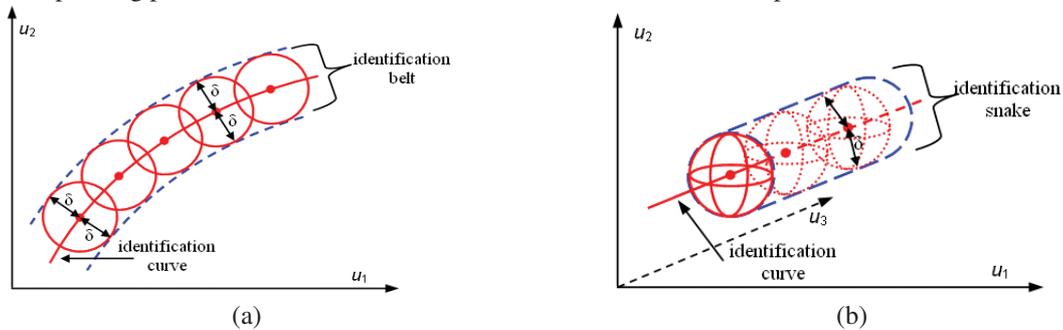


Figure 7. Models of identification belts and snakes in 2D (a) and 3D (b) spaces.

Different version of the method were investigated, but for implementation in the μ BIST, realized in the mentioned microcontroller ADuC814, we have used the 3D version of the method with the following assumptions: all identification snakes have constant scaling factor $\delta=2\sigma$, where σ is standard deviation, distance between interpolating points is equal to 1.5δ (the confidence level about 0.95). Description of the identification snakes in the fault dictionary (using coordinates of interpolating points and scaling factors) for the CUT with 10 elements requires 3000 bytes, for the fault range of $\pm 50\%$, and 1200 bytes for the range of $\pm 20\%$. In a testing procedure, 9 operations must be performed for the checking each interpolating point of identification curves in the fault dictionary. Thus, about 5000 operations are required for testing of 10 elements CUT. It can be easy realized in an acceptable time < 0.1 seconds.

IV. Experimental realization and verification of an integrated μ BIST

On the basis of hardware and software resources of the Analogue Devices microcontroller ADuC814, an integrated μ BIST for functional and fault diagnostic testing of analogue circuits in the EESs has been physically realized and investigated in the experimental embedded system. The structure of the μ BIST is shown in Fig. 8 and its circuit diagram is shown in Fig. 9. Almost all additional elements surrounding the ADuC814 chip are present in each EES and this is necessary for proper functioning of the microcontroller.

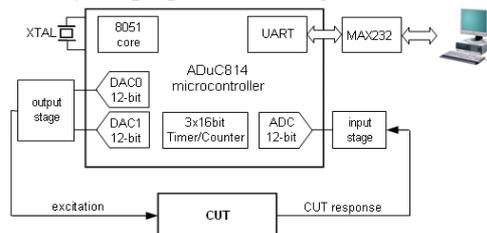


Figure 8. Block diagram of the realized μ BIST.

The microcontroller was programmed with the software realising two testing procedures of functional testing (via T_r -parameter CS signals) and the fault diagnostic testing (via the SBT method with sampling of the CUT output response). The algorithm of functional testing consumes not more than 980 bytes, while memory consumption by the algorithm of the fault diagnosis is about three times larger.

The μ BIST was investigated in the experimental EES on the basis of physical testing of real analogue circuits, mainly filters. Various values of Q_i , ω_n parameters and values of soft faults for each p_i element were physically entered to a real circuit.

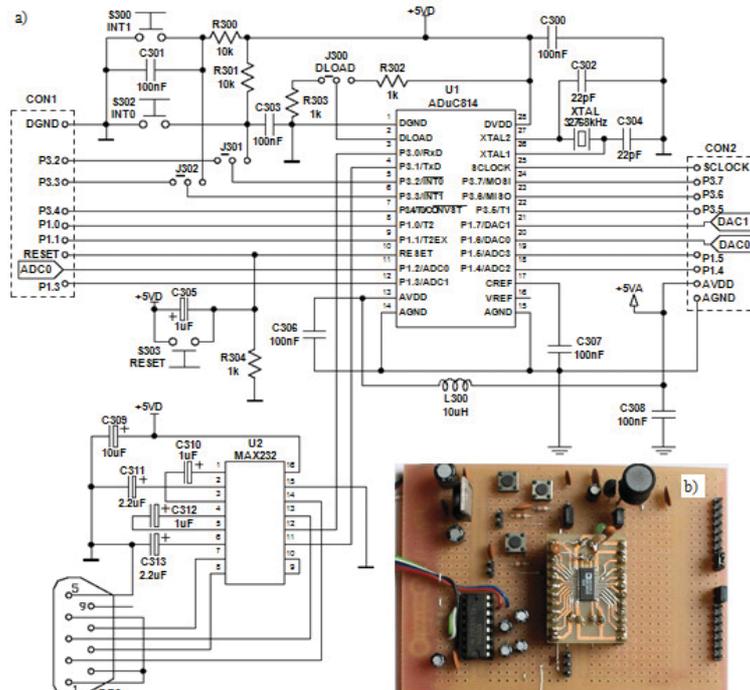


Figure 9. Circuit diagram of the realized μ BIST (a) and its picture (b).

For the functional testing the experimental results were compared with simulation ones. For example, in Fig. 10a experimental and simulated plots are shown concerning the influence of Q_1 factor deviation from the nominal state on CUT's response $y(t_e)$. Fig. 10b shows the plots of the CUT's responses as a function of ω_{n2} variations. As it is seen, the experimental results are very close to the simulated ones, especially in the range of $\pm 10\%$ of Q_1 deviation and in the range of $\pm 5\%$ of ω_{n2} deviation. The maximal experimental errors in $\pm 50\%$ range of Q_1 and ω_{n2} deviations did not exceed 3 mV.

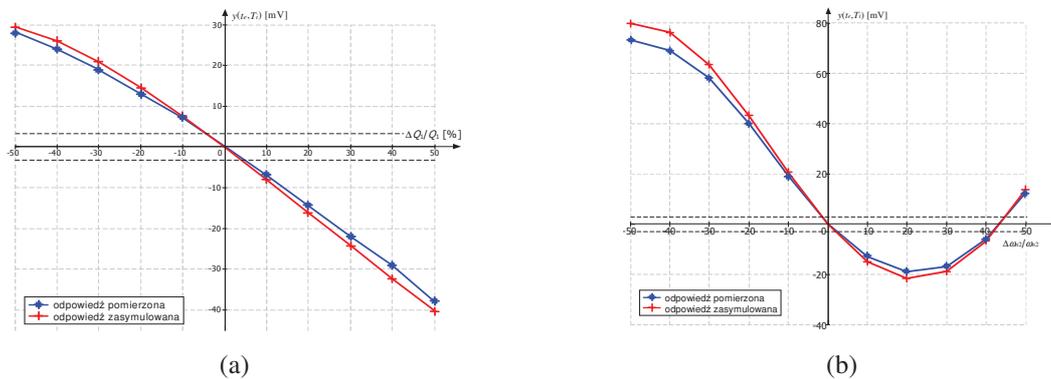


Figure 10. The simulated and measured responses in the realized μ BIST for Q_1 (a) and ω_{n2} (b) deviations.

Also an investigation of the diagnostic testing on the level of soft faults localization gave good results, widely presented in the Ph D dissertation [14]. Generally, the diagnostic function of the μ BIST can be useful for fault localization in analogue circuits with a moderate number of components (7-10), like filters, equivalent circuits of signal transmission lines or non-electrical objects (e.g. sensors) modelled in the form of multi-elements two-terminals or two-ports. The method is limited to the diagnosis of single soft faults in analogue circuits. It shows

the singleton faults and ambiguity groups. There are many possibilities of improving the method by better forms of the representation of dispersed identification curves. Recently, the neural classifier with two-central basis functions has been elaborated and reported in the Ph D dissertation [16]. It is well suited to application in μ BISTs. We are going to implement this classifier in the new version of the integrated μ BIST.

V. Conclusions

In the paper we proposed a new concept and solution of an integrated two-functional μ BIST, dedicated to testing of analogue parts of electronic embedded systems, which integrates 2 functions: the functional testing and fault diagnosis on the level of localization of a faulty component. The μ BIST has been constructed on the basis of reuse of the signal blocks (like microcontrollers) already present in each EES. We showed that the new generation of microcontrollers, like the ADuC814, have hardware and software resources sufficient to design μ BISTs for functional and diagnostic testing of linear analogue circuits, like filters, signal transmission paths or even some non-electrical objects (e.g. some sensors) modelled by electrical two-terminals and two-ports. There are perspectives of further improvement of the presented μ BIST, using a neural classifier that is more suited in μ BIST application.

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