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Experimental setup for non-destructive measurement of tunneling currents in semiconductor devices

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Abstract- A new experimental setup used to perform non-destructive measurement of electrical quantities on semiconductor devices is described in this paper. The particular case of tunneling current measurement in n-type metal-oxide-semiconductor (MOS) capacitors, whose dielectrics play a crucial role in non-volatile memories, has been investigated. When the gates of such devices are polarized with a sufficient bias voltage while the other terminals are grounded, tunnel conduction of electrons through the thin oxide layer is allowed. Typical tunneling current measurements obtained with this advanced setup are presented and compared to the results yielded by older standard experimental protocols. An application to the experimental observation of the temperature dependence of the tunneling current is proposed. Conclusions about the benefits of this kind of electrical measurements are then drawn.

I. Introduction

In the particular field of floating gate non-volatile memory (NVM) devices, such as EEPROM and Flash memory cells that can be found in nowadays common products like USB flash drives and smart cards, information is retained as an electric charge in the floating gate of a transistor. According to the value of this charge, two distinct logical states '0' and '1' can be differentiated from the 'virgin' state (floating gate void of charge) as shown in figure 1. The transition from one state to the other is obtained, when an electric signal is applied to one of the transistor's terminals, by the injection or withdrawal of electrons from the floating gate through the thin oxide layer of the transistor [1]. Due to this functioning, this thin oxide layer is critical to the reliability of the memory device. A schematic representation of a floating gate transistor used to realise EEPROM cells is given in figure 1.

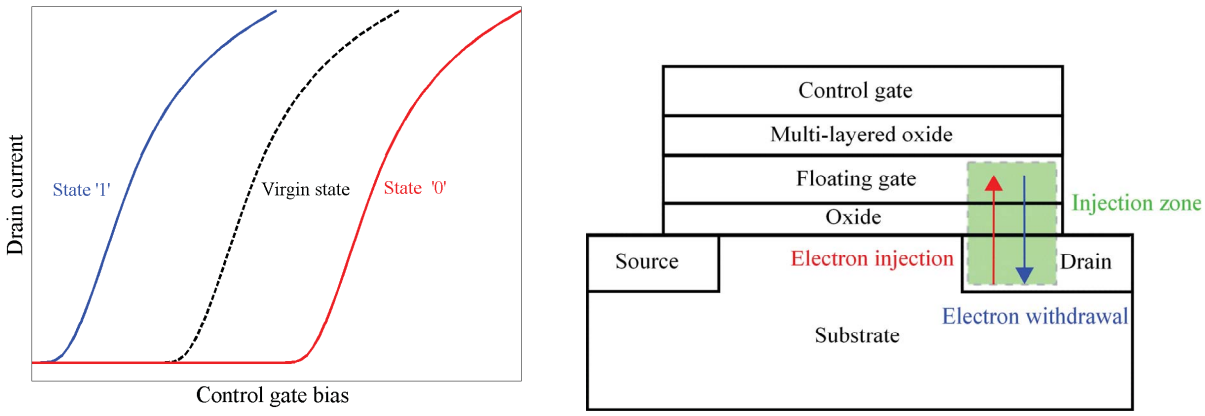

Figure 1. Distinction of two logical states according to the value of the floating gate charge (left). Schematic representation of a floating gate transistor used to realise EEPROM cells (right). The oxide is thinner in the injection zone to allow the tunnel conduction of electrons from the floating gate to the drain or vice versa.

The understanding of the electrical behaviour of such devices requires knowledge about the physical properties

of the injection zone of the memory devices. These properties can be studied through electrical characterization of test structures representative of the real device. In particular, measurement of tunneling current-voltage characteristics on test MOS capacitors is necessary.
Considering the various limitations of the standard methods usually used to measure tunneling currents, the need for a new non-destructive experimental setup and its description are detailed in section II. Section III presents typical experimental results obtained using this new setup, and benefits of dynamic measurement are highlighted. Finally, section IV draws conclusions on the presented experimental protocol and results.

II. Experimental setup

"Static" and "dynamic" current measurements are performed on 7.5 nm thick oxide n^{++} silicon/SiO_2/n^+ silicon capacitors (Fig.2), which are representative of the floating gate / tunnel oxide / drain injection zone of EEPROM devices. Doping concentrations of the gate and the back gate are 4.10^{19} cm^{-3} and 6.10^{18} cm^{-3} respectively. In order to be able to acquire tunneling currents that are measurable with parameter analysers, the area of these test structures has to be large enough (A = 100,000 µm²),

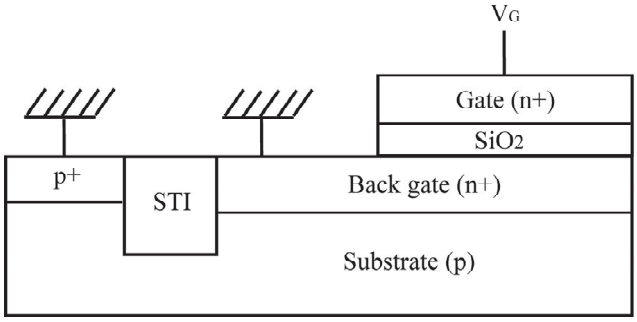

Figure 2. Simplified representation of the tested n-type capacitors. The signal is applied to the gate and current measurements are realized while the two other terminals are grounded.

A. Standard I-V Sweep Measurements

Static current measurements were performed with a classical Agilent 4156C parameter analyzer on n-type capacitors for negative gate voltages. In this case, the standard current sweep method is used, i.e. a succession of voltage ramps and plateaus of different amplitudes is applied to the gate through Source Monitor Unit 1 (SMU 1), and the current is measured during the plateaus as shown in figure 3. The major drawback of this kind of measurement, outside of its relative slowness and its inability to evidence transient regimes, is the difficulty encountered to evaluate the measurement time. The measurement time is the sum of the integration time that is set by the user and an "overhead" time that can't be controlled [2]. As a consequence, the time spent by the capacitor under polarization is not known accurately and the impact of such measurement in terms of oxide degradation, which can be far from negligible when high polarization fields are involved [3], cannot be quantified.

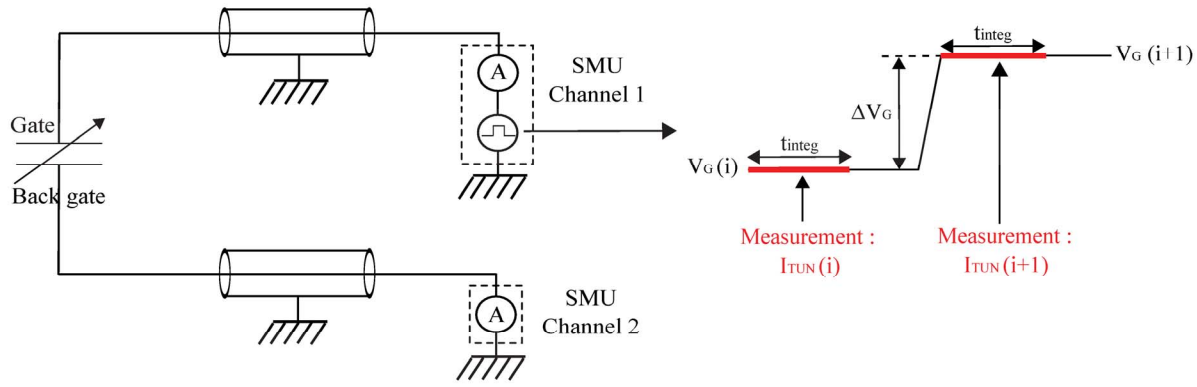

Figure 3. Experimental setup used for static tunneling current measurements on test capacitors. The signal applied to the gate of the device is represented on the right.

B. Dynamic I-V measurements

Dynamic measurements are performed with the help of an Agilent B1500A and its fast I-V module (WGFMU – B1530A) [4]. Short negative pulses of various rise and plateau times are applied on the gate of the n-type capacitors through Waveform Generator/Fast Measurement Unit 1 (WGFMU 1) and current measurement is realized during the whole polarization time (ramps and plateaus). The transient and permanent properties of the test capacitors can thus be observed using a single signal.
The minimal current measurement range value being 1 µA, we can reasonably expect to correctly measure currents as low as 1 nA. Integration time is dependent on the current level and can be set as low as 100 ns when large tunneling currents are involved. The general shape of the electric signals applied to the gates of the test capacitors during this kind of measurement is presented in figure 4. In this case, both the tunneling and displacement currents are acquired.

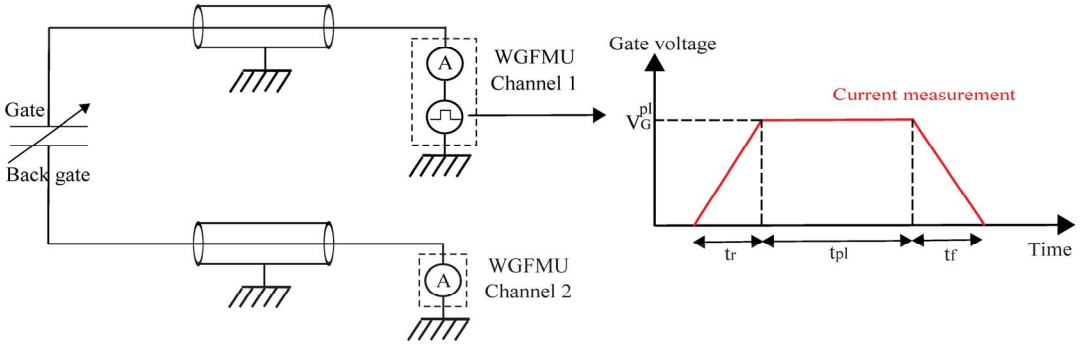

Figure 4. Experimental setup used for dynamic tunneling current measurements on test capacitors. The shape of the gate signal is determined by its rise time t_r, plateau time t_{pl}, fall time t_f and plateau voltage V_G^{pl}.

III. Experimental results

A. Tunneling I-V characteristics

A typical example of dynamic current measurement carried out for negative gate signals is shown in figure 5. The transient gate and back gate current characteristics $I_G(t)$ and $I_{BG}(t)$ can be divided into four main zones for which a dominating physical mechanism can be held responsible for their evolutions [5]. The steady-state gate and back gate current values can be extracted in the fourth zone for which the permanent regime has been reached. The reproduction of such current extraction for characteristics obtained for gate signals of various amplitudes V_G^{pl} leads to the acquisition of a complete tunneling I-V characteristic.

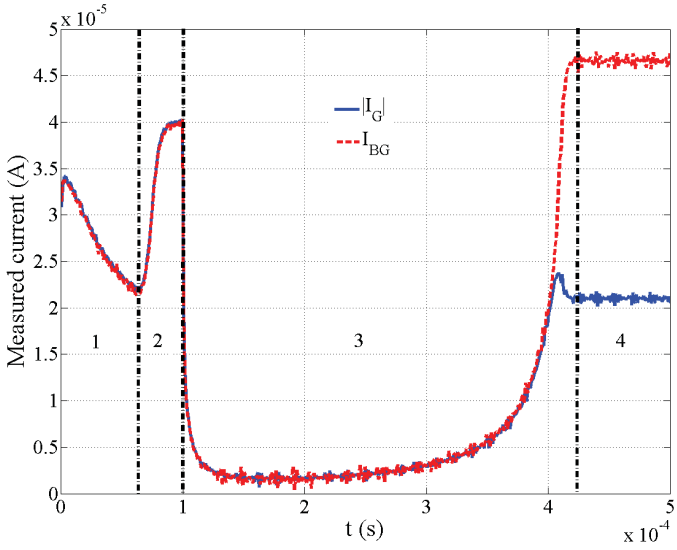

Figure 5. Dynamic tunneling current measurement realized at room temperature (t_r = 100 µs, V_G^{pl} = -8.4V).

B. Tunneling current degradation

The comparison of the tunneling I-V characteristics obtained from static and dynamic measurements is realized in figure 6. It can be observed that both experimental setups yield near identical results as long as the gate signal amplitude | V_G^{pl} | remains inferior to 8.5V. For higher gate voltages, the difference between both characteristics is pretty neat (about 30%). In the static measurement case, the time spent under polarization by the test capacitor is sufficient to provoke oxide degradation when high electric fields are involved.
This degradation, often attributed to interface states and to the trapping of electrons and holes in the oxide bulk near the anode interface [6] [7], is avoided in the case of dynamic measurements for which the plateau time of the gate signal is reduced to a minimum. On the contrary, figure 7 shows the evolution of the measured gate current as a function of time when a negative pulse of a longer plate time is applied (constant voltage stress). When high gate voltages are involved, oxide degradation resulting charging of the oxide leads to a fast evolution of the gate current, thus explaining the difference between static and dynamic I-V characteristics of figure 6 and stressing the need for a fast and non-degrading measurement protocol.

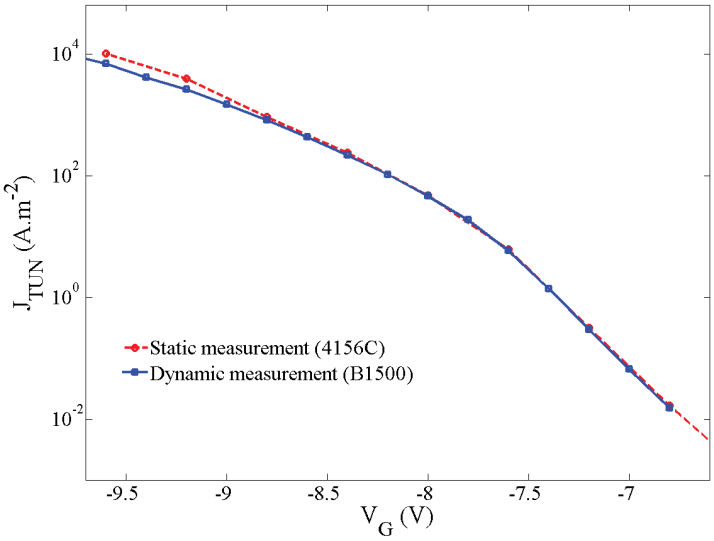

Figure 6. Comparison of the tunneling I-V characteristics obtained from static (red) and dynamic (blue) measurement methods.

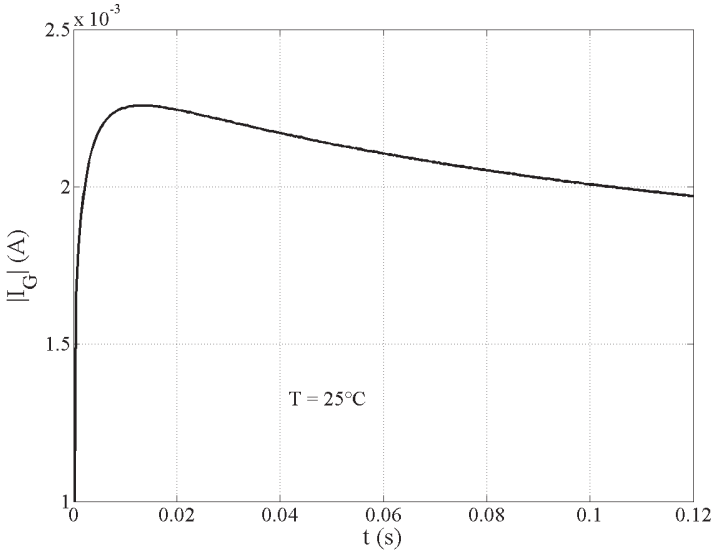

Figure 7. Dynamic gate current measurement realized at room temperature for V_G^{pl} = -9.8V.

C. Temperature dependence of the tunneling current

Study of temperature dependence of the tunneling current in MOS structures has been pretty well documented in the literature over the years. Many authors propose a decrease of the cathode/oxide barrier height as a plausible explanation for the experimentally observed increase in tunneling current with temperature [8] [9]. However, most works found in the literature give very few details concerning the characterization method employed to gather experimental data used to study the temperature dependence of the tunneling current. Most of the time, it can be assumed that either each I-V characteristic is obtained on a fresh test capacitor but the current measurement leads to some oxide degradation that can be enhanced with temperature, or that consecutive degrading current measurements are performed on a single test capacitor. In both cases, the experimentally observed temperature of the tunneling current is inaccurate.
Figure 8 shows two tunneling I-V characteristics obtained according to the method described in section III.a for two different temperatures (T = 25°C and T = 125°C). These experimental results, coherent with the study led in [10], show that the gate current is temperature independent when strong negative gate voltages ($|V_G| > 7.5V$) are applied on the gate of the test capacitors for which the back gate doping concentration is moderately high (i.e. inferior to about 1.10^{19} cm^{-3}). Such observations are very useful to simulate the electrical behavior of non-volatile memory devices as a function of temperature. It has been shown that the inclusion in numerical models of an inaccurate temperature dependence for the tunneling current, which is responsible for the charging of non-volatile memory floating gates, leads to unsatisfying predictions of the threshold voltages associated to the logical states presented in figure 1 [11].

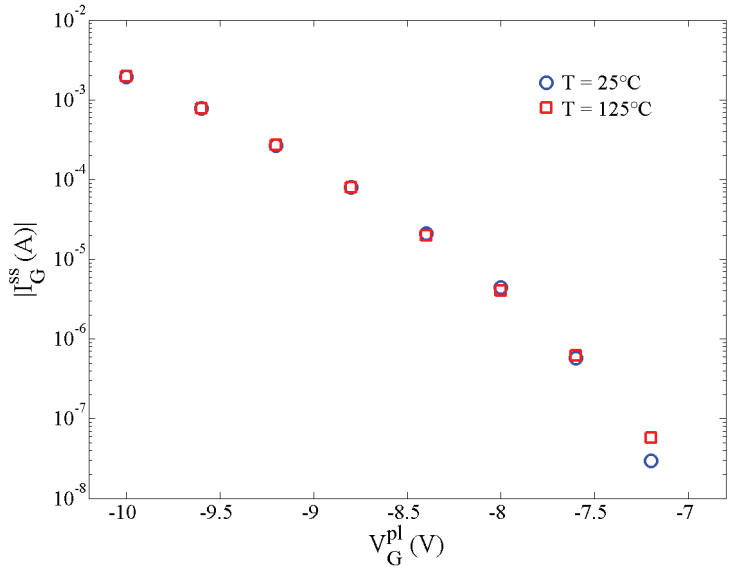

Figure 8. Dynamic measurement of the steady-state gate current value I_G^{ss} as a function of V_G^{pl} at T = 25°C and T = 125°C.

IV. Conclusions

A new experimental setup allowing non-destructive measurements of electrical quantities in semiconductor devices has been presented in this paper. Potential applications to the electrical characterization of MOS capacitors representative of the injection zone of floating gate non-volatile memory devices have been investigated. Dynamic tunneling current measurements performed according to this setup avoid oxide degradation as the polarization time is kept to a minimum, thus improving the measurement quality and saving the test structures for further electrical characterization. It also enables the observation of transient regimes that give useful information about the physical properties of the elementary cells, which will be embedded in the final product with a higher reliability level.

References

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