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CHARACTERIZATION AND VOLUME TEST OF THE AM06 CHIP

Seyed Ruhollah Shojaii [1], *Alberto Annovi* [2], *Davide Banfi* [3], *Matteo Beretta* [4], *Francesco Crescioli* [5], *Luca Frontini* [1,6], *Valentino Liberali* [1,3], *Lorenzo Marcellino* [3], *Alberto Stabile* [1]

[1] INFN - Sezione di Milano, Via G. Celoria 16, 20133 Milano, Italy, Email: sshojaii@cern.ch
[2] INFN - Sezione di Pisa, Largo B. Pontecorvo 3, 56127 Pisa, Italy
[3] Università degli Studi di Milano, Dip. di Fisica, Via G. Celoria 16, 20133 Milano, Italy
[4] INFN - LNF, Via E. Fermi 40, 00044 Frascati, Italy
[5] Laboratoire de Physique Nucléaire et de Hautes Energies, 4 place Jussieu, 75005 Paris, France
[6] Università degli Studi di Milano, Dip. di Informatica, Via Bramante 65, 26013 Crema, Italy

***Abstract* – This paper presents a methodology for the characterization and the industrial testing of a very complex Application-Specific Integrated Circuit (ASIC). The proposed test system is being installed at a company and it is very user friendly also for a non specialized operator.**

This framework has been developed within a collaboration by the Istituto Nazionale di Fisica Nucleare (INFN) and the Laboratoire de Physique Nucléaire et de Hautes Energies (LPNHE), and the same test setup is installed in the laboratories of INFN-Milan, INFN-Frascati and LPNHE-Paris.

1. INTRODUCTION

The AM06 is the 6th version of an Associative Memory (AM) chip. It has been designed for High Energy Physics (HEP) experiments application and fabricated in a 65 nm CMOS technology. The AM06 is a large digital chip, which occupies a silicon area of 168 mm^2 and contains about 421 million transistors. The chip core is composed by memory banks designed with full-custom approach and glue logic described in VHDL and synthesized with standard cells, while the perifery contains Serializer/Deserializer (SER/DES) IP blocks for high-speed serial communication [1]. The data stored in the memory is organized in 16 bit words; a group of 8 words is called a pattern. Each AM06 chip stores 2^{17} patterns and the chip input/output communication speed is up to 2.4 Gbit/s through the SER/DES IP blocks [2]. The AM internal operation is synchronous with a 100 MHz clock. At every clock cycle, the AM compares the input pattern with all the stored patterns in parallel; if a match is found, then the address of the stored pattern which matches the input pattern is sent to the output [3].

The AM06 chip is assembled into a 23×23 ball grid array (BGA) package for surface mounting.

HEP experiments require a large number of chips. More specifically, a production lot of 7500 AM06 chips will be fabricated within few months and all the chips of the lot must be tested with a standard procedure by a company. The developed test system has been set up at the company and it is very user-friendly and suitable also for an operator without specific training.

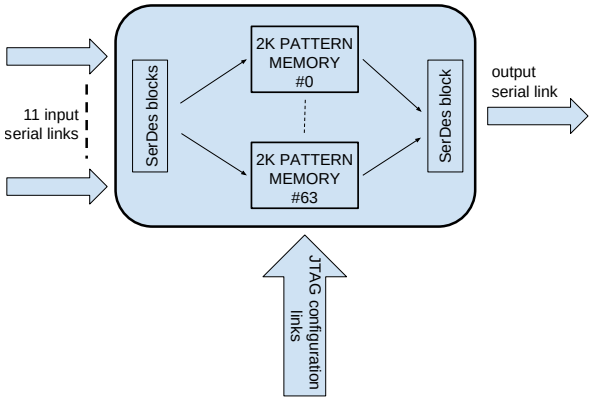

Fig. 1. AM06 architecture.

2. CHIP ARCHITECTURE

The AM06 architecture is based on the SER/DES interface and on the AM core, as shown in Fig. 1.

The input buses are organized in 11 serial links, each of them receiving serialized data. Input 16-bit words have a rate of 100 MHz, and are serialized with an 8b/10b encoding, thus giving a serial data rate equal to 2 Gbit/s. SER/DES input blocks convert the serial input to parallel data, which are sent to the core memory blocks.

The associative memory core is made of 64 blocks, each of them containing 2 k patterns. The core stores the patterns which the AM06 should find among the incoming data [4]. The AM06 compares the input patterns with the pre-stored patterns and the address of matching patterns are the output of the AM core. The address of the match-

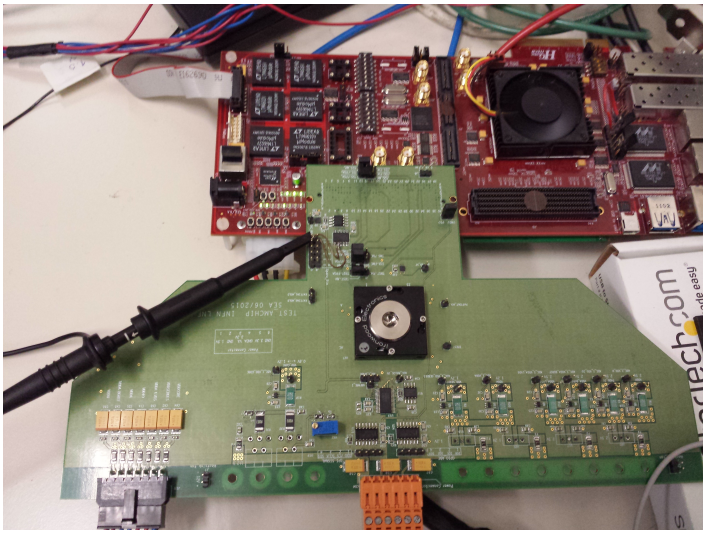

Fig. 2. Motherboard (red) and mezzanine board (green).

ing pattern is serialized by the output SER/DES block.

The AM06 has a standard JTAG interface for configuration and testing. One of the JTAG registers contains the ID code of the chip family.

3. MEZZANINE BOARD

Fig. 2 shows the test setup, which is based on a HiTech Global motherboard equipped with a VIRTEX-6 FPGA, and on a dedicated mezzanine board which contains a Zero-Insertion-Force (ZIF) scoket to allocate the chip under test.

The firmware for the FPGA was written in VHDL by LPNHE-Paris; a graphical interface in Python allows to set the test conditions and to start the test.

The mezzanine board was designed by INFN-Frascati and it provides two options for power supply:

1. independent voltages provided by several external power supplies;
2. on-board voltage supplies generated by DC-DC converters fed with a single external power supply.

The mezzanine board provides three different supply voltages, which are required by the AM06 chip:

1. SER/DES I/O, band-gap voltage reference, LVDS clock, and single-ended I/O are fed with 2.5 V;
2. SER/DES core and SER/DES standard cells are fed with 1.2 V;
3. the full-custom AM cores are fed with $V_{\mathrm{DD,core}} = 0.9 \div 1.2$ V.

In case of independent voltages, three different power supplies are used and the $V_{\mathrm{DD,core}}$ voltage is regulated from the PC connected to the power supply unit through the network.

When the on-board DC-DC converters are used, they generate two fixed supply voltages: 3.3 V and 1.2 V, while the voltage for the $V_{\mathrm{DD,core}}$ supply can be regulated manually by means of a trimmer.

The power consumption of core and SER/DES I/O blocks has been characterized very accurately on the mezzanine, which provides access points to measure the node voltages near the ZIF socket.

An on-board clock generator (100 MHz) is installed on the mezzanine, followed by a MUX and a clock buffer. The MUX receives both the motherboard clock and the mezzanine on-board clock as inputs, and it is possible to select one of the two clocks. The on-board clock generator provides a clock signal which is less noisy than the motherboard clock. Moreover, in HEP application the AMO6 will be driven by an on-board clock generator, and it is important to characterize the chip in realistic conditions. However, the FPGA clock generator has been also used, because its frequency can be changed by modifying the firmware and in this way we can investigate the chip performance with different clock frequencies.

The ZIF socket on the mezzanine board is the part of the test setup that needs to be handled more frequently. The operator must use a torque wrench to open and close the socket with the correct pressure on the chip package, to achieve good electrical contact between the chip and the mezzanine board, without damaging the chips solder balls. The system test setup will be placed into a box which pro-

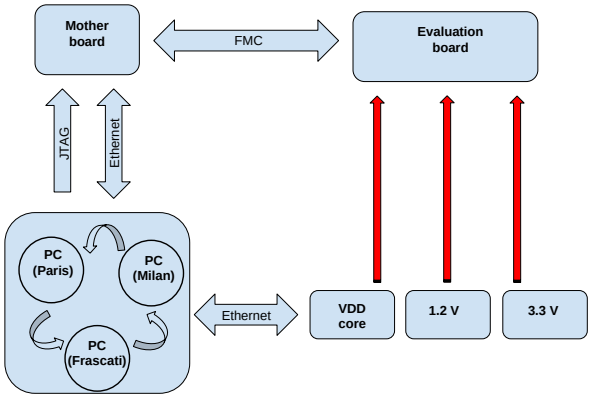

Fig. 3. Schematic diagram of the test setup.

vides access just to the ZIF socket to change the device under the test.

4. SYSTEM CONTROL AND COMMUNICATION

The PC communicates with the motherboard and with the $V_{\mathrm{DD,core}}$ power supply generator through the Ethernet (Fig. 3).

The test procedure consists of a set of Python scripts, which can be run also from remote. This feature allows to compare the behavior of the test boards in the three laboratories.

5. CHARACTERIZATION

The AM06 chip has been characterized with the described test system at the INFN laboratory in Milan.

Fig. 4 shows a portion of the $V_{\mathrm{DD,core}}$ characterization result when the mezzanine board is fed by the external power supply. The $V_{\mathrm{DD,core}}$ voltage exhibits many peaks which are related to the instants when the input patterns match with stored patterns. The reason is due to a peak in the instantaneous power consumption of AM06 when matching occurs. The same behaviour is observed also when the mezzanine is fed by the on-board DC-DC converter: in this case, the $V_{\mathrm{DD,core}}$ voltage exhibits a lower variation compared to the configuration with external power supply, however, the peaks are still present at the same instants.

For a better characterization of the AM chip, a second version of the mezzanine has been designed, which employs better filtering capacitors with very low series resistance and inductance, to achieve a reasonable attenuation of high frequency spikes.

The test procedure is made of three steps:

- **Pseudo Random Binary Sequence (PRBS) test:** the serial links of AM06 chip are characterized with a PRBS-7 sequence test which can have different duration:
  1. long time (several minutes or hours) at 2 Gbit/s, to obtain eye diagram and jitter;
  2. short time (0.1 s per serial link, i.e., ≈ 1 s in total) at 2 Gbit/s, for volume test.
- **Internal self-test:** a BIST circuit writes a particular sequence of patterns, then it generates input stimuli, and calculates the CRC of the addresses of all matching patterns.
- **Run test:** the chip is set into the "run" mode and a loop with a sequence of few events is given at the inputs; the output is compared with a predetermined list of matching addresses in real time.

The test sequence has 100 % coverage against single bit errors in the AM core blocks, in the readout, and in the main functions used to configure and run the AM chip.

The eye diagram of one of the AM06 serial links at 2 Gbit/s is shown in Fig. 5; the jitter is about 25 ps. The same result has been obtained for all chip serial links, thus confirming the good quality of the serial communication. The run test and the internal self-test results also confirm the functionality of the chip core at full speed. The AM06 chip is fully functional according to the specifications. Three identical test systems have been set up in Frascati, Milan and Paris. The three systems are connected together and users have access to the PCs through the network (see Fig. 3). The test of AM06 is ongoing, with frequent interactions between the three laboratories.

6. TEST COVERAGE AND COSTS

The AM06 chip is dedicated to HEP experiments and for this purpose 7500 AM06s are being fabricated. The test setup is finalized to test a large number of chips in a company. The volume test process is a combination of PRSB test, internal self-test and run test. The test procedure is automated as much as possible and a graphic interface has been developed to simplify the use of the test system.

For the operator, the test sequence consists of the following steps: (1) run a script that downloads the firmware onto the FPGA, without using directly the XILINX software; (2) run the python graphic interface; (3) mount the chip inside the ZIF socket; (4) run the test through the python interface; (5) when the test procedure is complete, remove the chip and put it into the appropriate bin, according to the test results displayed in the graphic interface; then another chip can be tested restarting from step 3.

The test result can be one of the following.

- **"GOOD"**: the software can read the ID code of the chip; the PRBS and internal memory tests have no error.
- **"DEFECTIVE"**: the software can read the ID code of the chip and the PRBS test has no error; the internal

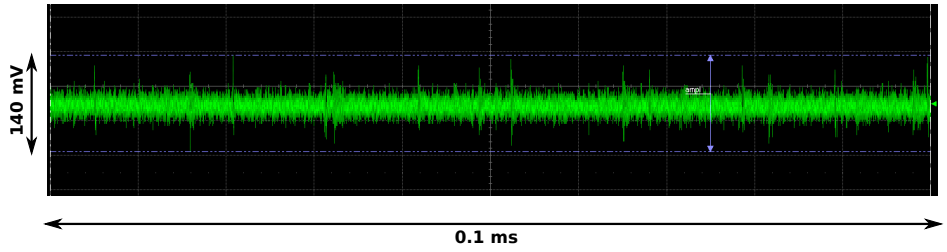

Fig. 4. Core voltage measured on the test board.

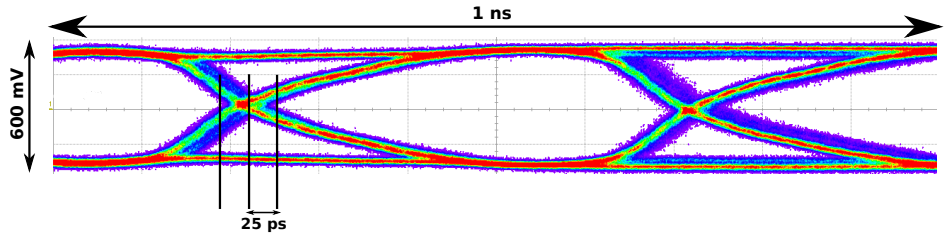

Fig. 5. Eye diagram of AM06 serial link at 2 Gbit/s.

memory test has errors located in some blocks of the associative memory.

- **"BAD"**: the software can not read the ID code of the chip or/and the PRBS test has errors. In this case the test procedure does not go further and stops before the internal memory test.

The standard test procedure for each chip requires 30 s and it is repeated twice, for two values of the $V_{DD,core}$ voltage. Taking into account the time for opening the ZIF socket and for changing the chip, the total time required to test a single chip is 1.5 min.

The time of test procedure can be changed by tuning a variable in the python script. When the test time is increased, the internal self-test procedure operates in a more detailed mode, thus providing information on the location of AM blocks which contain defects when characterizing a "DEFECTIVE" chip. This feature is not used in the industrial test.

The test setup has been assembled successfully at Microtest company in Altopascio, Italy, where the production lot of 7500 AM06 chips will be tested during next months. The test time for each chip has been kept short enough, to limit test costs; moreover, the test procedure is very user-friendly and does not require a specialized training of the operator.

7. CONCLUSION

This paper has presented the setup for testing the AM06 chip, a large associative memory designed for real-time pattern recognition in high energy physics experiments. The test setup and the measurement software have been developed to define a standard test procedure suitable for the industrial test of a large number of chips.

The laboratory characterization shows a fully functionality of both the AM06 and the test system.

A dedicated test procedure, especially developed for volume test, requires about 1 min of testing time. During this procedure, all the serial links of AM06 are tested with PRBS, and the core of the chip is tested with a self-test procedure based on CRC. The setup has been implemented successfully at the company and the operator is capable to perform the test of alarge number of AM06 chips without any interaction with test setup developers.

REFERENCES

[1] A. Andreani et al., Next generation associative memory devices for the FTK tracking processor of the ATLAS experiment, *Proc. IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*, pp. 1-6, 2013.

[2] M. Beretta et al., Next generation associative memory devices for the FTK tracking processor of the ATLAS experiment, *Journal of Instrumentation*, vol. 9, C03053, 2014.

[3] L. Frontini et al., A new XOR-based Content Addressable Memory architecture, *Proc. IEEE Int. Conf. on Electronics, Circuits and Systems (ICECS)*, pp. 701-704, 2012.

[4] A. Annovi et al., Design of a hardware track finder (Fast Tracker) for the ATLAS trigger, *Journal of Instrumentation*, vol. 9, C01045, 2014.