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Availability Comparison Between Distributed and Concentrated UPS Control Systems

Francesco Bertocci, Ada Fort, Marco Mugnaini, Valerio Vignoli

Dept. of Information Engineering and Mathematics, University of Siena, Siena, Italy
mugnaini@dii.unisi.it

Abstract **–Modern power systems require high reliability and availability standards in order to meet customer final expectations and market needs. In this context it is quite obvious that modern uninterruptible power supply (UPS) have started developing improvement strategies to achieve higher availability figures over time. At the same time power, dimension and performance constraints continued to be pushed up placing tight barriers to developers. UPS developers started therefore to design distributed systems where different functions could be allocated to different control board sections enhancing in this way with a limited effort the system availability and improving the overall device modularity and expandability. In this paper the authors tried to compare single core with distributed core boards availability performance including the possibility to model the board failure rates taking into account also environmental variations.**

I. INTRODUCTION

Modern data-centre development has pushed side service suppliers as UPS designers to evolve the requirements of their products. As a matter of fact this devices play a crucial role in assuring a continuous service for those who need to have access to data in every moment. Naturally the UPS availability performance together with the conversion efficiency become two important factors driving the selection of a device with respect to another.

In the last decades UPS developers tried to exploit different power conversion solutions as well as different architectures [1-2]. Recently some designers are proposing distributed architectures [1] as an alternative to traditional single block structures. These latter actually, even if providing the desired performance solution, were often lacking in flexibility and in case of additional power need could not be expanded further. On the contrary modular solutions could allow to match the conversion requirements and to satisfy customer expectations in terms of system configurability.

The modular development on the contrary requires improved electronic control board solutions which could jeopardize the achieved availability performance [3-8].

In order to overcome an overload of a single board for power conversion and communication management, and to achieve higher reliability and availability targets, producers started proposing distributed control board system.

The following paper is arranged in section I where the problem is introduced, in section II where the basic system architecture is provided in order to define the problem manifold and in in section III where the availability modelling is described. In section IV the simulation results are presented over a variety of operating assumptions for the main subsystem failure rates and finally section V collects the conclusions.

II. SYSTEM ARCHITECTURE AND DESCRIPTION

UPS structure can be summarize in a very simplified schematics as the one represented in Figure 1 There are two main parallel paths; one represented by the main feeder line which is supposed to be operative the majority of the time and a second one comprising an input filter stage, an AC/DC conversion block (taking into consideration double conversion UPS technology), a battery and an inverter section and final a bypass switch to move from the main line to the UPS structure upon need.

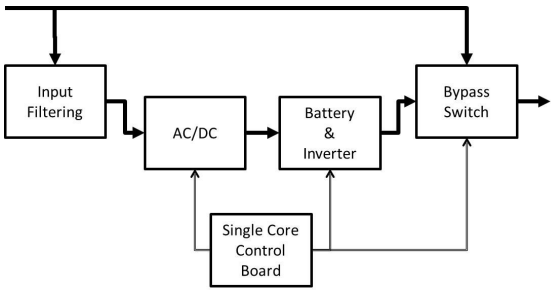

Fig. 1. General simplified single core UPS structure

All the power sections, that are in the AC/DC block, the inverter and the Switch are driven by a control board which is deputed to manage the communication with other modules if present. This control board can be managed by a single core structure as in Figure 1 or by

multicore arrangement as in Figure2. This latter solution has the advantage of distributing data processing operations lowering in this way the local temperature of the electronics. The enhanced number of components is therefore more than compensated by the temperature derating automatically applied. In Figure 2 in particular the assumption is to have a core dedicated to the AC/DC conversion and another one taking into account the battery and the inverter operations.

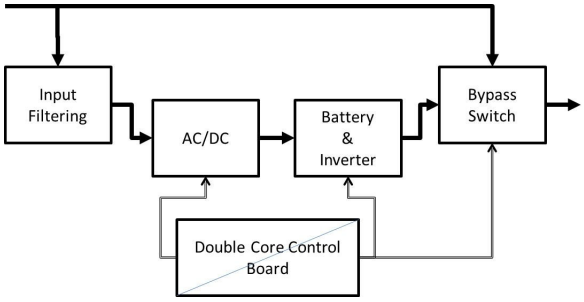

Fig. 2. General simplified multi core UPS structure

III. AVAILABILITY MODELLING

The simplified equivalent system of Figure 1 and Figure 2 reliability block diagram (RBD) is the one represented in Figure 3, where the components are considered as series and the multicore configuration is taken into account. Control board A represents the Inverter and battery section, control board B takes into account the conversion, while the power electronics embeds all the remaining system electrical and electronic components.

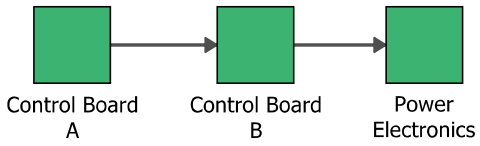

Fig. 3. Compact series block representation of the single core UPS power and control modules

In case we could consider that the system mission is not compromised if the control board section (control board B), devoted to the AC/DC conversion and consequent battery charger, fails one time then the proposed RBD changes as shown in Figure 4. Of course the assumption is valid considering that the UPS mission demand will happen only once and the battery will behave as an ideal storage.

The grey squares in the left lower corner of some of the blocks represent the mirroring condition, which means that the physical item representing that block in the real schematic is single even if in the RBD is replicated.

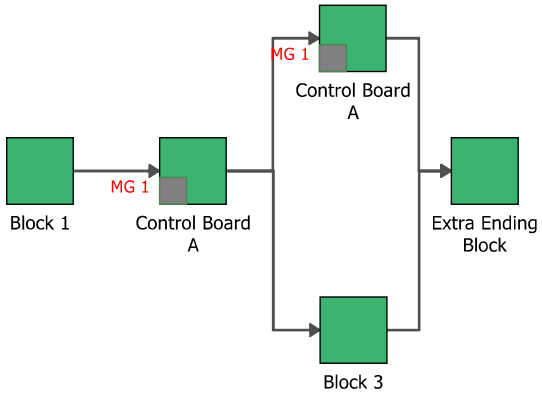

Fig. 4. Compact reliability block representation of the multi core UPS power and control modules

Figure 5 and 6 represent the corresponding fault tree diagrams (FTDs) to perform both reliability and availability analysis.

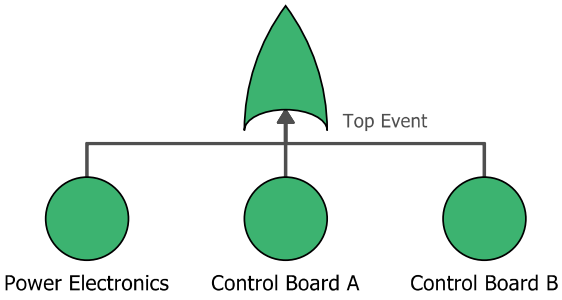

Fig. 5. FTD of the single core case

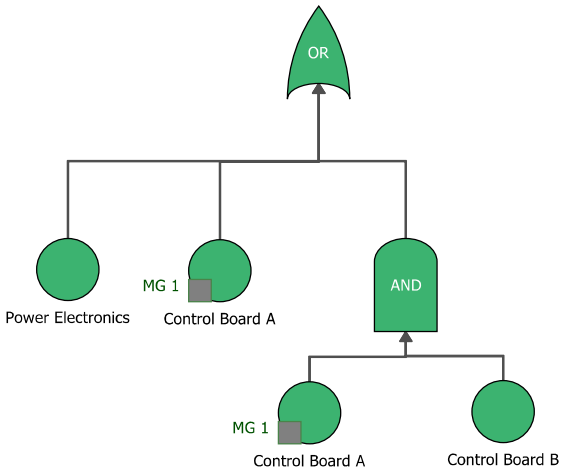

Fig. 1. FTD of the multi core case. Grey boxes represent mirrored components

Considering to use the rough sample data obtained from similar applications [1] and considering a ground fixed environment and 60°C as operating temperature it is possible to derive the behaviour of the two different diagrams as represented in Figure 6.

I can be noticed that the distributed board system, even if comprising a higher number of components results in a better steady state availability due to the temperature derating which is in the range 10%-30%.

TABLE I. BASIC CONSTANT FAILURE AND REPAIR RATES FOR AVAIALBILITY EVALUATION

SYSTEM	ELEMENT	FAILURE RATE [f/h]	REPAIR RATE [r/h]
UPS MAIN CONTROL BOARD & POWER INTERFACE	POWER ELECTRONICS	λ_E = **8.3809E-6**	0.1
	AC/DC CONTROL BOARD (B)	λ_B = **2,00264E-6**	0.1
	INVERTER AND STATIC SWITCH CONTROL BOARD (A)	λ_A = **2,8998E-6**	0.1

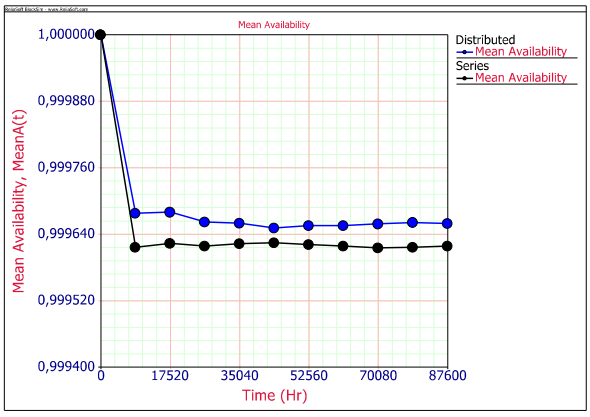

Fig. 6. Availability vs time of the distributed (multi core) and series (single core) configurations exploiting the FTD approach.

IV. MARKOV MODELLING AND SIMULATION RESULTS

Despite the results obtained in the previous section it is important to understand the changes that can be induced over the availability general trend once some temperature disturbance are applied to the operating environment.

To evaluate this behaviour it is possible to model the overall system as a traditional two state homogeneous Markovian model as shown in the literature. The equivalent failure rate will be the sum of the previously used failure rates as shown in Table I. If we then apply the same model to a failure rate which is increasing linearly over time simulating an increase of 3 degrees per hour of the environmental temperature, it is possible to notice has the system availability shown in Figure 7 drastically drops down up to 75% after 70 operating hours.

Considering to represent now the system of Figure 2 with a Markov diagram it is possible to use the state space representation shown in Figure 8.

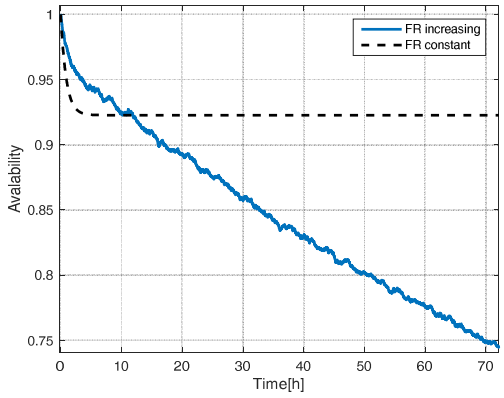

Fig. 7. Availability vs time of the single core solution once under constant and linearly increasing failure rates

It is then possible to compare the behaviour of the multicore structure with the single core one in terms of system availability.

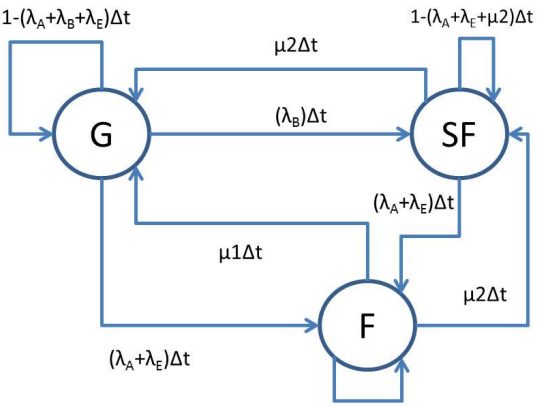

Fig. 8. Markov representation of the multicore distributed system. State SF takes into account a failure of the control board B section which does not compromise the system integrity

Results are shown in Figure 9, where it is possible to prove the gap between the two possible solutions if a repair rate μ = 0.1 r/h is assumed for the two state case.

In the three state case, as the one depicted in Figure 8, G identifies the working state or good condition, SF the first failure of the control board B which does not compromise the system mission, while F represents the failed state.

The differential equation system corresponding to the

diagram in Figure 8 is that of (1)

$$\begin{bmatrix} \dot{P}_G \\ P_{SF} \\ P_F \end{bmatrix} = \begin{bmatrix} -(\lambda_A + \lambda_B + \lambda_E) & \mu 2 & \mu 1 \\ \lambda_B & -(\lambda_A + \lambda_E + \mu 2) & \mu 2 \\ \lambda_A + \lambda_E & \lambda_A + \lambda_E & -(\mu 1 + \mu 2) \end{bmatrix} \begin{bmatrix} P_G \\ P_{SF} \\ P_F \end{bmatrix} \quad (1)$$

Two repair rates are assumed for this scenario, μ2=0.1 r/h and μ1 which is double with respect to the previously mentioned μ.

Despite of this penalizing choice the multicore model seems to offer better availability performance than the two state one.

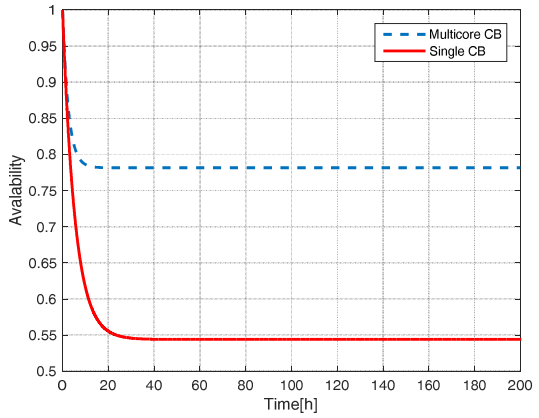

Fig. 9. Availability comparison of the multicore vs. the single core representation.

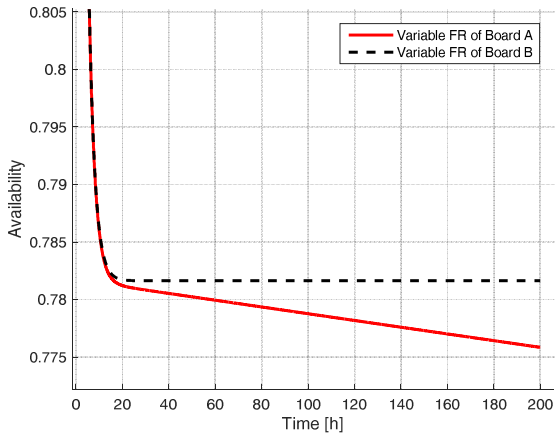

Fig. 10. Multicore availability diagram considering both a steady failure rate and a linearly increasing one. Such increase can be used to model a gradual warm up of the control board (A and B sections)

Figure 10 finally represents the situation where both a constant and a linearly growing failure rate are applied to the model described in Figure 8. Here again the behaviour of the steady failure rate would be preferred even if the increasing failure rate due to environmental variations is more likely to be experienced in an actual application.

V. CONCLUSIONS

In this paper the authors took into consideration two possible configurations for double conversion uninterruptible power supplies showing how these two systems can be represented and modelled both in terms of reliability block diagrams and through the use of Markov models. It has been shown that despite the increased number of components, the distributed solution is to be generally preferred due to the fact it can be considered in some cases fault tolerant and that the temperature derating achievable by such solution highly compensates the straight reliability decrease. The study has been carried out both considering constant failure rates and linearly growing ones in order to simulate local temperature gradients.

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