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Improvement in the efficiency of DC/DC power converters by controlling the switching frequency

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***Abstract* – In recent years DC/DC converters are becoming one of the most diffused power converter because of the spreading of renewables and storages. New topologies of DC/DC converters have been proposed to improve the energy efficiency. Anyway, in many applications the most diffused are always the traditional hard switching configurations for which some tricks are introduced in order to increase the efficiency. Usually, the switching frequency is considered a parameter to be kept low in order to reduce the losses. In this paper, the efficiency variation of a power converter with the switching frequency is deeply analyzed. From the reported analysis, it results that there is a particular frequency for which the power converter operates at its maximum efficiency. Moreover, for real converters, this frequency is in a range good also to ensure a good quality of the output voltage. In particular, the case of a SEPIC converter designed for PV application is taken into account and the optimal switching frequency is around 20 kHz. The proposed analytical approach has been verified by means of numerical results.**

I. INTRODUCTION

In recent years the wide diffusion of renewable energy sources (RES) has been facilitated by the big progresses obtained by power electronics. Several sources as photovoltaic (PV) systems, fuel cells and all the electrochemical storages are DC sources. Moreover, AC/AC power converters are often implemented by means of a DC stage. For this reason, DC/DC power converters have been deeply studied in recent years and innovative topologies have been proposed. The principal mission of DC/DC converters is to adapt different DC voltage level implementing, at the same time, algorithms for the optimization of the source (such as maximum power point tracking for PV).

During the design phase, reliability and cost of DC/DC power converters are of great concern to designers who seeks the satisfaction for the customer and manufacturer. While the cost is essentially connected only with the number and kind of components used, a failure has always been the fundamental concept of any reliability assessment. There is, however, a wide confusion concerns the exact definition of the failure. IEC60050-191 [1] definition of failure is the termination of the ability of an item to perform a required task. However, it is not necessary for a failure to terminate operation of the equipment. A performance drop below the warranty limits is considered a failure as well. In general, the functional elements of DC/DC power converter may be repeatedly, rearranged or its capability may be changed to achieve the required reliability level. In this respect, a high efficiency is the keyword to keep the function of the DC/DC power converter meets the warranty limits.

The choice of components of a higher quality (and price) of a certain topology can improve the efficiency only because their losses are significant for the efficiency of the whole converter. Indeed, in many configurations, losses in passive components could be significant if compared with switching devices. A deep analysis to understand if the switching devices could be replaced to improve the efficiency of a converter is often necessary.

As a second step, it is possible to act on the switching frequency to improve the efficiency of the converter taking into account also the constraints about the quality of the output voltage. It is a common thinking that increasing the switching frequency the output voltage improves but the losses increases. While this is true for switching losses that are linearly dependent on the switching frequency, it is not true for conduction losses not only in the switching component but also in passive components. At the beginning of '90 the switching losses were dominant in the phenomena and the global efficiency of power converters was a decreasing function of the switching frequency [2].

Anyway, the increasing of the switching frequency implies a reduction of the current ripple and, therefore, a reduction in the conduction losses of all the devices, active and passive, of the converters. For this reason, it exists an optimal switching frequency from an efficiency point of view and, often, this value is high enough to ensure a good quality of the output voltage.

In literature, few efforts have been conducted in order to optimize the switching frequency of the DC-DC power converters. The authors in [3] proposed an analytic method on on-chip buck converter to evaluate the frequency dependent losses. Optimization of the frequency is done independent of the load current and only by using power losses in MOSFET and inductor. However, the impact of frequency changes on diode is not considered. In another

work [4], the importance of keeping the efficiency of the DC-DC power converters in different ranges of load is taken into account. The VFC could generate the optimum value of the frequency due to the load current. The SPICE based model is used to do a comparison between the efficiency values achieved by constant frequency and adaptive frequency design. Meanwhile, our presented work provides more details, analytically and numerically, on the change of frequency on each important component power loss, passive or active. The achieved results are very important for assuring the availability and enhancing the reliability assessment techniques of power converter, along its life cycle.

In this paper, an analytical approach to estimate the optimal switching frequency will be discussed. Then, taking into consideration the SEPIC converter, that is a good topology for some applications [5]-[7], the proposed analytical approach is verified by comparing the analytical results with numerical ones. It will be shown that the optimal switching frequency, for a SEPIC converter designed for PV application, whose power is around 100 W, is around 20 kHz.

II. ANALYTICAL PROCEDURE FOR EFFICIENCY EVALUATION

As is well known, the efficiency of a power converter, defined as the ratio between the output and the input power can be calculated also as the ration between the output power and the power obtained by adding to the output power all the losses. It is worth to note that traditional models of DC/DC power converters do not take into account the influence of switching losses on the input/output characteristic of the converter itself. Therefore, calculating the efficiency as the ratio between output and input power is correct for experimental setup but is not correct for numerical models. In the following, the losses in each component, active and passive will be evaluated in order to study the variation of the global efficiency with the switching frequency. Moreover, looking at the losses of each component can help in individuating the *weak* element to be changed in order to improve the efficiency of the converter or monitored for reliability issues.

In order to calculate the losses of active and passive elements of a DC/DC power converter the following assumptions will be made:

a) Inductive currents are linearly variable in a switching period (i.e. high order variations are neglected and voltages across the inductances are considered constant during a switch state);
b) Capacitive voltage are linearly variable in a switching period (i.e. high order variations are neglected and currents in the capacitances are considered constant during a switch state);
c) Losses in the capacitances are neglected (i.e. losses in the equivalent series resistance of capacitors are much lower then losses in inductances and in switching components);
d) Switching losses are estimated by considering a linear increasing of the current with constant voltage during turn on and a linear increasing of the voltage at constant current during turn off.

With these assumptions, in the following, the losses occurring in inductances, in diodes and in switching components are modeled. For sake of simplicity reference to a case with only one switching component will be done but the presented procedure can be easily extended to power converters with more than one switching component and more than one duty cycle.

A. Inductances power losses

Losses in inductances are due to parasite resistances associated to the winding of the inductances. Because of hypothesis a), the current in the inductances during a switching period can be represented as in Fig. 1.

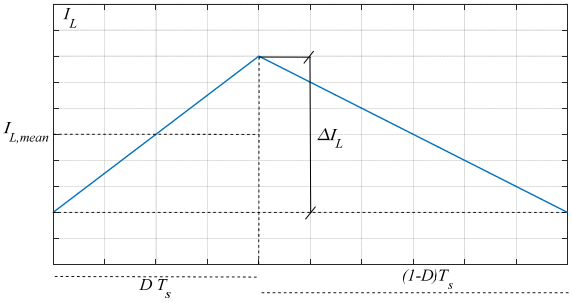

Fig. 1. Current in inductances

The losses can be, therefore, expressed as:

$$P_L = \frac{1}{T_s}\int_0^{DT_s} R_L\left(I_{L,mean} - \frac{\Delta I_L}{2} + \frac{\Delta I_L}{DT_s}t\right)^2 dt + \frac{1}{T_s}\int_0^{(1-D)T_s} R_L\left(I_{L,mean} + \frac{\Delta I_L}{2} - \frac{\Delta I_L}{(1-D)T_s}t\right)^2 dt \quad (1)$$

where T_s is the switching period, R_L is the resistance of the inductance and D is the duty cycle.

B. Diode power losses

Diode power losses are, essentially, conduction losses due to the voltage drop across the diode when it is in conduction mode. Usually, in DC/DC power converters, the current in the diode, when it is turned on, can be expressed as a linear combination of currents in inductive branches. Usually the diode is in conduction mode only in one of the two switching state, and in particular during the off time of the main switch. Its current can be represented as in Fig. 2.

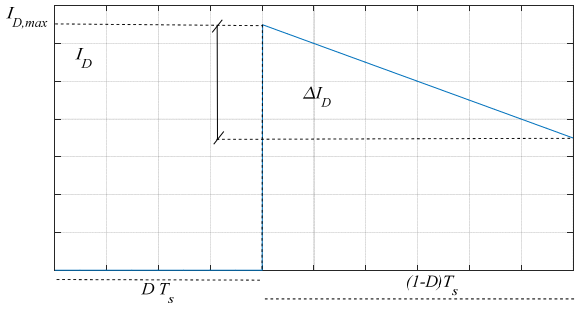

Fig. 2. Current in diodes

The voltage drop across the diode, when it is conducting, can be approximated with the sum of a constant term and a linear one:

$$V_D = V_{0D} + R_D I_D \tag{2}$$

where V_D is the voltage across the diode, V_{0D} is the forward voltage at zero current, R_D is the diode resistance and I_D is the current drawn by the diode. With reference to the diagram of Fig. 2 and taking into account (2) the power losses of the diode can be, definitely, expressed as:

$$P_D = \frac{1}{T_s}\int_0^{(1-D)T_s} V_{0D}\left(I_{D,\max} - \frac{\Delta I_D}{(1-D)T_s}t\right)dt + \\ + \frac{1}{T_s}\int_0^{(1-D)T_s} R_L\left(I_{D,\max} - \frac{\Delta I_D}{(1-D)T_s}t\right)^2 dt \tag{3}$$

C. Power switch losses

Power switch losses can be divided in conduction and switching losses. The conduction losses can be estimated similarly to diode losses. The current in the power switch is present only during the turn on and, usually, can be expressed as sum of currents in inductances. Its typical behavior is reported in Fig. 3.

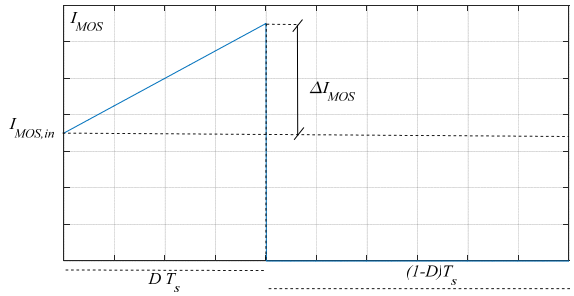

Fig. 3. Current in the power switch

Considering a MOSFET as power switch, during conduction its voltage drop is linearly dependent on the current therefore the losses can be expressed as function of the internal resistance. In particular they are:

$$P_{MOS,c} = \frac{1}{T_s}\int_0^{DT_s} R_{MOS}\left(I_{MOS,in} + \frac{\Delta I_{MOS}}{DT_s}t\right)^2 dt \tag{4}$$

where R_{MOS} is the internal resistance of the MOSFET.

According with technical literature [8], switching losses can be expressed as:

$$P_{MOS,sw} = \frac{1}{2T_s}\left[V_{MOS}(T_s)I_{MOS,in}\,t_r + \right. \\ \left. + V_{MOS}(DT_s)(I_{MOS,in} + \Delta I_{MOS})t_f\right] \tag{5}$$

where t_r and t_f are respectively the rise and the fall time of the MOSFET.

It is worth to note that in all the reported equation the current variations inside the switching period, represented in the figures, are function of the switching frequency. The higher is the switching frequency, the lower will be the current ripple and therefore, for the same load, all the conduction losses will decrease by increasing the switching frequency. On the contrary, the switching losses are a linear increasing function of the switching frequency as expressed in (5).

III. SEPIC CONVERTER

The model analyzed in the previous section will be applied to SEPIC converter. This converter has been chosen because, among the converters using only one power switch, it is one of the most versatile because it is capable of supplying an output voltage higher or lower than the input one. Moreover, the output voltage is not with inverted polarity with respect to the input voltage and this gives other advantages in some applications. Anyway, the analytical procedure proposed in the previous section can be easily extended to other power converters.

SEPIC electrical scheme is reported in Fig. 4.

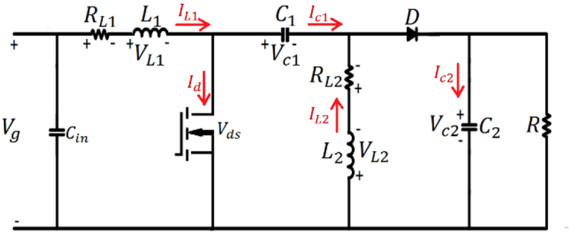

Fig. 4. SEPIC converter

When the power switch is turned on, the electrical equivalent circuit is reported in Fig. 5.

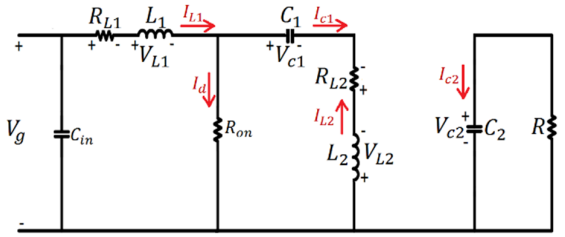

Fig. 5. SEPIC equivalent circuit during on time

It is easy to verify that, during on time it results:

$$\begin{cases} I_{C_1} = -I_{L_2} \\ I_{C_2} = -\dfrac{V_{C_2}}{R} \\ V_{L_1} = -R_{L_1} I_{L_1} + V_g - R_{on} I_d \\ V_{L_2} = -R_{L2} I_{L2} + V_{C_1} - R_{on} I_d \end{cases} \tag{6}$$

When the switch is turned off the equivalent electrical circuit of the SEPIC converter is that reported in Fig. 6.

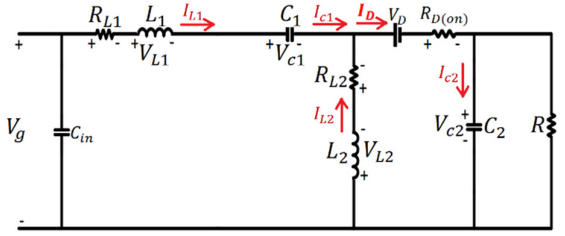

Fig. 6. SEPIC equivalent circuit during off time

It is easy to verify that , during off time it results:

$$\begin{cases} I_{C_1} = I_{L_1} \\ I_{C_2} = I_{L_1} + I_{L_2} - \dfrac{V_{C_2}}{R} \\ V_{L_1} = -R_{L_1} I_{L_1} + V_g - V_{C_2} - R_{D(on)} I_D - V_D - V_{C1} \\ V_{L_2} = -V_{C_2} - R_{D(on)} I_D - V_D - R_{L_2} I_{L_2} \end{cases} \tag{7}$$

In order to make easier to understand the working operation, the typical evolution of the interesting quantities is depicted in Fig. 7.

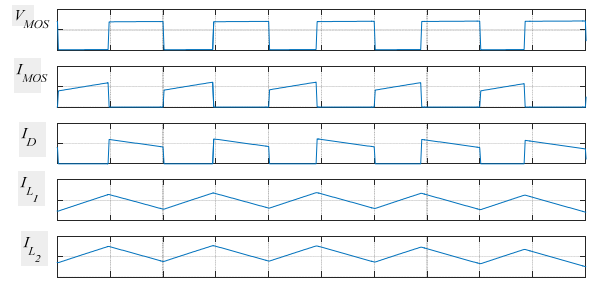

Fig. 7. SEPIC currents and voltages during five periods.

At steady state, the mean values of the inductance voltages and of the capacitance currents has to be zero. Neglecting the voltage oscillation across the capacitances, multiplying (6) by D and (7) by (1-D) and summing, after some calculations, it is possible to obtain:

$$\begin{cases} I_{L_2,mean} = \dfrac{V_{C_2}}{R} \\ I_{L_1,mean} = I_{L_2,mean} \dfrac{D}{1-D} \\ \Delta I_{L_1} = \dfrac{D V_g T_s}{L_1} \\ \Delta I_{L_2} = \dfrac{D V_g T_s}{L_2} \\ I_{D,\max} = I_{L_1,mean} + I_{L_2,mean} + \dfrac{\Delta I_{L_1} + \Delta I_{L_2}}{2} \\ \Delta I_D = \Delta I_{L_1} + \Delta I_{L_2} \\ I_{MOS,in} = I_{L_1,mean} + I_{L_2,mean} - \dfrac{\Delta I_{L_1} + \Delta I_{L_2}}{2} \\ \Delta I_{MOS} = \Delta I_{L_1} + \Delta I_{L_2} \\ V_{MOS}(T_s) = V_{MOS}(DT_s) = \dfrac{V_g}{1-D} \end{cases} \tag{8}$$

IV. NUMERICAL VALIDATION

In order to validate the analytical analysis discussed in section III, a numerical model environment has been built in Simulink/SimPowerSystem. The data of the SEPIC converter used for the simulations are reported in Table 1.

Table 1. Main data of the SEPIC converter

Input/output data	V_g	40 V
	R	4.4 Ω
Inductors	*Inductance*	220 µH
	Resistance	62 mΩ
Capacitors	C_1	300 µF
	C_2	940 µF
Mosfet	*Type*	IXFH 40N30
	R_{MOS}	85 mΩ
	t_r	60 ns
	t_f	45 ns
Diode	*Type*	FFPF10UP20S
	V_D	0.6 V
	$R_{D(on)}$	55 mΩ

By means of the SimPowerSystem model it is possible to calculate the conduction losses of each component. On the contrary, it is not possible to use the Mosfet model to evaluate the losses during the switching transient. For this reason, in order to calculate the switching losses, the scheme reported in Fig. 8 has been implemented. For computing the turn-off (turn-on) losses, the voltage (current) value just after the commutation is multiplied for the current (voltage) value just before the gate pulse. According to (5), this product is weighted for the ratio between the rise time t_r (fall time t_f) and the switching period T_s and multiplied by 0.5.

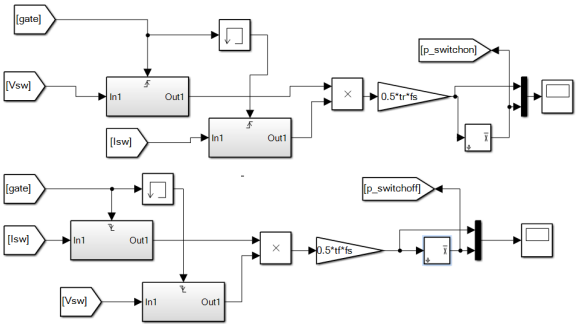

Fig. 8. Scheme for the estimation of switching losses

In order to estimate the variation of the losses in each component for different output powers, a feedback chain acting on the duty cycle for controlling the output power has been used. The losses have been calculated after a period of time long enough to make the system working at steady state. Moreover, in order to eliminate oscillation due to the control, the mean value calculated over 100 switching periods has been taken into account. In Fig. 9, Fig. 10, Fig. 11, Fig. 12 and Fig. 13 the losses of the components versus frequency variation are reported. The losses are analytically calculated (continuous lines) and compared with the simulated one (x markers) for 4 different load conditions of the converter (25%, 50%, 75% and 100%). From the analysis of the figures, a good agreement between the analytical model and the numerical data can be found. The maximum error is obtained for the minimum switching frequency equal to 5 kHz. This can be explained taking into account that the feedback control chain is not able to keep the converter output power rigorously constant in this condition. In fact a small oscillation is still present and causes the error in the numerical estimation of the losses.

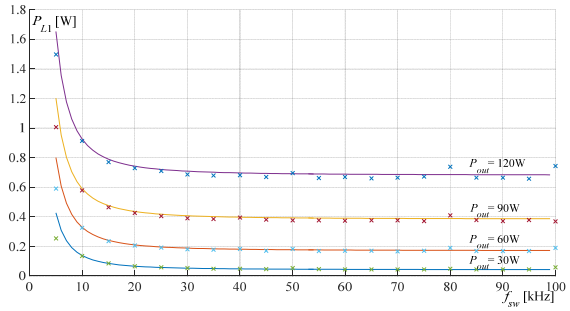

Fig. 9. Conduction losses in the inductor L_1

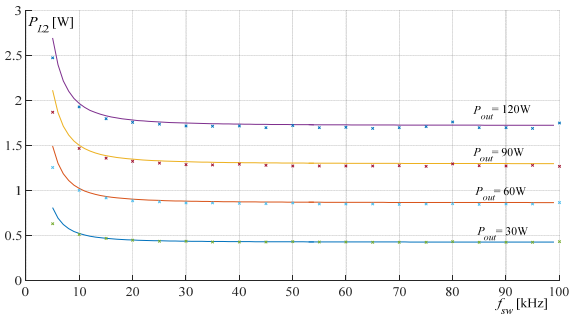

Fig. 10. Conduction losses in the inductor L_2

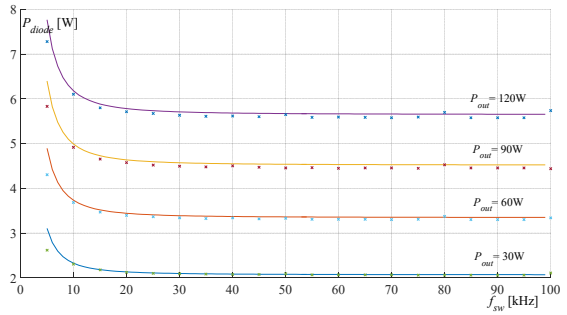

Fig. 11. Conduction losses in the diode

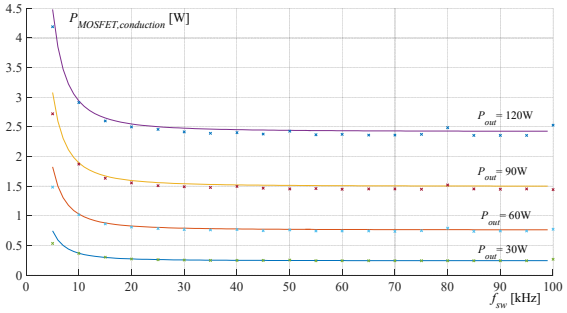

Fig. 12. Conduction losses in the MOSFET

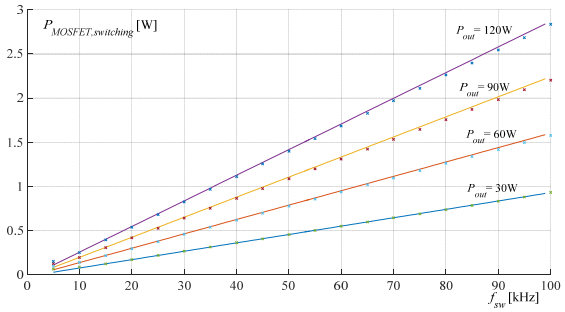

Fig. 13. Switching losses in the MOSFET

As it could be expected, all the conduction losses reduces with the switching frequency while the switching losses linearly increase. Anyway, the reduction of the conduction losses is significant at low frequencies and non-influent at high switching frequencies. This is why the global efficiency is maximum at a switching frequency equal to 20 kHz as can be observed in Fig. 14. The choice of a switching frequency lower than 20 kHz is not justified neither for voltage quality issues nor for efficiency improvements.

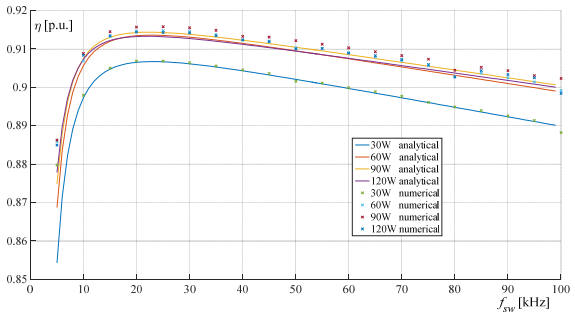

Fig. 14. Converter efficiency versus frequency

The performed analysis can be very interesting also to understand which is the most critical component of the converter from the efficiency point of view. In this case, for example, in order to improve the global efficiency it is much more convenient to change the power diode than the power MOSFET. Indeed, at full power and at the best switching frequency, the power losses of the diode are double than those of the MOSFET.

The components of power converter exhibit thermal and operational stresses that result in a degradation in the output power. This analysis allows to identify the minimum switching frequency required for optimizing the efficiency thus minimizing the stress of the components. A further advantage can be gained from the introduced analysis on improving the reliability of DC/DC power converter during the operational phase of its life cycle. This can be conducted by applying the same analysis procedures to calculate the new power losses and determine the new optimal frequency that ensures the operation of power converter above the guaranteed value in case of component replacement.

V. CONCLUSIONS

During the design phase of DC/DC power converter, elements can be replaced or reconfigured in order to achieve a higher reliability or performance. In this work, an analysis allowing to determine the power losses as function of the switching frequency has been proposed. This analysis allows to define the minimum switching frequency optimizing the converter efficiency. This allows to reduce the stresses of the components thus improving the system reliability.

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