MEASUREMENT OF ANALOG SIGNALS BY MEANS OF THE IEEE Std 1149.4 MIXED-SIGNAL TEST BUS

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Abstract - *Architecture and properties of the virtual probes created by the analog modules of the IEEE Std 1149.4 test bus are presented. Capabilities of the bus co-operated with the CIM 97 Multidiatest Measurement System in the area of the analog signal were investigated on the examples of the resistance, capacitance and inductance measurement. Application of the bus, when access to analog nodes of the circuits is limited and the analytical method is needed for supporting of testing, is discussed.*

Keywords - measurement, analog signal, test bus

1. INTRODUCTION

Success of the IEEE Std 1149.1 test bus [1] in VLSI digital circuit testing caused that the conception of the extension of the bus architecture for analog circuits measurement has appeared. In 1999, after some years of discussion, the IEEE Std 1149.4 mixed-signal test bus for common test operations of analog and digital parts of circuits was confirmed [2].

The structure of the compliant to IEEE Std 1149.4 chip is presented in Fig. 1.

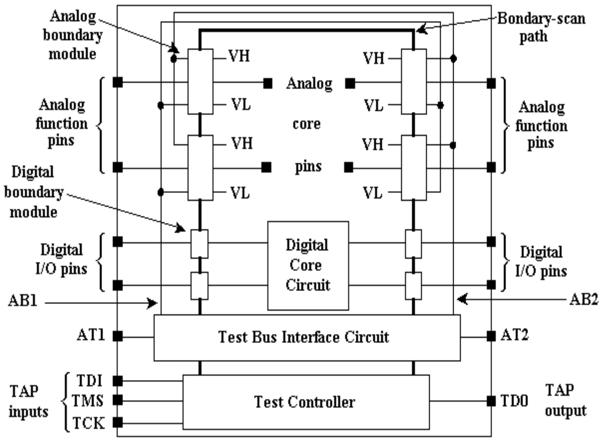

Fig. 1 - Architecture of IEEE Std P1149.4 chip.

Analog Boundary Modules (ABMs), Test Bus Interface Circuit (TBIC), analog internal buses (AB1, AB2) and external pins (AT 1, AT2) were added to the IEEE Std 1149.1 test bus structure. They create the virtual probes for measurement of analog signals.

2. ANALOG VIRTUAL PROBES

2.1.Architecture

As it is illustrated in Fig. 2 and Fig. 3, ABM's and TBIC are the switching networks. The analog functional pin can be connected to AB1 and AB2 internal buses and to dc voltages (VH, VL, VG). One-bit digital information about the voltages appearing at analog function pins with respect to a reference voltage Vref is captured and than become TDO signal.

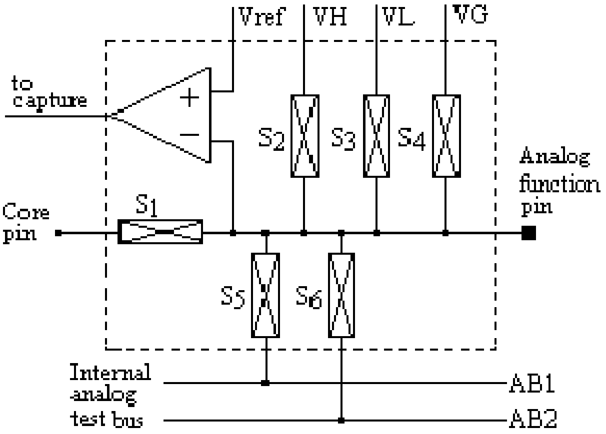

Fig. 2 - Switching structure of AMB.

TBIC distributes analog signals passing through AT1 and AT2 and enables isolation of the internal analog buses in the chip when they are not in use. TBIC provides also calibration of the analog test bus and testing of the integrity of the bus.

The operation of the switches is determined by the content of the boundary-scan register, which is loaded by Test Access Port (TAP).

Depending on the data configuring test circuits, ABMs and TBIC create the analog virtual probes between nodes of the Circuits Under Test (CUT) and measurement equipment connected to AT1 and AT2 test pins. The analog probes are used only in EXTEST and PROBE modes of the bus operation.

In EXTEST mode, ABM's are put into the core disconnect state (S1 opened). Then, the probes carry analog signals between analog functional pins and analog port of the bus. It facilitates testing of the elements placed outside the chips equipped with the bus.

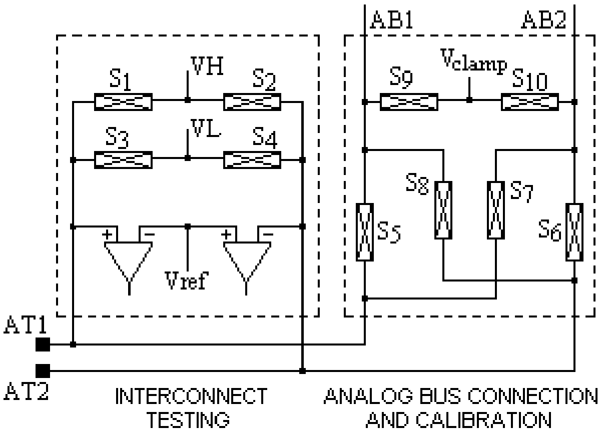

Fig. 3 - Switching structure of TBIC.

In PROBE mode, the analog functional pins are connected to core (S1 closed). CUT can work normally and some parameters of the signal at the analog nodes can be measured. The probes can also be used to provide a stimulus signal to the nodes.

2.2. Properties

Investigations of the probes created in MNABST-1 IEEE 1149.4 test chips made by Matsushita Company [3] were done by means of CIM 97 Multidiatest Measurement and Diagnostic System designed in Technical University of Gdańsk [4].

The structure of probes is presented in Fig. 4 (only the TBIC and ABM switches closed during analog measurement are shown). TBIC and ABM switches of MNABST-1 are made as the quad analog switches controlled by S external signals. Values of the switches' resistance define by the producer are: S00-100 Ω, S01-400 Ω, S10-1.6 kΩ, S11-6.4 kΩ. Measurements were done for different control signals.

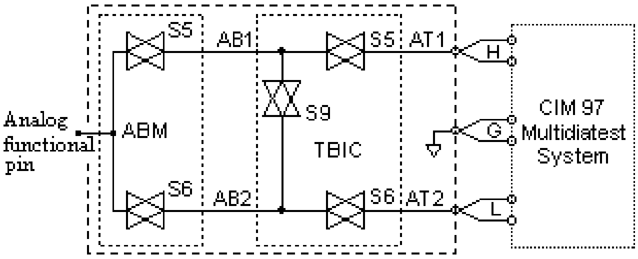

Fig.4 - Virtual probes created by the IEEE Std 1149.4 test bus.

Resistance versus voltage and frequency of these probes in the MNABST-1 chip were measured in two situations:
"measurement" - S5 and S6 switches are closed, S9 switch is opened,
"calibration" - S5, S6, S9 switches in TBIC are closed, all others are opened.

The results of investigations are presented in Figures 5, 6, 7. Resistances of the probes are significant. The values can be comparable with the resistances of CUT and depend on the dc voltage that appears on the switches.

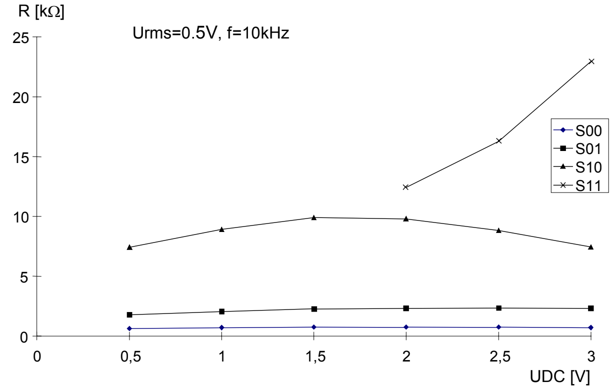

Fig. 5 - Resistance of the analog virtual probes.

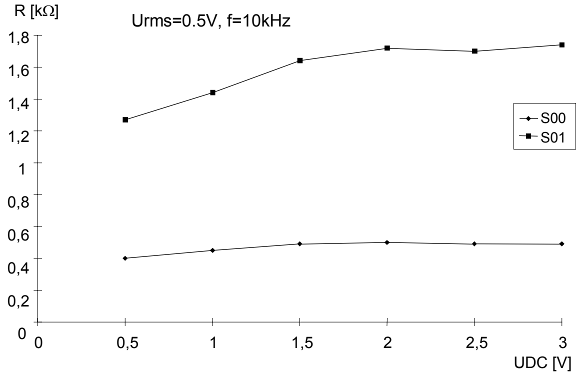

Fig. 6 - Resistance of the analog test bus in calibration mode.

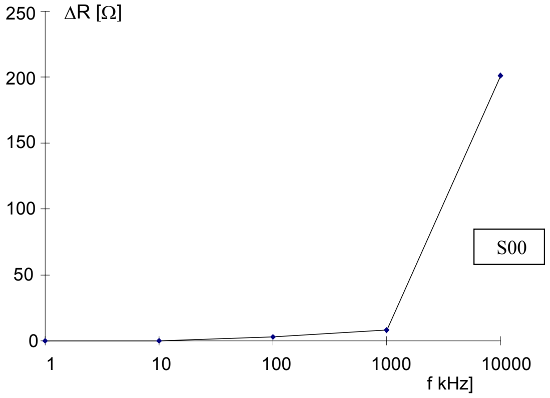

Fig. 7 - Resistance versus frequency of the analog virtual probes.

The results of investigation of the probes' resistance versus frequency show that measurement frequency must be limited because parasitic inductance dominates above some frequency.

The results of the leakage made in EXTEST mode show that the differences between I_{AT1} and the current flowing in external resistance in comparison with I_{AT1} are about 1 %. The leakage does not depend on the impedance of the switches. It depends on the current forced in AT1 input and on the value of external resistance. Leakage currents cause the systematic measurement error which can be reduced in calibration mode of the bus.

Parameters of AT2 measurement line of the bus were investigated with regard to non-linear distortions. Measurements were been done directly on analog function pins and on AT2 pin of the bus. The results for 1 kHz frequency are presented in Fig. 8. The distortions are small but the difference between h_{AT2} and h_{out} is visible.

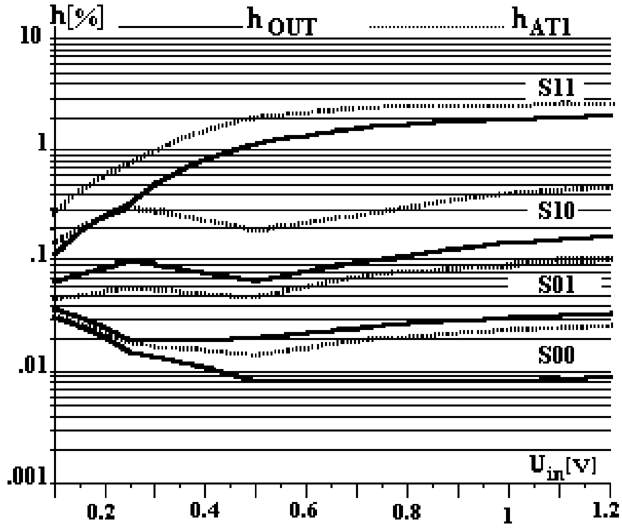

Fig. 8 - Non-linear distortions of ABM in MNABST-1

An important issue is the influence of ABMs' switches placed between the analog core and analog functional pins on normal work of the circuit. If the non-linear distortions are essential, application of the bus with investigated types of CMOS switches requires adding extra buffers or ABMs cannot contain switches placed between cores and analog functional pins.

3. MEASUREMENT

The MNABST-1 test chips are built like the chip presented in the Fig.1. They have got 15 identical ABMs. They don't contain the analog cores and enable direct access to core pins and analog functional pins of the ABMs. Thanks to that, realization of many measurement experiments was possible [5,6].

Structure and performance of the analog measurement probes created by the bus impacts on the measurement strategy. Inconstancy of the switches' resistance caused that the principle is a current stimulus at AT1 pin and voltage measurement at AT2 pin. Some examples of the measurement configurations of the bus are shown in Fig. 9.

Measurement of the R, C and L elements via test bus were done using the CIM-97 Multidiatest Measurement and Diagnostic System which contains the HP4192A Impedance Analyser.

Accuracy of measurement of the resistors' values was 0.2% to 6,3%, according to the forced current (1mA to 0.125mA respectively).

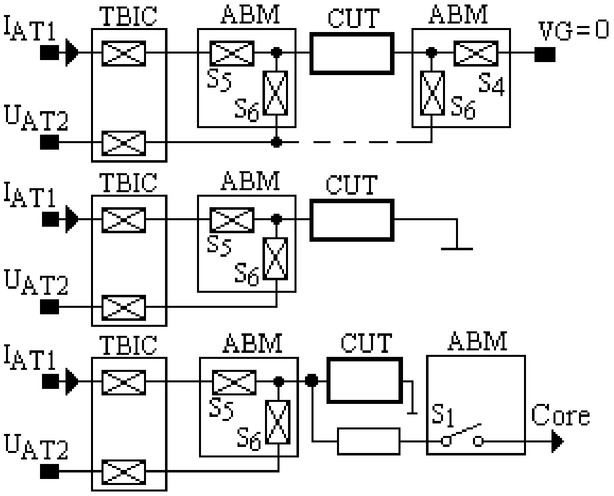

Fig. 9 - Measurement configurations of the analog bus.

Measurements of the C and L were done in series and parallel substitute diagrams of impedance for two values of the switches' resistances of the chip. The results of measurement of the 33 pF capacitor are correct for frequency from 1 to 10 kHz in series and parallel substitute diagrams (Fig. 10) and do not depend on the switches' resistance. But, for 10 pF capacitor (Fig. 11), results are different for different switches.

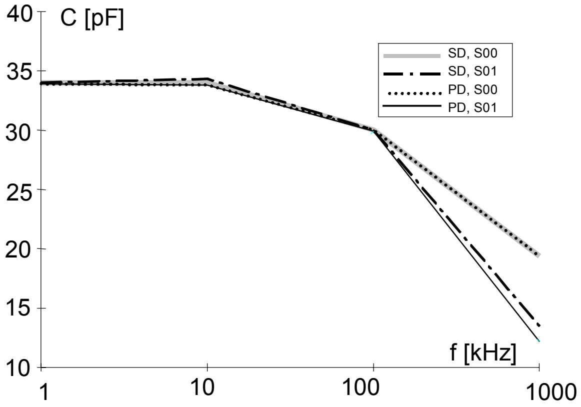

Fig. 10 - Results of the C = 33 pF capacitor measurement in series (SD) and parallel (PD) substitute diagrams for different values of the analog bus switches (S00, S01).

The results show that accuracy is better, if series substitute diagram is chosen. It depends on relation of Zx impedance modulus to the summarized switches' resistance. In general, low measurement frequency and small resistance of the switches are advantageous, but lowering of measurement frequency is limited because of the disturbances introduced

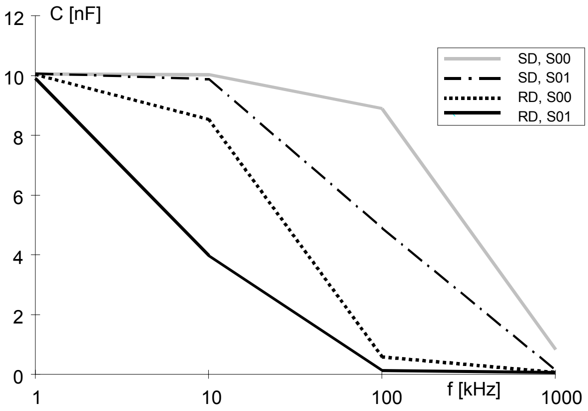

Fig. 11 - Results of the C=10nF capacitor measurement in series (SD) and parallel (PD) substitute diagrams for different values of the analog bus switches (S00, S01).

by the control signals of the bus. Above suggestions are correct for measurement of inductance (Fig.12).

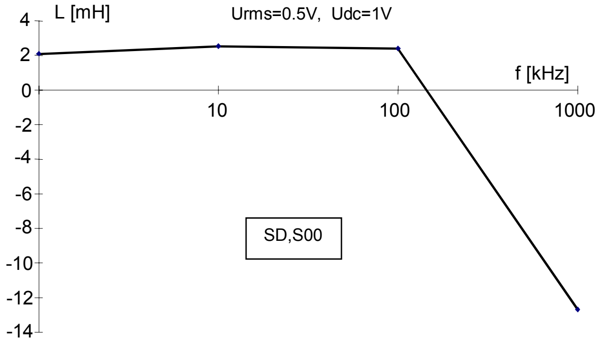

Fig. 12 - Results of L=2.31mH induktor measurement in series (SD) substitute diagram.

Access of the bus to nodes of the extended analog networks placed between ABMs of IEEE Std 1149.4 compliant chips is often limited to input and output of the networks. Then, the support by analytic methods becomes necessary for parametric testing. Known methods based on admittance model of circuit and on the properties of linear equations can be used if measurement could be made by means IEEE Std 1149.4 bus. One of them is the method based on the bilinear transformation [7]. The idea is the measurement of two (or more) independent circuit functions (for example: input (output) impedance, voltage gain) and the determination of the changes in components' values of the CUT with respect to the nominal values which are presented as the family of the plots. The application of this method for testing of the low pass analog filter using the mixed-signal test bus did not introduce any essential errors to the results of the measurements in comparison with the direct measurements. Question is the choice of measurement frequency optimal for resolution of the results and for application of the bus.

4. CONCLUSION

Investigation has shown that the structure of the bus impacts on the results of the analog signals' measurement. It should be taken into account during the selection of levels and frequency of the measurement signals, when the bus is used. The proper measurement strategy can improve accuracy of the results obtained by means of the bus.

ACKNOWLEDGEMENTS

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