NON-LINEAR MODEL BASED CALIBRATION OF D/A CONVERTERS

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Abstract - *Various error sources cause linearity errors which degrade the performance of D/A converters. The paper presents a non-linear model to describe multiplying D/A converters. A Walsh transformation based diagnostic tool is used to determine the model parameters. Based on this model, a calibration scheme is derived, in order to compensate the non-linear behaviour of the converter. Practical applicability of the proposed method is shown by measurements performed on a custom designed test circuit.*

Keywords - bit intermodulation, calibration of converters, digital-to-analog conversion, testing data converters, Walsh transformation

1. INTRODUCTION

There is a growing demand on highly linear D/A converters, as the significance of digitally controlled instruments and devices and complex modulations used for telecommunication is rapidly increasing. The linearity of D/A converters is highly dependent on - and limited by - the IC manufacturing processes.

However, the overall study of the converter's linearity can be done without going into technology-level analysis. The paper will determine a non-linear model for a multiplying D/A converter, that is used to calibrate it. The calibration of multiplying D/A converters is more difficult than the calibration of commonly used fixed reference converters, because the non-linearities must be described by input signal independent parameters, to allow for their correction.

The only needed *a priori* information is the *integrated non-linearity diagram* (INL) of the data converter. The INL is the error between the real and ideal output characteristic of the converter.

2. LINEARITY ERRORS OF D/A CONVERTERS

A perfectly linear D/A converter can be described by (1). Note that the global offset and gain errors do not have effects on the linearity properties of the converter, as long as they are not code dependent.

$$V_{out} = V_{ref} \cdot \sum_{i=1}^{N} \frac{b_i}{2^i} \tag{1}$$

The linearity errors may have multiple causes, and these errors are topology and sometimes process dependent. The most usual reason for having a non-linear distortion of a converter is that the binary weights of the individual bits are not perfect. For example, if the converter uses the well-known R-2R ladder to generate binary weighted currents, resistor mismatches distort the binary division [1]. Although the imperfection will cause a linearity error, the *superposition principle* will still hold. This means that the contribution of a bit to the output signal is independent from the states of the other individual bits and therefore the superposition of the erroneous binary weighted currents - regarding to the input code - will give the actual output current [1]. In that case, the linearity of the device can be fully described by the bit error terms ε_i for any digital input combination:

$$V_{out} = V_{ref} \cdot \sum_{i=1}^{N} \left[b_i \left\{ \frac{1}{2^i} + \varepsilon_i \right\} \right]. \tag{2}$$

Unfortunately, there are some errors which can not be described by the above formula. For example, the interactions between switches can produce non-linearities for which the superposition no longer holds. These errors are the so-called *superposition errors*. In that case a thorough test is needed to determine the worst case errors.

Extending the model of the converter (2) to cover the static superposition non-linearities leads to a more accurate model of the circuit:

$$V_{out} = V_{ref} \cdot \left(\sum_{i=1}^{N} \frac{b_i}{2^i} + \sum_{i=1}^{N} b_i \varepsilon_i + \sum_{i=1}^{N} \sum_{j=i}^{N} b_i b_j \varepsilon_{ij} + \sum_{i=1}^{N} \sum_{j=i}^{N} \sum_{k=j}^{N} b_i b_j b_k \varepsilon_{ijk} + \ldots + b_1 \ldots b_N \varepsilon_{1\ldots N} \right) \tag{3}$$

This model incorporates the effect of various switch interactions, and any other source of non-linearity. The ε terms describe the different interaction mechanism that span the superposition error.

In practice, the superposition errors are so small, that the linear error model (2) is often valid. However, as the resolution or the required linearity increase, the effect of the superposition errors can no longer be neglected.

3. ANALYZING THE LINEARITY ERRORS

3.1 Walsh functions

The time domain analysis of the non-linearity is useful to determine the specifications of the converter, but it is far less efficient to evaluate the error sources. This is especially true

for superposition errors, which are easy to detect but whose source is almost impossible to trace. However, if the analysis is made in a transformed space, where the cumulative errors can be spread into orthogonal error components, it becomes possible to identify the error sources. The Walsh transform exactly performs such a decomposition [2]. The Walsh functions are denoted as $W(n, t)$, where n is the sequence number of the Walsh function, and t denotes the time. For $m = 8$ the Walsh kernel functions are plotted on Fig. 1. The Walsh functions compose an ortonormal basis of functions. The transformation matrix contains the binary represented Walsh functions, and it is symmetrical. In the next sections,

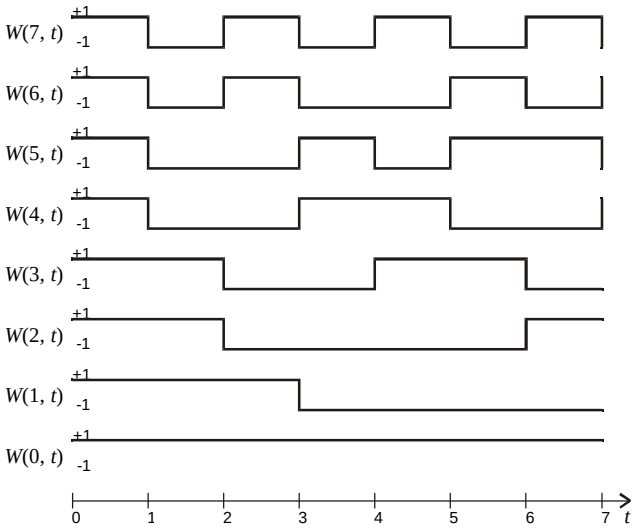

Fig. 1. Walsh functions for $m = 8$

the error functions of bit errors and higher-order interactions will be studied, and the Walsh decomposition of these functions.

3.2 Bit errors

As said before, a common linearity error of converters is that the bit weightings are not ideal. If this non-ideality is assumed to be dominant, only linearity errors are present, and superposition errors are negligible. The number of error sources then equals to the number of bits, and therefore from N appropriate measurements are sufficient to derive the real transfer function of the converter.

First, the bit errors will be studied. If a bit is switched on, then an erroneous current value appears at the output. This means that if there is only one bit error, the *integrated non-linearity diagram* looks like a square wave whose amplitude equals to the amplitude of the error and with a frequency which depends on the position of the erroneous bit (Fig. 2)[1]. Fortunately, a square wave is one of the orthogonal basis functions of the transformation (Fig. 1). The only problem is that the Walsh functions are only orthonormal if they are defined over the set (+1, -1). Therefore an offset ($W(0, t)$) is also needed to decompose the error function to Walsh functions, and the amplitude of the Walsh sequences will be the half of the amplitude of the error. If the i^{th} ($i = [1, \ldots, N]$) bit has an error, it will generate a Walsh component at sequence $2^i - 1$ and one at sequence zero. Hence the bit errors are easily detectable in the Walsh

1. $f(x_i)$ value is plotted as a line from x_i to x_{i+1}

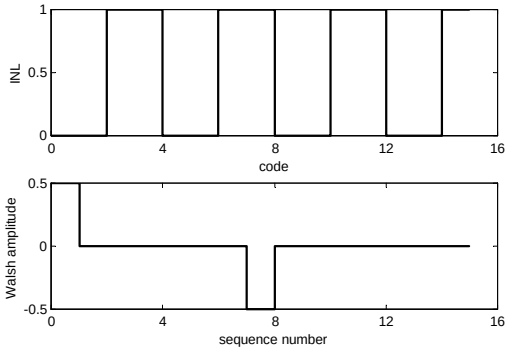

Fig. 2. A 4-bit converter's INL diagram and its Walsh transform with one bit error ($\varepsilon_3 \neq 0$)

transform of the INL: just the $2^i - 1$ sequences must be calculated for each i. The effect of the noise is decreased with this transformation, because in the Walsh space there are only N non-zero sequences from 2^N components. However, much more data are measured than it would be minimally required to determine the bit errors. The benefit of analyzing the INL in the Walsh space becomes evident if higher-order interactions are also present.

3.3 Higher-order intermodulations

Due to superposition errors higher-order intermodulations are present. In the further sections, the number of interacting bits will be referred as the *order* of intermodulation. Since normally the superposition errors are much smaller than the linearity errors, bit errors will probably also present. The higher-order intermodulations can be also determined with the Walsh functions. If two or more bits are interacting, then an error function will result which is the *product* of the corresponding bit error functions, which can be also described by the product of Walsh functions. Each function in the product corresponds to a bit taking part in the interaction. The product of Walsh functions equals to (4):

$$W(n_1, t) \cdot \ldots \cdot W(n_r, t) = W([n_1 \oplus \ldots \oplus n_r], t) \qquad (4)$$

where the $\oplus$ operator is the modulo-2 summation. This means that the multiplication of Walsh functions produces another Walsh function. On the other hand, due to the modulo-2 summation, the multiplication will not generate sequence outside the $(0, 2^{N-1})$ space. However, again caused by the definition of the Walsh series, the real result will be slightly different. The error function of a bit error is described by two Walsh functions,

$$\varepsilon_{i_n}(t) = \left(-\frac{1}{2}\right)[W(n, t) - W(0, t)] \qquad (5)$$

where $n = 2^{i_n} - 1$ and $i_n \in [1, \ldots, N]$ denotes the index of the erroneous bit. Therefore the product of error functions in the time domain is

$$\varepsilon_{i_{n_1}} \cdot \ldots \cdot \varepsilon_{i_{n_r}}(t) = \prod_{j=1}^{r}\left(-\frac{1}{2}\right)[W(n_j, t) - W(0, t)] \qquad (6)$$
$$= \left(-\frac{1}{2}\right)^r \prod_{j=1}^{r}[W(n_j, t) - W(0, t)]$$

Due to the fact, that $W(n, t) \cdot W(0, t) = W(n, t)$ the intermodulation will produce components also at the

sequences where the bit errors ($W(n_j, t)$) should appear (Fig. 3).In fact, an intermodulation generates components at

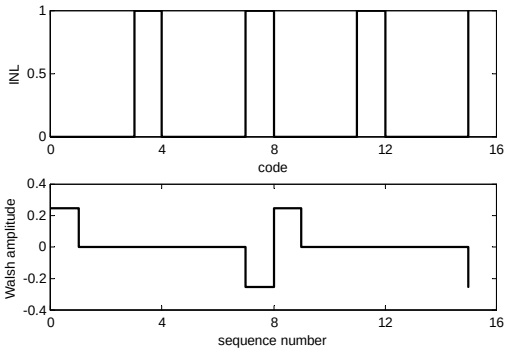

Fig. 3. A 4 bit-converter with 2 intermodulating bits (b_3, b_4) and without bit errors

all the lower order intermodulations. Hereinafter, the expression *mainterm* will refer to the sequence calculated as the modulo-2 sum of all the interacting bits ($n_1 \oplus \ldots \oplus n_h$). This sequence is only affected by higher-order intermodulations, and not by lower or equal ones. This *key fact* enables the separation of the error sources. Unfortunately, different intermodulations can be present at a single sequence (except the highest-order mainterm), but they can be separated by solving a set of linear equations. However, at the cost of an increased noise sensitivity. From (6) it is also clear that the amplitude of an *r*-order intermodulation will be decreased by a factor of $1/2^r$.

4. DETERMINING THE ERROR TERMS

4.1 Transformation matrix

Although the Walsh transformation separates the first-order errors ideally, for higher-order intermodulation an additional linear transformation is needed due to the spreading of higher-order intermodulation terms through the Walsh space. Identification of the intercorrelation terms requires two step: first the Walsh spectra of the INL are calculated,

$$\underline{w} = \mathbf{W} \cdot \underline{inl} \tag{7}$$

where $\mathbf{W}$ is the Walsh transformation matrix. The spectra are then further transformed with a linear transformation $\mathbf{T}$ in the intermodulation terms

$$\underline{\varepsilon} = \mathbf{T} \cdot \underline{w} \tag{8}$$

where $\underline{\varepsilon}$ contains the intermodulation terms [4]. There are only $2^N - 1$ intermodulations in the $\underline{\varepsilon}$ vector, because the zero order intermodulation has no importance. An in depth discussion of the transformation and theory can be found in [4]. As an example, the following vector contains all the correlation terms for a 3 bit converter (the 3 bits are denoted as 1, 2, 3):

$$\underline{\varepsilon}^{\mathbf{T}} = \left[\varepsilon_1\ \varepsilon_2\ \varepsilon_3\ \varepsilon_{12}\ \varepsilon_{13}\ \varepsilon_{23}\ \varepsilon_{123}\right] \tag{9}$$

As the purpose of this paper is to discuss the properties of the error terms and to propose a calibration algorithm based on the model of the converter, the focus will be put on compensation from now on.

5. CALIBRATION

Calibration is a possible way to increase the linearity of the converter. Here a parallel compensation scheme is proposed, where the non-linear characteristic of the main converter is corrected with a superimposed correction current (Fig. 4). A

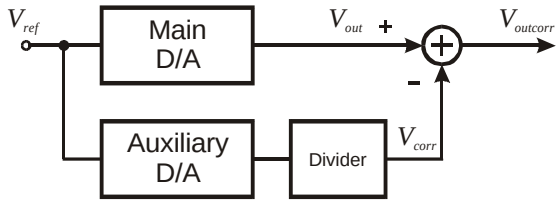

Fig. 4. Calibration scheme

second (auxiliary) converter is used to generate the correction current. The result is a highly linear converter. The model of the converter (3) is the basis for the correction algorithm. According to (3) the ideal (or required) transfer function (1) and the error contribution can easily be separated. If the model parameters are known ($\varepsilon_1, \ldots, \varepsilon_{1\ldots N}$), then the error contribution to this code can be computed and loaded in the auxiliary DAC. Subtracting both main and auxiliary signals bring the corrected output close to the ideal one.

One problem arises with the calibration: the error terms are obviously not constant, they can depend on frequency, temperature, input voltage level, etc. The properties and the usability of the calibration will hence be determined by the importance of these dependencies. In the next sections, these issues will be discussed based on measurement results.

6. MEASUREMENT RESULTS

6.1 Measurement set-up

Even if the simulations tend to prove the theory, the final verifications are made on real measurement data. Therefore, a test circuit was built, containing an 8-bit D/A converter and the support circuitry. The input data was generated by a digital I/O card, whose output was measured with a HP3458A high-precision multimeter. The reference signal was produced by a highly-stable, 10 V DC Zener precision reference. The INL was calculated as the difference between the real output and the best-fit line of the output characteristic. Each time 10 periods were measured, and the Walsh transform of the INL was averaged.

6.2 Verifications of the theory

The first measurements are simple INL diagram measurements: all codes are incrementally applied to the DAC (all of the measurements are made on DAC08 type converters). The INL measurements show that the method is applicable. The next set of measurements are made with different 'random' excitations. Random means that although all combinations are excited during a period, the order of the input signal's consecutive samples is chosen randomly. Three different realizations are measured and each realization consists of 10 periods (at ~1sample/s sampling rate). The aim of these experiments is to distinguish between dynamic and static effects. If the results are independent on the input sequence, then the errors are related to static errors. If there is a change in the intermodulation terms between the different perturbations, then the errors are at least partly caused by a dynamic effect. If dynamic effects are the significant error

$$V_{outcorr} = V_{ref} \cdot \left(\sum_{i=1}^{N} \frac{b_i}{2^i} + \sum_{i=1}^{N} b_i \varepsilon_i + \sum_{i=1}^{N} \sum_{j=i}^{N} b_i b_j \varepsilon_{ij} + \sum_{i=1}^{N} \sum_{j=i}^{N} \sum_{k=j}^{N} b_i b_j b_k \varepsilon_{ijk} + \ldots + b_1 \ldots b_N \varepsilon_{1\ldots N} \right)$$
$$- V_{ref} \cdot \left(\sum_{i=1}^{N} b_i \varepsilon_i + \sum_{i=1}^{N} \sum_{j=i}^{N} b_i b_j \varepsilon_{ij} + \sum_{i=1}^{N} \sum_{j=i}^{N} \sum_{k=j}^{N} b_i b_j b_k \varepsilon_{ijk} + \ldots + b_1 \ldots b_N \varepsilon_{1\ldots N} \right) = V_{ref} \cdot \left(\sum_{i=1}^{N} \frac{b_i}{2^i} \right) \quad (10)$$

sources, then the method is practically unusable for this type of converter. On Fig. 5 the measurement results are

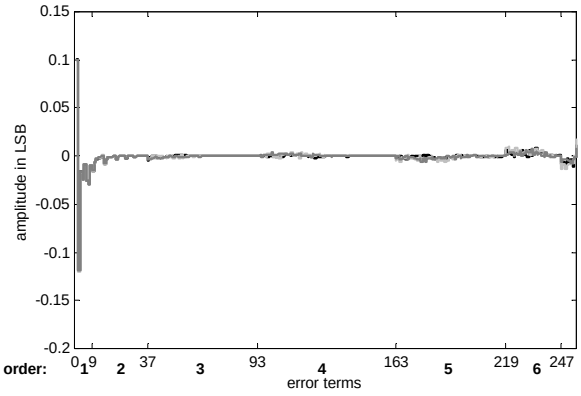

Fig. 5. All intermodulation error terms, ‘random’ excitations

plotted. The abscissa contains all the error terms, going from the bit-errors (index 1—8) to the higher-order correlations. Significant error terms appear at the first and second-order intermodulations, which are magnified out in Fig. 6. When

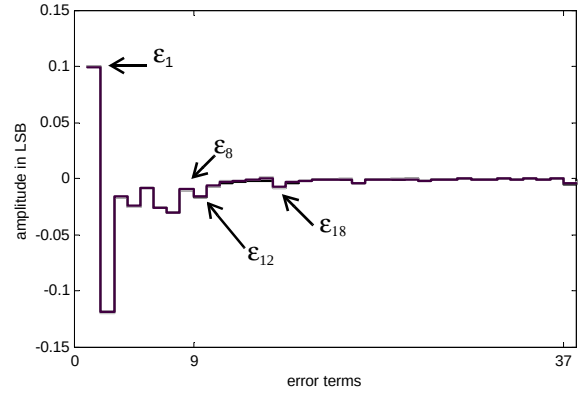

Fig. 6. First and second-order error terms, ‘random’ excitations

looking at the plots, keep in mind, that the error terms are *absolute* errors in LSB. The 3 measurement data for the three ‘random’ excitations produce 3 *slightly* different error pattern. The standard deviation of the data is calculated, and reaches it maximum for the highest-order term ($5{,}18 \cdot 10^{-3}$), but for the first and second-order terms it is only $1{,}36 \cdot 10^{-3}$. This means that fortunately the static errors are dominant, and this chip is suitable for further tests of the method.

6.3 Measurements on different DAC08 chips

The usability of the method was tested with measurements on different samples of the same type of converter (Fig. 7). The test was made on 5 chips from 2 different manufacturers. These results also indicated the applicability of the theory. The first-order errors differ for each chip, because the bit errors are caused by the imperfections of the binary division, which are different for each chip. The magnitude of the bit errors are in the same order for the different chips, which is also in agreement with our expectation. However, the second-order intermodulations show interestingly high correlations for all the chips. They are almost the same for any chip, what implies that these errors seem to be represent some kind of ‘structural‘ error.

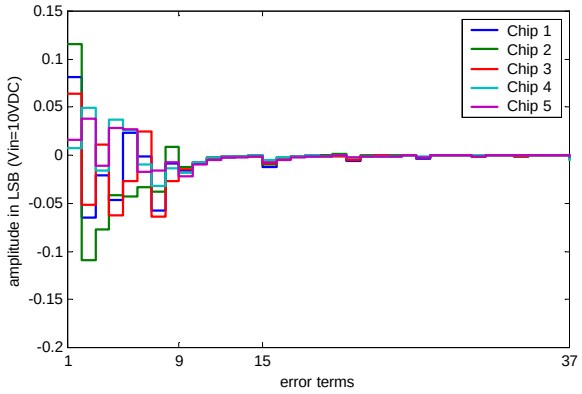

Fig. 7. Error terms of 5 different DAC08 chips

6.4 Properties of the model parameters

The model parameters are not constant, they depend on the power supply, temperature, etc. Unfortunately, they can even be dependent on the input signal (V_{ref}). A set of measurements is made to analyze the input signal dependency of the $\varepsilon_1, \ldots, \varepsilon_{1\ldots N}$ parameters. If the input signal dependence dominates in the bit errors, then the parallel calibration, and generally the calibration of multiplying converters is not possible with this method. However, at least in the case of bit errors ($\varepsilon_1, \ldots, \varepsilon_N$), it is expected to be independent of the input. These errors represent the errors of the binary division, which is mainly caused by device tolerances, and therefore should be independent from the input. The measurement results clearly satisfy the expectations. The measurements were made at different DC input voltages, from 4V to 10V in 1V step. The amplitude of the errors was not divided by the input voltage, therefore the plots - as all of the previous ones - show the error terms multiplied by the input voltage. All the error terms change monotonically with the input signal. The first-order bit errors seem to show a linear decrease with the reference. At zero input voltage, the bit errors would be equal to the error caused by leakage currents, which are quite the same for each bit. This is the reason why the lines converge to one point as the input voltage decreases. In order to characterize the linearity, a

linear regression of the error terms was performed, and the

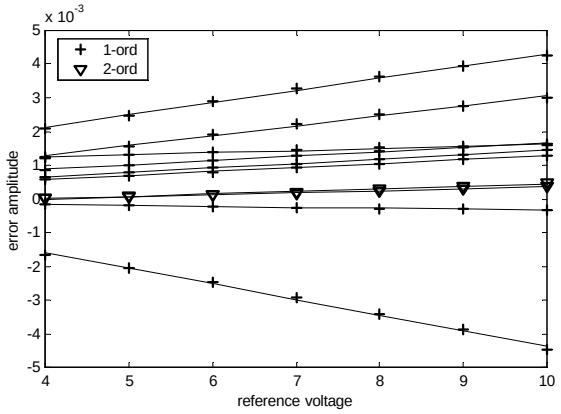

Fig. 8. Input signal dependency of some error terms

approximation error was also calculated. The second-order terms are clearly depart from linearity in this region, resulting in a really high linearization error (see Fig. 9.). Fortunately, the first-order error terms are behaving as a linear function of the input signal. The maximum error of the linearization is as low as 4.629%, which means that the calibration using the first-order terms is applicable in the measured input voltage range. Even if the second-order terms are not linear in the input signal (it seems that they are approximately quadratic functions of the input), using the raw estimation of the errors during the calibration further increases the linearity of the corrected DAC (see later).

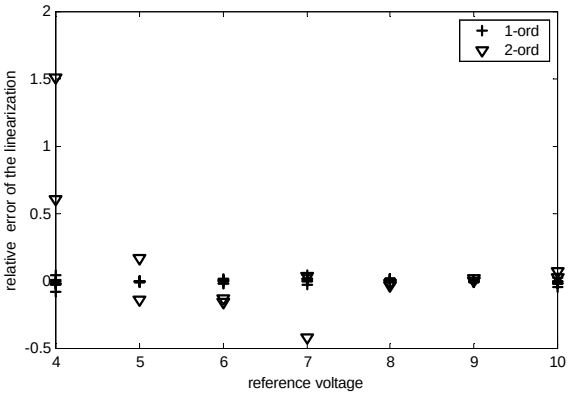

Fig. 9. Relative error of the linearization

6.5 Measurement results of the calibrated converter

The calibration was also realized on the custom designed test circuit. From the previous measurements it was clear that significant intermodulations are only present at the first-, second- (and maybe the third-) order intermodulations. There are 255 possible intermodulation terms for a 8-bit converter, but a good model is already obtained by using about ~30 intermodulation terms. To show the applicability of the theory on real measurements, two types of calibration are performed and the calibrated signals were measured. In the first case, only first-order intermodulation terms ($\varepsilon_1, \ldots, \varepsilon_N$) were used to calibrate the device. Next, a second trial was made, using first- and second-order terms ($\varepsilon_1, \ldots, \varepsilon_N, \varepsilon_{12}, \ldots, \varepsilon_{78}$). From

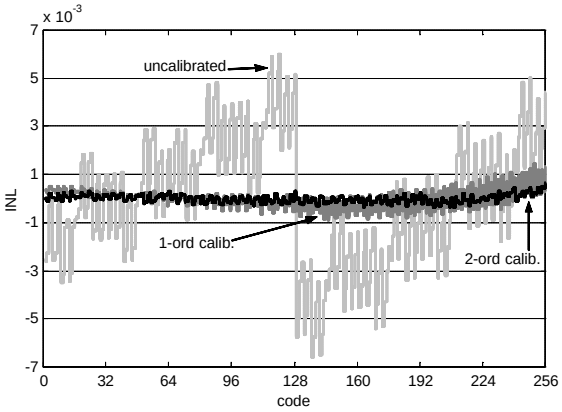

Fig. 10. INL of uncalibrated, first-order calibrated, and first- and second order calibrated converter

the results it is easy to see that the theory is applicable to real devices. Significant increase in linearity can be achieved with first-order correction and one gains an additional order of magnitude for the first- and second-order calibration.

7. CONCLUSIONS

A method is presented to characterize and correct the static non-linearity of D/A converters. It was shown that the INL contains all the required information. Using the Walsh transformation it is possible to identify both the bit errors, and the higher-order intermodulations. Unfortunately, due to the definition of the Walsh functions, higher-order intermodulations also produce components at lower-order terms. An additional linear transformation is required to extract the error terms. Real measurements were used to validate the theory and to have an idea about the behaviour of the error terms. Based on the non-linear model, a calibration procedure was also performed and was shown to increase the linearity of the converter by an order of magnitude.

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