A MOSFET-ONLY DAC FOR A GENERAL ARRAY CONFIGURED DEVICE

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Abstract - In this paper we present an 8 bits CMOS-only Digital to Analogue Converter (DAC), which has been used to introduce complex signals inside of a system based on an array of discrete elements. The design and the test are designed taking into account the nature of its application.

1. INTRODUCTION

Last developments in microsystems field tends to define architectures based in array configured single devices in spite of classical one device system. This fact allows using all the potential capabilities of the new technologic developments, not only in pure electronics as in micromechanics field.
Some examples can be tactile sensors, array configured gas sensors, CMOS image sensors and range finders and multiple applications in biomedical environment.
In the other hand each single device (sensor or actuator) could need, in order to achieve better performances a great number of input and output signals, and this demand could increase as packaging technologies (like multi-chip modules) becomes more and more useful.
These required signals in many cases include DC signals and more complex waveforms with external addressing by means of a digital circuitry to control them.
One of the more useful solutions to achieve this fact consists on a DAC architecture, that can deliver at the output any required waveform shape, only controlling the input digital part by means of a digital control circuitry.
For all the cases, pure CMOS microelectronics array systems or more complex MCM electronics and micromechanics array systems, we need to address this control signals to a great number of individual cells, and this number can increase more and more as technology developments increase. Due to this fact, the capacitance to be charged at DAC output could increase considerably to enable a signal partitioning in order to introduce some buffers in an intelligent way.
In a general point of view we have to introduce analogue buffers, by means of the use of voltage follower configured operational amplifiers.
In our particular design target, we have to drive an array of 320x320 individual cells with a total capacitive load for each column of 15pF, which means a total load of 4800pF. For this particular target, a global driving is difficult to achieve, taking into account we need to reduce the area cost, and is a better solution split the driver scheme into single blocks, each one for every column. Another design target is to transfer high-speed signals, which means variable periodic ramps that are showed in figure 1.

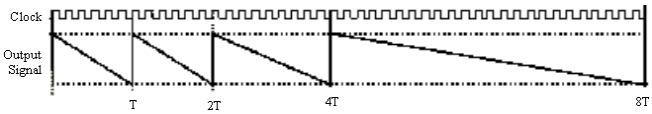

Figure 1. Typical high speed signal

Our limitations are 10 μs as the minimum period of the signals and a slew-rate as high as 20 V/μs. To achieve these performances we have designed a two-stage class AB operational amplifier [8] as the column analogue buffer. We can think easily there is a hard task to obtain these target requirements using a single stage buffering.
It has been taking into account that the same operational amplifier could be used in order to drive this great number of individual buffers by a proper way.
For the other hand, new digital CMOS technologies tends to a more compact structures by means of the minimisation of the channel length of the transistors. In this design environment, resistors become higher (in terms of area) as transistor dimensions becomes lower. Typical R-2R ladders, used in classical DAC design, in this field becomes useless and is better to think in a MOSFET only DAC to reduce area cost. Also, MOSFET DAC's are intrinsically faster and more linear than resistor-string DAC's [1]. Another important consideration is the need of reduced supply voltage in order to avoid transistor breakdown and reduce power consumption. This fact has to be taken into account to design low-voltage structures (3V in our case).
One of the more used architectures to design MOSFET-only DAC is based in the current-steering techniques [2,3], using an array of matched current sources. They are frequently used to achieve high linear devices, using segmented architectures and proper switching scheme [4].
In order to achieve this high linearity, a great number of transistors have to be implemented (to achieve n bit linearity, we need 2^n transistors without any segmented architecture) and geometrical matching of the structure becomes important in order to reduced undesired nonlinearly.
Another simple solution, for medium linearity, as can be 8 bits (this is the target required for our application), is to use a MOSFET ladder as D/A converter [5], based on a linear current division technique [6]. The architecture of the global ladder is similar to the classical resistor-based R-2R ladder, as can be seen in figure 2.

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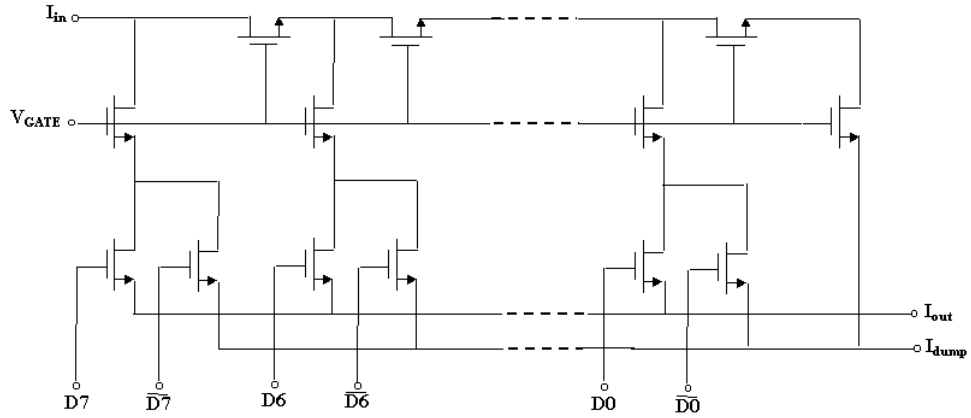

Figure 2. MOSFET ladder

Our approach has been the use of a similar MOSFET ladder with an efficient buffer circuitry, which will be described in the next section.

2. DESIGN

In order to well understand the main aspects involved in the design process, it could be better to split the design section in two different parts, concerning the two key elements of the system, the output buffer and the MOSFET ladder.

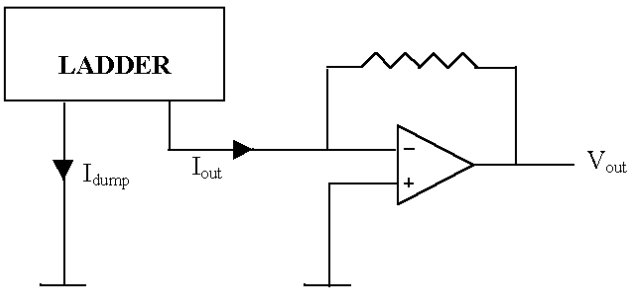

Figure 3. Output voltage configuration

2.1 Output buffer

In order to obtain output voltage waveforms, a simple transimpedance amplifier could be used. In figure 3 can be seen the classical transimpedance configuration using an operational amplifier and a resistor.

In order to increase the linearity of the final DAC structure, this configuration can't be used, because of the non zero input resistance of the amplifier, which introduces an important mismatch between the two output signals of the DAC.

To improve the performances of the structure, it can be introduced between the DAC output and the current to votlage conversion stage a current buffer with very low input resistance. Also, another problem with exhibits the classical configuration of figure 3 is the voltage offset of the operational amplifier that introduces another source of mismatch between the output current signals. Taking into account this fact the current buffer to be introduced between the stages needs to transfer at the input current terminal a well defined voltage value, equal to the value that sources dummy current output, with a very low offset.

This feature can be achieved using a current conveyor (figure 4), which performs a double voltage-current transference, as can be seen in equation 1.

Figure 4. Current conveyor

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & a & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}$$

Equation 1

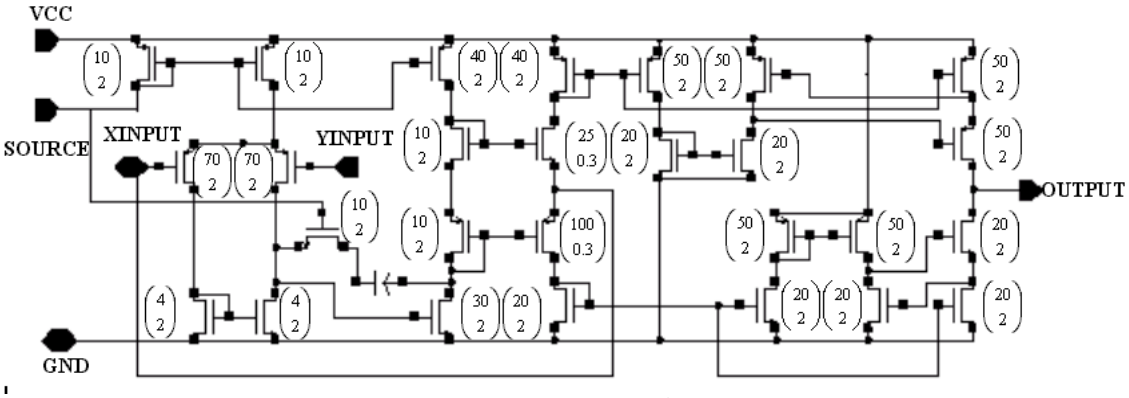

Figure 5. Current Conveyor Configuration

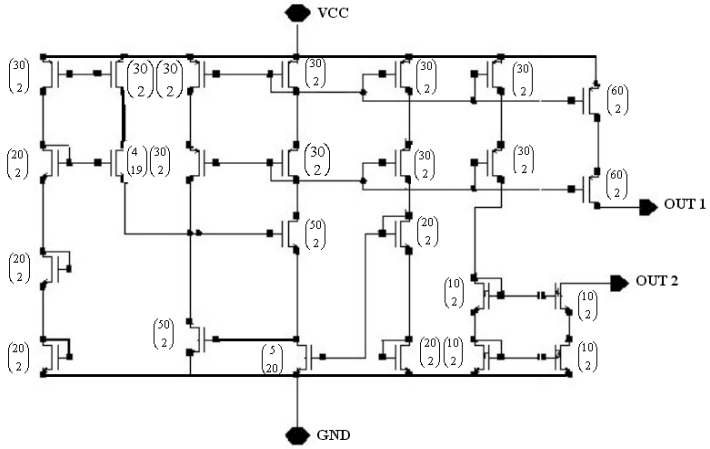

Figure 6. Current Source

Novel high speed current conveyor configuration uses an input stage similar to used in standard current feedback operational amplifiers. This fact increases the offset of the voltage transfer but increases speed performances of the global device. This offset increase avoids using this configuration and it's better to design a current conveyor using a more classical approach using an input voltage differential stage [7]

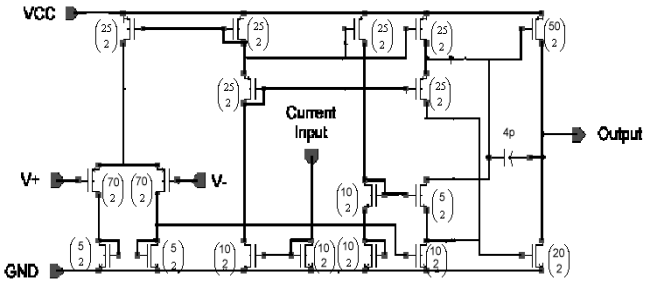

Figure 7. Output Buffer

Relating to current-to-voltage conversion, the classical design depicted in figure 2 has been used in order to control the voltage levels at the output. Related to the operational amplifier design, we can use the same design used in the buffer stage, so a classical operational amplifier with a class AB output stage has been used to drive the output charge. The schematic of the circuit can be observed in figure 7 [8].
Also, in order to deliver the desired bias current in each circuit an autopolarization reference has been used. In this design, a transistor in the linear region has been used instead of classical resistor, as can be see in figure 6.

2.2 DAC design

The DAC is based on the structure depicted in figure 2. An additional circuitry has been added to the simpler structure in order to avoid undesired glitches in the output of the DAC. We must take into account we have to avoid no path for the current in all switching time. This fact could be achieved using the latch of figure 8. The behaviour of this latch assures that during all switching time there is a path for the current by means of the delaying of the input signals of each pair of MOS [4].
Also, two extra MOS transistors connected between the decision pair and both outputs assures no influence of the output voltage value on the behaviour of these decision transistors. Both extra transistors have the gate connected to the Vgate (HIGH) terminal, which means they are in the in saturation or linear region, not cut-off.

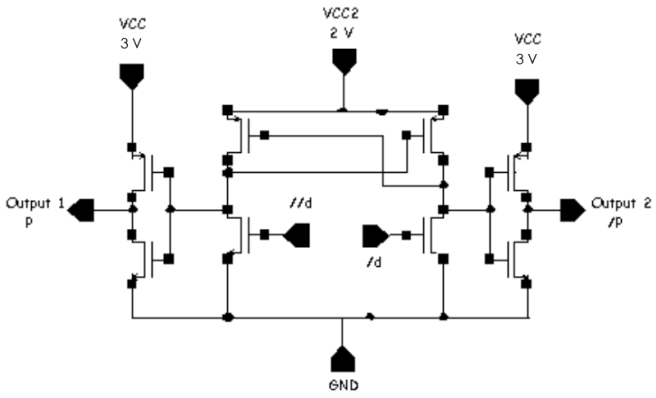

Figure 8. Schechematic of the Latch circuit

3. SIMULATION RESULTS

Simulated results, depicted in figure 9 for a clock period of 250ns, exhibit 8 bits linearity of the total system for the required voltage values. Experimental results will be used to determine the final speed-linearity capabilities of the system.

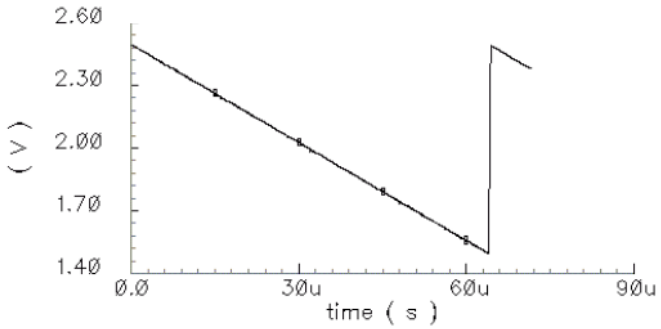

Figure 9. Simulated results for period=250ns

4. LAYOUT

A picture of the layout is presented in figure 10. The final structure is placed in the right side of the upper part of the layout. This has been implemented using 0.35 μm CMOS technology from AMS.

5. PROPOSED TEST METHODOLOGY

Due to the specific topology of our system, the DAC testing has some particular points that have to be taken into account:

- The DAC is used to generate a specific waveform: a ramp with increasing period.
- There is a complex buffer system with a low-impedance input stage designed in order to drive the global circuitry.
- We have only two inputs to control the digital circuitry: an enable circuitry and an external clock input.

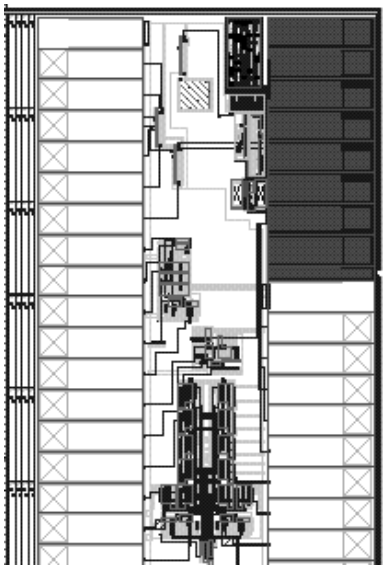

Figure 10. Layout of the design

So, no influence of the charge is expected in the behaviour of the DAC (confirmed by simulation, we can obtain an input resistance in the current conveyor less than 1 Ω). The problem is we don't have accessibility to the DAC outputs and we can't also modify its input waveforms.

So, for the final behaviour of the system there are only two parameters of interest, the linearity of the array related with the speed of the clock signal. These topics are mainly related with the real RC constants of the DAC structure, non-expected glitches and the transfer function and charge capabilities of the output buffer system.

Final tests will consist on different patterns of clock frequencies and a synchronised scanning of the system output, in order to obtain the linearity-frequency characteristic, that could be thought as the main figure of merit of the system, as can be seen in figure 10.

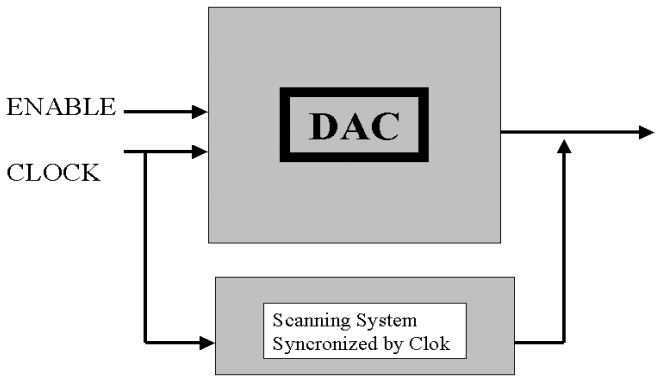

Figure 10. Test scheme

The main goal is to obtain the maximum speed for a constant linearity of eight bits. We must keep in mind final speed of the global system will be function of the maximum speed of the DAC without losses in linearity.

6. CONCLUSIONS

A system capable to drive a high number of individual elements in an array configuration has been developed. The system is based in an eight bits MOSFET-only DAC that is the key element of the design. An easy test scheme, based in the specific behaviour of the system, has been developed in order to be implemented as soon as design comes from the foundry. This test is based on an own figure of merit; linearity vs speed of the system that is the main parameter to be obtained with the developed test schedule.

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