FREQUENCY DOMAIN ANALYSIS FOR INTEGRAL NONLINEARITY MEASUREMENT IN A/D CONVERTERS WITH DITHER

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Abstract – *The paper examines the problem of achieving a fast measurement of nonlinearity for a dithered converter. It is shown that, since dither removes small-scale systematic errors, measuring the remaining large-scale (smooth) nonlinearity can be efficiently achieved via a fast frequency domain test, formerly analyzed by the authors for conventional converters without dither. The test appears especially suited for dithered converters, and can be useful for the periodic adjustment of a look-up table intended for removing large-scale nonlinearities.*

Keywords - Analog-Digital conversion, Data Acquisition, Nonlinear systems, Dithering.

1. INTRODUCTION

Dithering is a common and well-known technique, more and more employed in modern digitizers for measurement application, which basically consists in adding a random or pseudorandom small signal (dither signal) to the input waveform. More specifically, in the subtractive topology the dither signal is pseudorandom and is synchronously added to the analog input and subtracted from the digital output; in the non-subtractive topology the dither signal is only added at the input and then (optionally) removed by averaging or filtering the output.

Non-subtractive dither is especially appealing and more common in practice, because – unlike the subtractive one – it does not need costly hardware for generating a precisely known signal and perform synchronous analog and digital operations. Besides, it can be sometimes implemented by simply exploiting the analog noise of the converter or other small stable signals inherently present in the digitizing hardware. In this work we are mostly concerned with non-subtractive dither, even if many consideration can apply also to the subtractive topology.

Dither is essentially a trade-off, as it decreases systematic errors at the cost of increasing random errors, which can be finally averaged out (or not). Early works regarding this subject (e.g. [1], [2]) concern the case of ideal quantization, and show that a proper dither signal is able to make the quantization error totally uncorrelated with the input (so that it can be effectively eliminated by a proper digital filter). The effect of dither on a more practical model of ADC, i.e. on a nonlinear quantization, has been more recently studied by many authors (e.g. [3], [4]).

From these works it can be generally inferred that dither is able to transform part of the nonlinearity error in random noise, just like it does for quantization error (which is, indeed, a nonlinearity). As intuition suggests, dither is not able to nullify the nonlinearity error completely but only to "smear" it [3]. In short, it is able to remove the nonlinearity only at a microscopic level (quantization error is indeed a microscopic nonlinearity), while large scale nonlinearities are better removed by a look-up table or some similar technique [5].

The considerations above bring to evidence the problem of *measuring the residual large-scale nonlinearity in a dithered nonlinear quantizer*, for example for the purpose of error correction. The first impression of having a simple and already solved problem is in fact deceptive: moreover, comparatively few works exist on the specific topic of dithered ADC testing (one example is [6]).

The first possible idea [5] is to carry out a standard histogram test [7] on the undithered quantizer, afterwards deriving an estimate of the nonlinearity of the dithered quantizer by convolution with the probability density function (pdf) of the dither (or applying the nearly equivalent equations in [3]). The drawbacks of this approach are that it is obviously costing in terms of time and computations (especially when dealing with a high-resolution ADC) and that often the pdf of the dither is not known very precisely. It should be obviously preferable a direct nonlinearity measurement on the dithered ADC.

Another possible option, providing such a direct nonlinearity measurement, is the simple comparison of the averaged output with the (known) input of the converter. This method is undoubtedly very reliable, as it deals directly with the physical input and output of the ADC, and does not require complicate computations, or any knowledge of the dither signal. On the other hand, it can be even more time-consuming than histogram test, as a large number of averages are needed in order to remove all the random errors introduced by the dither and obtain only the systematic part of the conversion error.

The third possibility is illustrated in this paper and consists in using FFT analysis to reconstruct the integral nonlinearity of a dithered ADC. This approach is incomparably faster then the two above and, like the direct nonlinearity measurement, does not require information or calculations involving the pdf of the dither signal. As will be clear from theory and experiments, this test exploits the dither capability of removing quantization and small-scale nonlinearities in order to provide accurate results. Besides velocity and reliability, there are other advantages, related to the problem of ADC linearization, which will be briefly discussed in the conclusions.

2. THEORY

Before speaking about the test methodology it is important to recall some simple but often misunderstood aspects of nonlinearity in ADC's, dithered or not. The integral nonlinearity of a converter is defined (without considering gain and offset errors that are inessential in this context) as the difference

$$inl_k = t_k^{id} - t_k \qquad (1)$$

being t_k^{id} the ideal (equispaced) threshold levels and t_k the actual threshold levels of the quantizing characteristic. The servo-loop based static test or the dynamic histogram test are the standard methods to obtain this quantity [7], which is usually represented by plotting it versus the index k or, equivalently, versus the equispaced threshold levels t_k^{id}. Although useful and very common, this plot should never be understood as a representation of the true "nonlinearity" of the ADC that, due to quantization, is a far more erratic function. The static characteristic of the converter is indeed

$$g((x) = quant(g_s(x)) \qquad (2)$$

where $quant(\cdot)$ stands for ideal quantization and $g_s(x)$ is a function (for example a piecewise function) such that $g_s(t_k) = t_k^{id}$. This equation expresses the decomposition (Fig. 1) of the nonlinear quantization characteristic in the cascade of a smoother nonlinear characteristic $g_s(x)$ and ideal quantization.

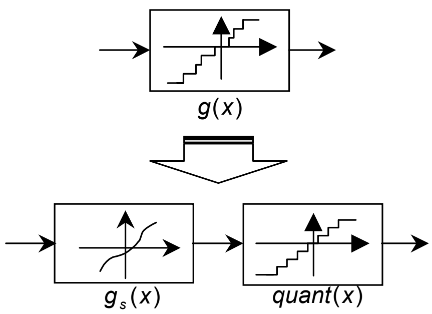

Fig. 1. Decomposition of a nonlinear quantizer $g(x)$ in an ideal (linear) quantizer *quant*() preceded by a smoother nonlinearity $g_s(x)$.

Due to the relation $g_s(t_k) = t_k^{id}$, the nonlinearity introduced by the first block, $g_s(x) - x$, is represented by a plot of inl_k vs. t_k, which is different (even if only slightly in practice) from the usual plot of inl_k vs. t_k^{id} (Fig. 2a). The overall nonlinearity of the ADC, $g(x) - x$, includes quantization error, which is usually of the same order of magnitude of inl_k (Fig. 2b).

Now, a dither signal $n(t)$ with pdf $f(n)$ simply transform the nonlinear characteristic $g(x)$ in an average characteristic that is the convolution $g_d(x) = g(x) * f(n)$. This is basically a smoothing (or a low-pass filtering) of $g(x)$. It is not surprising, therefore, that the dither technique, originally designed for removing the quantization error, has been found also useful to remove or reduce sharp variations in the integral nonlinearity. Such sharp variations are sometimes called "differential nonlinearity" (which is in strict sense the numerical derivative of the integral nonlinearity) or more exactly "small-scale errors" [5] (which means that they arise and vanish in an interval of few LSB, and not that they are small).

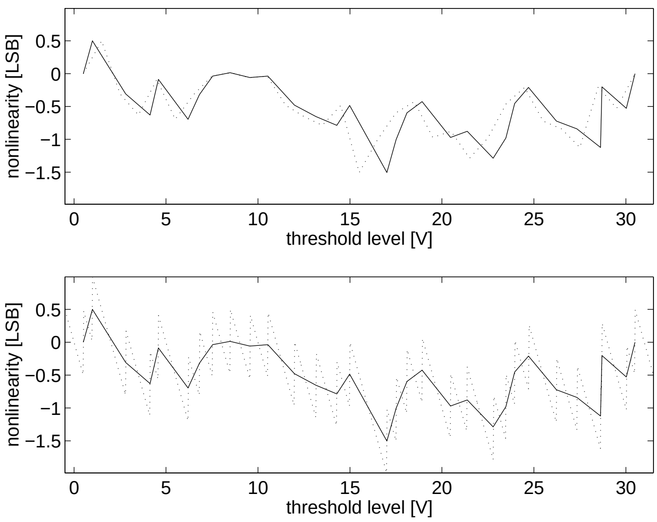

Fig. 2. (a) – Comparison between a plot of inl_k vs. t_k^{id} (…) and a plot of inl_k vs. t_k (—). The latter is the true nonlinearity of the block $g_s(x)$. (b) – Comparison between the nonlinearity of the block $g_s(x)$ and the nonlinearity of the converter ($g(x) - x$), that includes quantization error.

It is therefore clear that when an ADC is dithered its characteristic $g_d(x)$ – having removed quantization errors and small-scale nonlinearity errors – becomes a smoothed version of the block $g_s(x)$ in Fig. 1. In this situation it is quite reasonable to hypothesize that $g_d(x)$ is well approximated by a *polynomial* function. As the authors illustrated in former works [8], [9], measuring a polynomial approximation of a converter nonlinearity is quite simple and quick via an FFT test. The simple theoretical basis of the test is the following.

If at the input of the memoryless characteristic $g(x)$ is applied the sinusoidal signal $x(t) = V\cos\omega t + C$, then the output must be in the form:

$$y(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos(n\omega t) \qquad (3)$$

It can be easily demonstrated that the best (in the mean-squared error sense) polynomial approximation of $g(x)$ is the sum

$$g(x) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n C_n\left(\frac{x-C}{V}\right) \qquad (4)$$

where $C_n(x)$ is the n-th degree Chebyshev polynomial of the first kind, $C_n(x) = \cos(n \cdot \arccos(x))$.

In [8] and [9] the possibility of using this theory in standard ADC testing has been investigated. In this case quantization error is a major concern, that makes virtually impossible to obtain information about the differential nonlinearity by frequency-domain investigation. Nevertheless, the FFT test on an undithered converter can give, by proper selection of the harmonics to insert in (4), useful information about the integral nonlinearity.

In the case of an ADC with dither, when quantization and small-scale nonlinearity errors have been practically eliminated, the illustrated technique is particularly attractive. In this case the details about $g_s(x)$ provided by the histogram test appear clearly unnecessary and redundant, and moreover a polynomial expression of the overall characteristic $g_d(x)$ seems to be particularly convenient to implement an efficient error-correction scheme.

3. EXPERIMENTS

The theoretical conclusion that the FFT test of integral nonlinearity can give very good performance on dithered converters needs of course practical demonstrations. A meaningful validation has been obtained by means of experiments, reported here, involving an 8-bit flash converter embedded in a digital oscilloscope.

All the results reported below have been obtained using a coherently sampled sinusoidal test signal at about 1500 Hz. The choice of a comparatively slow test signal assures that dynamic effects that arise at higher frequencies do not pollute the results. The performed tests must be considered therefore substantially static, and the measured nonlinearity is truly the *static part* of the ADC transfer function. It is not useless to stress that measuring the integral nonlinearity with a conventional histogram test at “high” frequencies (i.e. when also meaningful dynamic errors are present) can give a gross qualitative idea of the performance deterioration in dynamic conditions, but the obtained result can by no means considered representative of the ADC transfer function.

In the first experiment the actual threshold levels of the converter have been accurately measured by performing a histogram test with an overdriving sine wave, according all the prescriptions in [7]. A very high number of samples have been acquired (many thousands per code bin) so that random errors on the measured nonlinearity are certainly negligible. On the other hand, also systematic errors have been made very small using a sine wave with very high purity compared with the ADC resolution.

The result of the histogram test is represented, in Fig. 3 (thin line), as a plot of the integral nonlinearity $inl_k = t_k^{id} - t_k$ vs. the actual threshold levels t_k. As explained in section 2, this plot is actually a graph of the difference $g_s(x) - x$, that is the nonlinearity of the device *without* considering ideal quantization. It is important to notice the typical appearance of the nonlinearity in an actual ADC: it can be seen as the superposition of a slowly varying function with greater amplitude, and smaller components with much faster variations. It is clear, from the briefly recalled theory of Chebyshev polynomials, that the first component generates distortion power concentrated it in few spurious harmonics, whereas the latter components are responsible for distortion power spread in many small harmonics, in a way similar to quantization error.

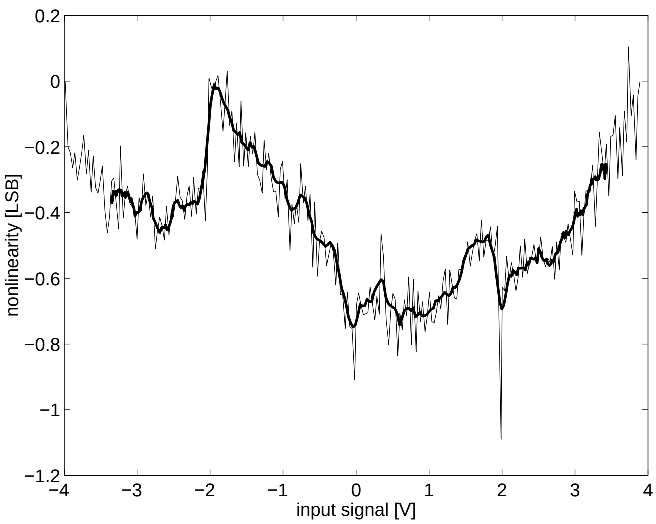

Fig. 3. Linearity of the 8-bit ADC: without dither, measured by the histogram test (thin line), and with dithered, measured via sine wave fit on the average of 10,000 records of 2,000 samples (thick line). It is apparent that, besides quantization errors, also small-scale nonlinearity errors are dramatically reduced by the dither.

In the second test the ADC has been employed with a Gaussian non-subtractive dither with standard deviation $\sigma_d \approx 1.5$ LSB rms. The aim was indeed to measure directly the nonlinearity of the dithered converter, without resorting to simulations or computations that require accurate knowledge of the dither pdf. The "brute force" method employed is the following:

1) acquire N records $y_i(t)$ of a spectrally pure sine wave;

2) calculate the average $y(t) = \frac{1}{N}\sum y_i(t)$;

3) find the best-fit sine wave $x(t)$ of the averaged signal $y(t)$ [7];

4) find the nonlinearity as $g_d(x) = y(t) - Gx(t) - O$, where G and O are gain and offset errors.

The number of records must be fixed according to the desired uncertainty on the measured $g_d(x)$, which can be quantified simply by the formula

$$\sigma_{tot} = \sqrt{\sigma_d^2 + Q^2/12} / \sqrt{N} \quad (5)$$

We have chosen N = 10,000 obtaining an uncertainty of about 0.05 LSB with a confidence level of 99.7 %. Needless to say, this simple test is very time-consuming. The result, reported in Fig. 3 (thick line) for comparison with the histogram test, shows that the dither, besides removing the quantization error, has also eliminated most of the small-scale errors of the converter.

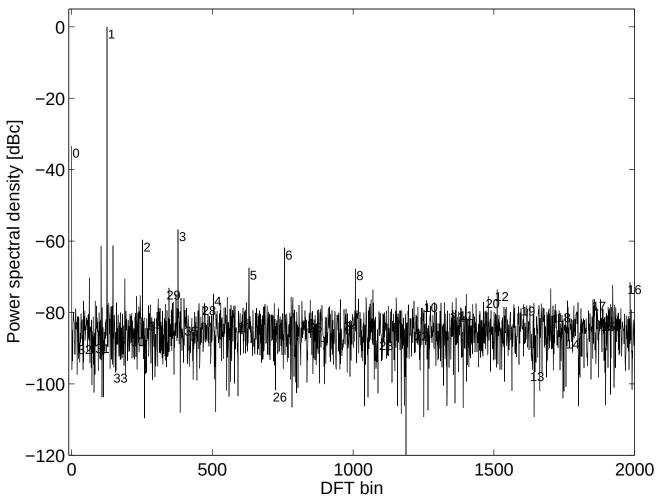

Fig. 4. Normalized power spectral density of the output of the undithered ADC under test (16,000 samples) when stimulated by a sinusoidal input. The plot shows the first 35 harmonics, that have been employed to obtain the Chebyshev polynomial approximation of the nonlinearity of the dithered converter.

Finally, we have performed the FFT test on the undithered ADC. As the ADC was embedded in a digital oscilloscope allowing the acquisition of a maximum of 4,000 samples per record, four records have been acquired and averaged, so utilizing 16,000 samples for the estimate. Fig. 4 represents the normalized power spectral density of the output of the converter. In the plot the first 35 harmonics are highlighted, as they have been used to reconstruct the nonlinearity of the dithered converter. As pointed out in previous works [8], [9], the optimum number of harmonics to consider is a critical point, as it depends on the actual noise level inherently present in the digitizer and on the number of acquired samples. Providing a simple formula yielding the number of harmonics to consider on the basis of the measured spectrum is one of the still open questions of this research. At the moment we can say, as a rule of the thumb deriving from our experiments, that for an 8-bit converter tested with 8,000-16,000 samples, considering from 30 to 50 harmonics is almost always perfectly adequate to obtain good approximations to the integral nonlinearity.

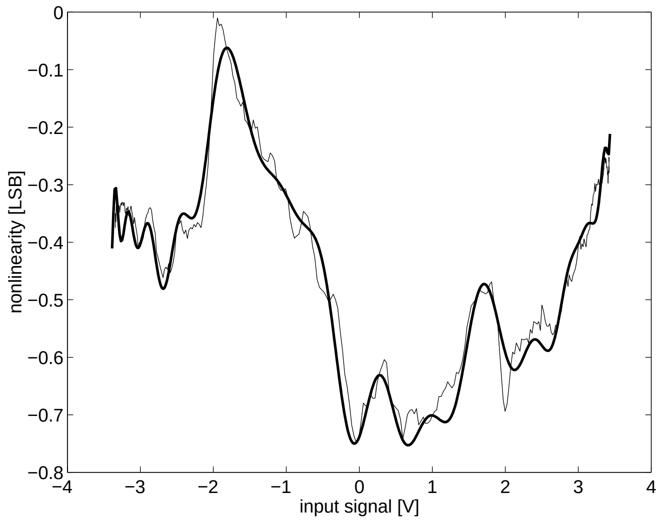

Fig. 5. Plot of the overall nonlinearity of the dithered ADC measured via FFT (thick line), compared with the "true" nonlinearity measured via sine wave fit on the average of 10,000 records (thin line). The FFT test has required only 16,000 samples and the result is a sum of 35 Chebyshev polynomial terms.

The nonlinearity derived from the application of formula (4) is compared, in Fig. 5, with the "true" nonlinearity of the dithered converter as measured by the direct comparison of the input with the averaged output. It is apparent that the test results are quite satisfactory: the maximum deviation between the two estimates is below 0.1 LSB, and the typical deviation is 5-10 times smaller. On the other hand, the test is practically instantaneous, if compared with the histogram test or the sine wave fit on the averaged output.

7. CONCLUSIONS

Theoretical considerations about nonlinearity in dithered ADC's suggest that the residual systematic error in such devices is mainly large-scale integral nonlinearity without sharp variations (which means that the differential nonlinearity becomes very small). The FFT test for measuring the integral nonlinearity therefore deserves particular attention as a tool for testing such particular acquisition systems. It must be considered, indeed, that:

1) in a dithered ADC, the nonlinearity is usually well approximated by a polynomial function, which is not always satisfactory for an ADC without dither;

2) an important issue in dithered ADC is the correction of the remaining large-scale errors, which should be periodically measured with a fast and simple test;

3) for the purpose of error-correction, it can be useful to have a simple expression of the linearizing function instead of a look-up table with a very large number of entries.

The FFT test of nonlinearity is therefore perfectly suited for this case. With special reference to the point three above, it must be kept in careful consideration that the nonlinearity function is expressed using only few coefficients (35 in the reported experiment). It seems promising, therefore, the idea of implementing a linearization algorithm based on Chebyshev polynomials, in order to improve the digitizer performance, following the scheme presented in [5].

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