METROLOGICAL MODELLING OF Σ–Δ ADC

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Abstract: *The paper uses a metrological approach to modelling of Σ–Δ ADC. The main goal of such modelling is possibility to evaluate the uncertainty of A-D conversion with given probability. The main attention is devoted to errors produced by noise. Analysis uses both frequency and time domains. The application of the metrological modelling is demonstrated at the example of the concrete ADC manufactured by Analog Devices company. The paper is based on application of metrology in design made in MPEI (Russia) as well as on widespread investigations of Σ–Δ ADC fulfilled in University of Westminster (England).*

Keywords: sigma-delta analog-to-digital converter, quantization noise, metrological modelling.

1. INTRODUCTION

Σ–Δ ADCs are very widespread in many applications. According to analysis made in [1], Σ–Δ ADCs are used in 9 fields of application from 14 considered. Only successive approximation ADC has the same rating. The number of publications devoted to Σ–Δ ADCs seems to dominate last years in comparison with other types of converters. The most specific and important feature of Σ–Δ ADC is noise. It comes from two sources [2]. The first one is the electrical noise in the semiconductor devices and resistors. The second source is so called quantization noise. In principle, quantization error is a systematic one but it can be considered as a random quantity or quantization noise if input quantity of the ADC is a random variable. There is many papers investigating the quantization noise. The basic block diagram shown in Fig. 1 is usually examined [3,4].

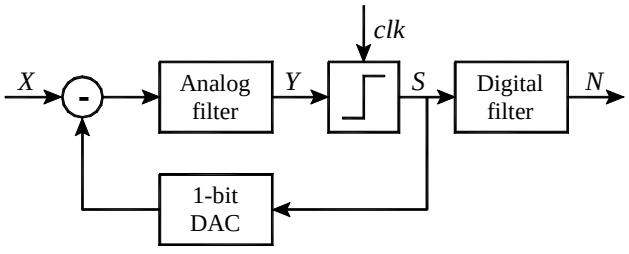

Fig. 1. Basic block diagram of Σ–Δ ADC.

Input analog signal X (DC voltage, for example) is converted into code N. An analog filter consists of n integrators. A comparator or quantizer is synchronized by clock signal with frequency Kf_S, where K is the modulator oversampling ratio. Digital output of the comparator S is transformed with 1-bit digital-to-analog converter to analog form to be subtracted from the input signal. Digital filter realizes weighting averaging [5]. The output data rate for the digital filter = the first notch of the filter = f_S [2,4].

It is usually supposed [3,4] that spectral intensity of comparator signal S_C is constant. To prove this fundamental idea, the transfer function of the comparator (1-bit converter) is represented in [3] as a part of many bit ADC, the input signal being uniformly distributed in the range [-2, +2]. Reference voltage V_{REF} is accepted here as unit. Then the comparator can be modelled as an amplifier with gain η followed by the quantization noise ε. The value of η can be chosen so [3] that the signal Y multiplied by η is spread over the whole range [-2, +2].

The *SNR* of the circuit shown in Fig. 1 is found in [3] as

$$SNR \approx 10 \log \frac{3a^2 (2n+1) K^{2n+1}}{2A^2 \pi^{2n}}, \qquad (1)$$

where a is the input signal amplitude (referred to reference voltage V_{REF}), A is the gain of the noise transfer function of a "lowpass modulator" or analog filter. It was accepted $a = 1$ and $A = 1$ in [3]. Corresponding functions of *SNR* vs. K for different n are shown in Figure 12 [3] and are the same as in Figure 14.11 [4]. According to (1) *SNR* can be increased without limit if n increases and $K \geq 4$. This result is not clear even without stability analysis. The second question is a possibility to increase *SNR* changing the gain A. These questions are investigated in the next section. The specific problems of noise in the case of narrow-band bandpass sigma-delta modulators are discussed in [6] but are not included in this paper.

Electrical noise was examined [7] for the switched-capacitor integrator (SCF) shown in Fig. 2.

The capacitor C_{IN} is connected between input voltage V_{IN} and ground or between ground and inverting input of the operational amplifier due to switches 1 and 2 with frequency f_{IN}. From transfer function point of view the capacitor C_{IN} acts as a resistor having a resistance [4,7]

$$R_{EQ} = \frac{1}{f_{IN} C_{IN}} \qquad (2)$$

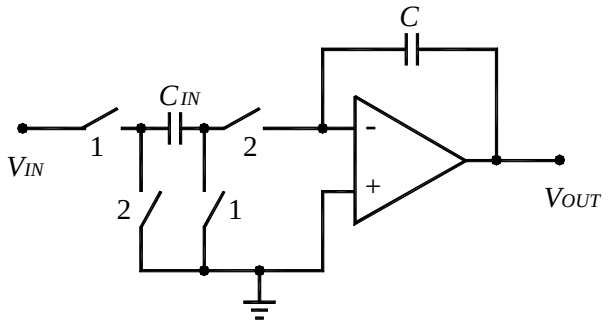

Fig. 2. Switched-capacitor integrator.

It is evident that (2) can be used to calculate the dependence of V_{OUT} on V_{IN}. It is not evident that (2) can be also utilized ([7] and several other papers) to find the Root-Mean-Square of thermal noise in accordance with well known equation (Nyquist noise)

$$RMS_T = \sqrt{4kTR_{EQ}\Delta f}\ , \tag{3}$$

where k is the Boltzman's constant that is equal to $k = 1.3807\cdot10^{-23}$ W×sec/°K, T is the absolute temperature, Δf – frequency band where the noise is evaluated. According to [7] and other papers mentioned there (3) is valid for a differential SCF while RMS_T of a single SCF is $\sqrt{2}$ times less. The influence of switched-capacitor bound with reference voltage is ignored. The authors of [7] suppose without any proofs that "the thermal noise generated by amplifier is less critical than that of switches". The most papers devoted to noise analysis ignored its dependence on gain. All mentioned statements will be considered in sections 3 and 4.

2. QUANTIZATION NOISE OF Σ–Δ ADC

2.1. Analysis in frequency domain

This noise is not a random error and can be considered as a random quantity in the case of random input signal. To calculate standard deviation or *RMS* of the noise the spectral intensity of a comparator must be found before. It is supposed that spectral intensity of a comparator S_C is constant within frequency band from zero to $0.5Kf_S$.

Analog filter (see Fig. 1) is based on the n integrators with transfer function in frequency domain

$$H(\omega) = \frac{1}{A(\omega\tau)^n} \tag{4}$$

Spectral intensity of the noise referred to input of analog filter is taking into account the model of comparator [3] described in Section 1

$$S_{IN} = \frac{S_C}{\eta^2 H^2(\omega)} \tag{5}$$

Integrator constant $\tau = RC$. For switch-capacitors techniques equivalent resistor R_{EQ} given by (2) can be used instead of R, then

$$\tau = \frac{1}{bKf_S}, \tag{6}$$

where

$$b = \frac{C_{IN}}{C} \tag{7}$$

Then quantisation noise equals to

$$RMS_Q^2 = \frac{\left(\pi^n V_{REF}\right)^2}{3(2n+1)} \cdot \frac{1}{K^{2n+1}} \cdot \left(\frac{A}{\eta b^n}\right)^2 \tag{8}$$

The third part of (8) shows the conversion of a voltage range from modulator input to comparator input. According to Section 1, the value of η must be chosen by the way which corresponds to the condition $A/\eta b^n = V_{FS}/4V_{REF}$, where V_{FS} is the full-scale voltage of the analog-to-digital converter based on given Σ–Δ modulator. Then (8) is simplified to

$$RMS_Q^2 = \frac{\left(V_{FS}\pi^n\right)^2}{48(2n+1)K^{2n+1}} \tag{9}$$

The problem of stability [3] forces to decrease RMS_Q by factor W, which depends on concrete circuit. Then

$$RMS_Q^2 = \frac{\left(WV_{FS}\pi^n\right)^2}{48(2n+1)K^{2n+1}} \tag{9a}$$

The factor W can also include any deflection from theory given above. Signal-to-noise ratio [1] is equal to

$$SNR = 10\log\left(\frac{6(2n+1)K^{2n+1}}{W^2\pi^{2n}}\right) \tag{10}$$

Let us compare (10) with (1). Equation (10) does not depend on A and shows the result 6 dB more than (1) if a=1 and W=1. Difference is produced due to choice of η value.

To find limitations of (10) in dependence on n and input frequency change, the analysis of quantization error in time domain is necessary.

2.2. Analysis in time domain

Now let us find the transfer function of Σ–Δ ADC. The schematics of the first and the second order Σ–Δ modulators are shown in Fig. 3 and Fig. 4 correspondingly.

The output of a comparator is supposed to be equal accurately to reference voltage V_{REF} or $-V_{REF}$ depending on the sign of its input voltage. Due to this approximation the 1-bit DAC (see Fig. 1) is not shown. All switches have two positions: 1 (shown in Fig. 3 and 4) and 2 (opposite). It is supposed $C_1 = C_2 = C_3$. The initial values of integrators outputs are supposed to be set to zero [5]. Transfer function of modulators were found and reflected Table 1 and Table 2.

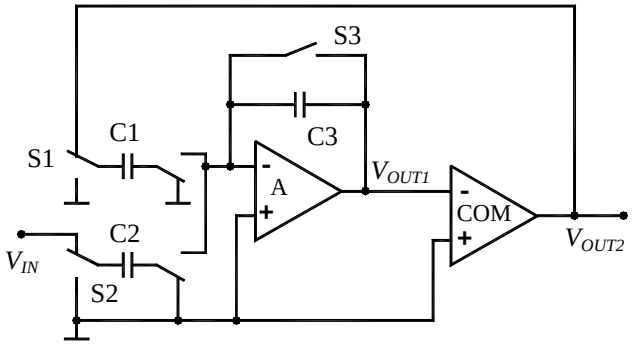

Fig. 3. The schematic of first order Σ–Δ modulator.

In order to save place it is accepted in the tables that $V_X = V_{IN} / V_{REF}$.

Codes in Tables 1 and 2 correspond to the stream of "1"s and "0"s at the output of comparator. These codes are transformed to desirable codes of ADC due to the digital filter shown in Fig. 1. The simplest digital filter is a digital counter [5]. It distinguishes only codes with different numbers of "1"s or "0"s. Transition from code 1011 to 1101, for example, is not distinguished by this filter. Numbers in the first column of Tables 1 and 2 show code transition levels. Bolded values are only ones, which take place for ADC with averaging filter. By applying a more sophisticated weighting filter [5], all codes shown in Table 1 can be theoretically reflected to output codes of Σ–Δ ADC and all code transition levels take place in the transfer function of Σ–Δ ADC. For considered example, averaging filter gives four code transitions, the same code bin widths, quantum $Q = 0.5V_{REF}$ and transfer function with zero differential and integral nonlinearity. A special digital filter gives possibility to use more code transitions. But code bin widths are not the same in the case of weighting digital filter. Therefore differential and integral nonlinearity arise. The former does not depend on kind of weighting averaging if all transformed codes are used. The latter depends on kind of weighting averaging. Corresponding absolute differential nonlinearity referred to V_{REF} is shown in Tables 1 and 2. As an example, weighting coefficients 0.4; 0.3; 0.2; 0.1 for "1"s or –0.4; –0.3; –0.2; –0.1 for "0"s at the 1, 2, 3 and 4th place in sequence of codes for $K = 4$ are used to build the transfer function and to calculate the integral nonlinearity. The middle of code transition levels is used to calculate this error [1]. One can find from Tables 1 and 2 that weighting averaging in comparison with simple averaging decreases maximum quantisation error but enters differential nonlinearity.

Table 1. Transfer function of the first order Σ–Δ modulator.

V_X range	Code	Code bin width	Differential nonlinearity	Output code with weighting coefficients	Integral nonlinearity with weighting coefficients
$-1 < V_X < \mathbf{-0.75}$	0000			–1.0	0
$\mathbf{-0.75} < V_X < -2/3$	0001	0.0833…	0.10	–0.8	–0.092
$-2/3 < V_X < -0.5$	0010	0.166…	0.021	–0.6	–0.017
$-0.5 < V_X < \mathbf{-0.25}$	0100	0.25	–0.063	–0.4	–0.025
$\mathbf{-0.25} < V_X < 0$	0101	0.25	–0.063	–0.2	–0.075
$0 < V_X < \mathbf{0.25}$	1010	0.25	–0.063	0.2	0.075
$\mathbf{0.25} < V_X < 0.5$	1011	0.25	–0.063	0.4	0.025
$0.5 < V_X < 2/3$	1101	0.166…	0.021	0.6	0.017
$2/3 < V_X < \mathbf{0.75}$	1110	0.0833…	0.10	0.8	0.092
$\mathbf{0.75} < V_X < 1$	1111			1.0	0

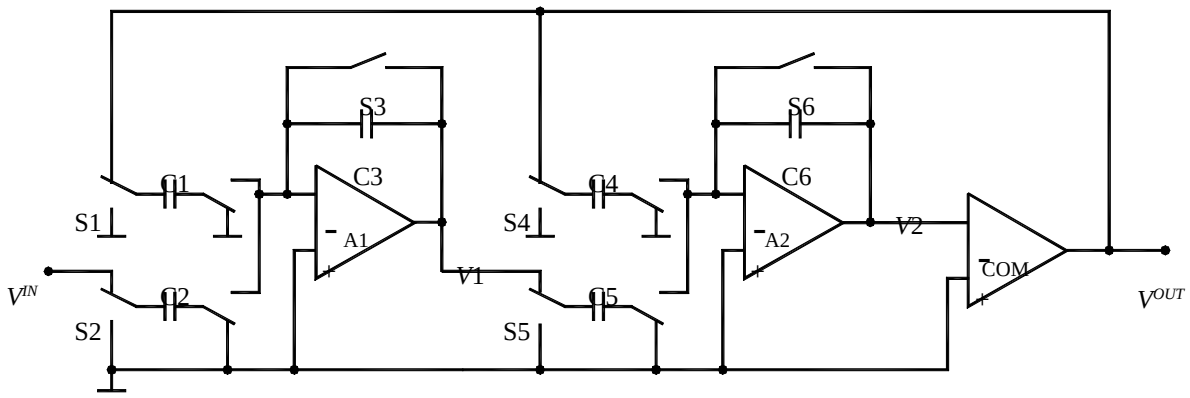

Fig. 4. The Σ–Δ modulator schematic of the second order.

Analysis in time domain allows to find some limitation of theory given in [3,4] and reflected in (9)–(10).

-Both differential and integral nonlinearity can take place in Σ–Δ ADC even with ideal capacitors, switches, operational amplifiers and comparator. These errors are not described by (9)-(10).

-According to (1), (9)-(10) quantisation noise can be decreased to any value for given K due to n increase. In fact increase of n gives more combination of codes for given K. But the number of such combinations is limited. For example, increase of n from 1 to 3 gives increase of code combinations from 10 to 12 if $K = 4$ (see Table 1 and Table 2). But the maximum number of code combinations equals to 16. If this number is got then following increase of n with $K = 4$ can not decrease *RMS* or increase *SNR* for any kind of weighting averaging.

Table 2. Transfer function of the second order Σ–Δ ADC.

V_X range	Code	Code bin width	Differential nonlinearity	Output code with weighting coefficients	Integral nonlinearity with weighting coefficients
$-1 < V_X <$ **–0.9**	0000			–1	0
–0.9 $< V_X <$ –5/6	0001	0.066…	0.11	–0.8	0.067
–5/6 $< V_X <$ –2/3	0010	0.166…	0.014	–0.6	0.15
–2/3 $< V_X <$ **–0.3**	0100	0.366…	–0.186	–0.4	0.083
–0.3 $< V_X <$ –1/6	0101	0.133…	0.047	–0.2	0.33
–1/6 $< V_X <$ 0	0110	0.166…	0.014	0	0.083
0 $< V_X <$ 1/6	1001	0.166…	0.014	0	–0.083
1/6 $< V_X <$ **0.3**	1010	0.133…	0.047	0.2	–0.033
0.3 $< V_X <$ 2/3	1011	0.366…	–0.186	0.4	–0.083
2/3 $< V_X <$ 5/6	1101	0.166…	0.014	0.6	–0.15
5/6 $< V_X <$ **0.9**	1110	0.066…	0.11	0.8	–0.067
0.9 $< V_X < 1$	1111			1.0	0

3. ELECTRICAL NOISE OF Σ–Δ ADC

According to Fig. 3 and 4 capacitor $C2$ is charged to input voltage without any error if noise of switches is not taken into account. By the same reason charge of this capacitor is transferred to the output of an operational amplifier without any noise if noise of the operational amplifier is not taken into account. Change of input sampling frequency is not important too because transferred charge equals to zero. Therefore, according to authors opinion, application of (2)–(3) to find noise is a mistake. Corresponding noise is absent both for single-ended and differential circuits.

Let us now discuss the noise of the operational amplifier. Only voltage noise will be discussed because very low input current of the operational amplifier is supposed. Let RMS of input noise within wide frequency band up to unity-gain frequency f_{OA} (more than 1 MHz usually) mark as E_{OA}. Two ways of operational amplifier noise influence on ADC performance are possible.

The first one is the noise, which goes to the output of the operational amplifier constantly. The value of this noise is important at the moment when capacitor C_5 is disconnected from the first operational amplifier (for the second order modulator shown in Fig. 4).

The second way of operational amplifier noise influence is realized due to commutation of capacitor C_2 with frequency f_{IN} and to commutation of capacitor C_1 with frequency f_{REF}. The value of this noise is important at the moments when capacitor C_1 or C_2 are disconnected from the operational amplifier. If mentioned moments are different then two noise parts are independent. The more frequency of commutation the more influence of the second way. The gain of the ADC (G) is usually increased by increase of commutation frequency at low gain and by decrease of $C1$ at high gain [2]. That is why the noise referred to input can decrease vs. gain faster then square of commutation frequency f_{IN} at low gains as it is clear from (11). The model [3] given by (2)–(3) supposes that noise is proportional to $\sqrt{f_{IN}}$.

The influence of the comparator and the following operational amplifiers (in the case of order n>1) on the noise is supposed to be negligible in comparison with the influence of the first operational amplifier.

Let us now discuss noise of switches. Let on-resistance of switches S_1 and S_2 mark as $R_{SW\cdot1}$ and $R_{SW\cdot1}$ correspondingly. When the switches connect inverting input of the operational amplifier through capacitors C_2 and C_1 to the ground, the noise of these switches is transferred to the output of the operational amplifier just as the second way of E_{OA} influence. It means that the influence of switches at high gains is important if spectral density of the switches noise is the same or more than spectral density of the operational amplifier. The typical value of on-resistance is 5 kΩ [2]. One can find from white noise model of resistance that spectral density is about 9 nV/$\sqrt{Hz}$ or RMS of noise is $E_{SW} = \sqrt{4kTR_{SW}\Delta f}$ = =9 μV within the frequency band from zero to 1 MHz. The operational amplifier must be a low-power device with low settling time. Under these conditions spectral density is usually more than 20 nV/$\sqrt{Hz}$ and noise of switches becomes negligible.

A unity gain buffer amplifier [2] is often used in order to increase the input resistance with regard to V_{IN}. This amplifier is also the source of electronic noise. Let us describe noise *RMS* of the buffer amplifier as E_B. The digital filter (see Fig. 1) with output data frequency f_S decreases standard deviation of electronic noise by K times. Electronic noise referred to input of ADC accepting that all sources of noise are independent is

$$RMS_E = \frac{f_S C_3}{f_{IN} C_2 \sqrt{K}} \times \tag{11}$$

$$\times \sqrt{E_{OA}^2 \left(1 + \left(\frac{C_2}{C_3}\right)^2 \frac{f_{IN}}{f_S} + \left(\frac{C_1}{C_3}\right)^2 \frac{f_{REF}}{f_S}\right) + E_B^2 \left(\frac{C_2}{C_3}\right)^2 \frac{f_{IN}}{f_S}}$$

Total RMS of error produced both by quantisation and electronic noise is

$$RMS_{TOT} = \sqrt{RMS_Q^2 + RMS_E^2} \tag{12}$$

4. COMPARISON OF THEORY WITH EXPERIMENTAL DATA

The proposed theory was checked by experimental data of [2]. The quantization noise dominates at comparatively high f_S. From (3) and experimental data [2] for conditions $n = 2$, $K = 19$ (it corresponds to maximum possible $f_S \approx 1$ kHz), $V_{FS} = (2V_{REF} / G) = 5$ V/G, the average value of W was found: $W_{av} = 1.3602$. Using this result, RMS_Q was calculated for different G by (9a) and compared with experimental data of [2].

The experimental results [2] for the lowest frequency $f_S = 5$ Hz where $K = 3840$ (quantisation noise is negligible here) were used to find equivalent value of operational amplifier noise E_{OA} from (11). The average value $\overline{E}_{OA} = 38.5$ μV was found which was much more than possible value of switches noise. Then this value was used to calculate RMS_E of noise for different gains G. The comparison of experimental and calculated results have shown error less than 20% and is negligible. Both theory (11) and experiment show dependence of noise on gain (or f_{IN}) more faster than $\sqrt{f_{IN}}$ in opposite to theory [7] given by (2)–(3).

Average value of buffer noise RMS, $\overline{E}_B = 50$ μV, was also found from experimental results [1] and (11). In accordance both to (11) and experimental data, the influence of the buffer and the operational amplifier is practically the same at high gains while noise of the operational amplifier dominates at $G = 1$. The calculated values of $\overline{E}_{OA}$ and $\overline{E}_B$ were used to predict by (12) the total noise of the ADC for other combinations of K, f_S, G and $V_{REF.}$ Modelling error was less than 30 % and is negligible. It means that the proposed model can be considered as metrological one.

To evaluate the uncertainty of A/D conversion with given confident probability P it is necessary to multiply the result found from (12) by corresponding coefficient γ. If, for example, P = 0.95 then γ≈2.

5. CONCLUSIONS

5.1.The equations to evaluate the RMS of Σ–Δ ADC quantization noise (9), (9a) and the SNR (10) were found from analysis in frequency domain under ideal conditions. A coefficient W is supposed to take into account real conditions.

5.2. The analysis in time domain allowed to find some differences between idealized and real conditions of Σ–Δ ADC performance including following:

5.2.1. A differential and integral nonlinearity can take place in Σ–Δ ADC even with ideal electronic elements (switches, operational amplifiers, comparator etc.).

5.2.2. For given oversampling ratio K, the improvement of SNR due to increase of analog filter order n has a limit besides stability. This limit is defined by the number of code combinations in K symbols of "1" or "0".

5.3. Electronic noise does not depend on both switched capacitance and input sampling frequency of Σ–Δ modulator with ideal elements. The most important source of electronic noise at low gain is the operational amplifier, at high gains the influence of operational amplifier and the buffer is approximately the same. The transfer of switches noise is the same as of the operational amplifier at high gains. For real elements the noise of switches is usually negligible for all gains.

5.4. Improved model of Σ–Δ ADC allows to evaluate the random error with given probability (typically P=1) using only three measured or specified parameters (W, E_{OA}, E_B). The evaluation is valid for wide ranges of full-scale input voltage (or gain and reference voltage), output data rate, oversampling ratio, input sampling frequency, with the buffer amplifier or without it.

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